General Semiconductor Industries, Inc.

SEMICONDUCTOR PRODUCT DATABOOK - 11TH EDITION

General Semiconductor Industries, Inc.

DIODE AND TRANSISTOR PRODUCT CATALOG

This catalog contains a complete listing of standard products manufactured by General Semiconductor Industries, Inc.

This catalog is designed to supply the user with industry standards on transient voltage suppressors (TVS), zener diodes, and power switching transistors. Complete device characterization is also supplied on General Semiconductor's special TransZorb® silicon transient voltage suppressor and C^2R® high speed, high voltage switching transistor.

HOW TO USE THIS CATALOG:

Devices are listed by product classification; that is, Transient Voltage Suppressors, Zener Diodes, and Transistors.

TransZorb TVSs are listed by JEDEC types first, followed by product type numbers in numeric alpha sequence. Transistors are categorized by continuous collector current rating.

A numeric alpha index is located in the front section of the catalog indicating the section and page number for each product.

HOW TO ORDER:

All devices in this catalog are available through your local distributor. For special device selection, consult your *General Semiconductor Industries sales representative*, or

General Semiconductor Industries, Inc.
2001 West Tenth Place
Tempe, Arizona 85281
Phone: (602) 968-3101
FAX: (602) 966-6396

General Semiconductor (Ireland) Ltd.
Macroom
County Cork IRELAND
Phone: (353)(26) 41401
FAX: (353)(26) 42716

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For literature on Square D Transient Voltage Surge Suppression end user products, please contact GSI's Literature Department at (602) 968-3101.

DESIGN CHANGES

General Semiconductor Industries, Inc., reserves the right to discontinue product lines and that the final judgement concerning selection and specifications is the buyer's and that in furnishing engineering and technical assistance, seller assumes no responsibility with respect to the selection or specifications of such products.

SPECIFICATIONS

General Semiconductor Industries, Inc., reserves the right to change electrical and or mechanical characteristics (except JEDEC) as specified herein.

NUMERIC / ALPHA INDEX — DIODES

Available in JAN and JANTX(V)

NUMERIC / ALPHA INDEX — DIODES (Cont'd)

★ NEW PRODUCT

See individual data sheets for suffix types.

NUMERIC / ALPHA INDEX — DIODES (Cont'd)

★ NEW PRODUCT

See individual data sheets for suffix types.

★ NEW PRODUCT

See individual data sheets for suffix types.

NUMERIC / ALPHA INDEX — DIODES (Cont'd)

★ NEW PRODUCT

NUMERIC / ALPHA INDEX — DIODES (Cont'd)

★ NEW PRODUCT

NUMERIC / ALPHA INDEX — TRANSISTORS

★ NEW PRODUCT

Available in JAN and JANTX(V)

SECTION 1

TRANSIENT VOLTAGE SUPPRESSORS

TRANSZORB® TVS
DEFINITIONS AND SPECIFICATIONS

TransZorb suppressors are semiconductor devices which are designed, manufactured, specified and tested for transient voltage suppression applications.

TransZorb suppressors are PN Silicon transient voltage suppressors that are characterized by their phenomenal surge handling capabilities, extremely fast response time (1×10^{-12} seconds), and low series resistance (R_{on}).

There are four basic sources of transients:

1. Lightning or induced lightning effects.
2. Inductive switching (EMI).
3. Electrostatic discharge (ESD).
4. Nuclear EMP (NEMP).

The TransZorb transient voltage suppressors have been used effectively for many years in telecommunication applications where lightning induced voltage can seriously damage voltage sensitive components. The devices have been tested and proven effective to the following domestic and international specifications:

REA (Rural Electrification Administration)
PE-60.
Condition: 100v/μs rise, 10 x 1000μs, 1KV

FCC (Federal Communication Commission)
Docket 19528, Part 68.
Condition: Longitudinal— 10 x 160μs, 1500v
Metalic— 10x 560μs, 800V

CCITT (Consultative Committee, International Telegraph & Telephone)
Record K17.
Condition: Repeaters— 10 x 800μs, 6KV,
100 x 800μs, 5KV

Some additional Industry Standard Transients are listed below:

IEEE (Institute of Electrical & Electronic Engineers)
IEEE Standard 472 (ANSI C37.90a-1974)
Condition: Surge Withstand Capability— 1.5 MHz oscillatory wave, 3KV
IEEE Standard 587 (ANSI C62.41-1981)
Condition: Long Branch Circuits— 0.5μs-100KHz oscillatory wave 6KV
Short Branch Circuits— 1.2 x 50μs impulse wave 6KV

SAE (Society of Automotive Engineers)
Aerospace Standard AS1212
Condition: Transient Surge— 50ms, 180 volts
Transient Spike— 10μs, 600 volts
Electromagnetic Susceptible Test Procedures for Vehicle Components.
Specification SAE J1113
Condition: Load Dump & Field Decay— 100ms, 150V
Repetitive Spike— 10μs, 200V

NEMP (Nuclear Electromagnetic Pulse)
Condition: Damped Sinewave— 10μs max., 1KV

Military Transient Specifications
MIL-STD-704 (Aircraft Electrical System Characteristics)
DC 1 x 5μs, 600volts;
50ms, 80volts;
ac 10ms, 180volts.
MIL-STD-1399 (DOD-STD-1399) (Interface Standard for Shipboard Systems, Section 103, Electric Power)
1.5 x 40μs, 2500 volts.
MIL-STD-1275 (Military Vehicles, 28 volt Electrical Systems)
Voltage Spikes— .05μs oscillatory wave <500KHz, 250 volts;
Voltage Surge— 50ms, 100volts

TransZorb suppressors have proven to be effective in Airborne Avionics and Controls, Mobile Communications equipment, Computer power supplies, Numerically Controlled Machinery, and in many other applications where inductive and switching transients are present.

With their fast response times and low clamping factors, TransZorb suppressors can protect Integrated Circuits, MOS devices, Hybrids, and other voltage-sensitive components. TransZorb suppressors can also be used in series or parallel to increase the peak power ratings.

TransZorb suppressors have been evaluated for susceptibility to neutron and gamma radiation. Neutron flux irradiation of 1.4×10^{13} neutrons/cm and cumulative gamma dosage of 2×10^{7} rad(Si) have been applied to the TransZorb suppressor without causing appreciable parameter changes.

They have also been proven effective for EMP suppression. For actual test results and applications send for the EMP report #AD 909267L, at the Defense Documentation Center, Alexandria, Virginia 22314.

Because of the unpredictable nature of transients and the variation of the impedance with respect to these transients, impedance (R_{on}) is not specified as a parametric value. However, a minimum voltage (BV) at low current conditions and a maximum clamping voltage (V_C) at a maximum peak pulse current is specified.

The maximum observed clamping voltage (V_c) is approximately the same for all pulses shown within the limits of the curve in Figure 1. In some instances, the thermal effect may be responsible for 50 to 70% of the observed change in voltage when subjected to high current pulses or severe duty cycles. The maximum reverse leakage current must be doubled for voltage types up to 11 volts for bipolar devices.

Figure 2 shows a typical power derating curve for TransZorb suppressors when derated above 25°C. Clamping voltage vs. varying peak pulse current curves at one millisecond, extended power curves vs. time, and detailed technical data sheets are available.

When selecting a TransZorb suppressor, first determine the transient condition or the source of the pulse for each application. Specify maximum dc or ac peak voltage with tolerance. This maximum voltage level should be equal to or less than the reverse stand-off voltage of the TransZorb suppressor.

Consider what is the minimum and maximum voltage for a given circuit.

Because of the temperature coefficient, the minimum breakdown voltage (BV) should be considered as the reverse stand-off voltage (V_T) when operating at the extreme temperature of -65°C.

The maximum clamping voltage (V_c) is a desired voltage to provide adequate protection for a circuit component.

Determine the proper device according to the peak pulse power. This can be accomplished by knowing the source impedance and the maximum transient voltage. Once the maximum peak pulse current (I_{pp}) is known (and if its value is less than the maximum I_{pp}), use the maximum clamping voltage (V_c) to calculate power for worst case design for most applications.

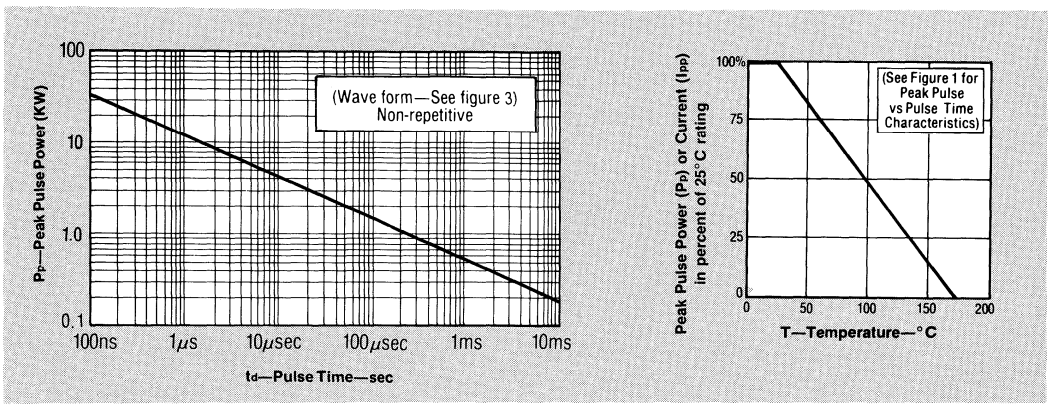


FIGURE 1—Peak Pulse Power vs Pulse Time For a 600 Watt Device

FIGURE 2
Power or Current vs. Temperature Derating Curve

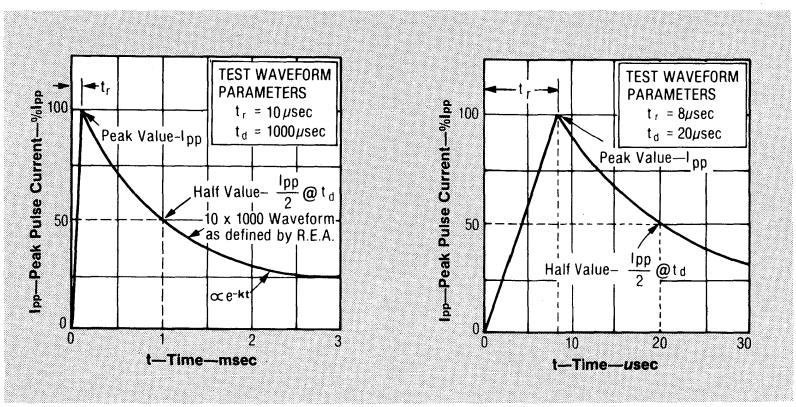


FIGURE 3—Pulse Waveform (10/1000*us*)

FIGURE 3A—Pulse Waveform (8/20*us*)

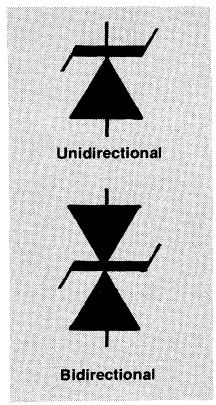


FIGURE 4
TransZorb Circuit Symbols

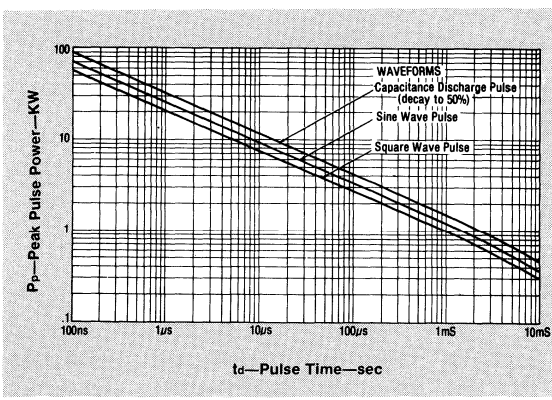


FIGURE 5—Peak Pulse Power vs Pulse Time For a 1500 Watt Device

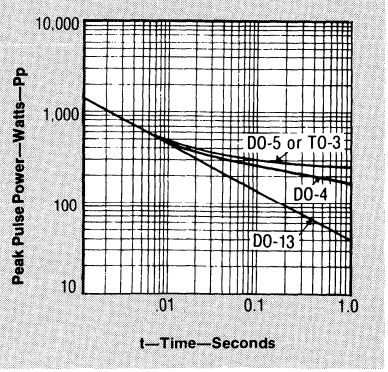


FIGURE 6
Peak Pulse Power vs Pulse Time (Extended)

TRANSZORB TVS QUICK REFERENCE GUIDE

PEAK PULSE POWER RANGE	LOW								MEDIUM			
PEAK PULSE POWER RATING @ 1mS	500W				600W			700W	1500W			
APPLICATION	Computer, Consumer, Medical										Military	
SERIES	GMP-5 thru GMP-58	SA5.0 thru SA170A	SAB5.0 thru SAB28	SAC5.0 thru SAC50 *	P6KE6.8 thru P6KE400A *	SMB5.0 thru SMB170A	SMB6.5C thru SMB43CA **	SBL10 thru SBL100C *	SMC5.0 thru SMC170A	SMC6.5C thru SMC43CA **	1N5555 thru 1N5558	1N5629 thru 1N5665A	1N5907 thru 1N5908
PAGE REFERENCE	Page 1-36	Page 1-48	Page 1-52	Page 1-53	Page 1-44	Page 1-56	Page 1-58	Page 1-55	Page 1-60	Page 1-62	Page 1-6	Page 1-8	Page 1-10
0	5.0	5.0	5.0	5.0	5.5	5.0	6.5	10	5.0	6.5		5.5	5.0
		6.5*			7.5*								
25			28								30		
50				50			43			43			
100		170				170		100	170		175	171	
200					340								
400													
800													

Reverse Stand-Off Voltage — V_R — Volts (Note 1)

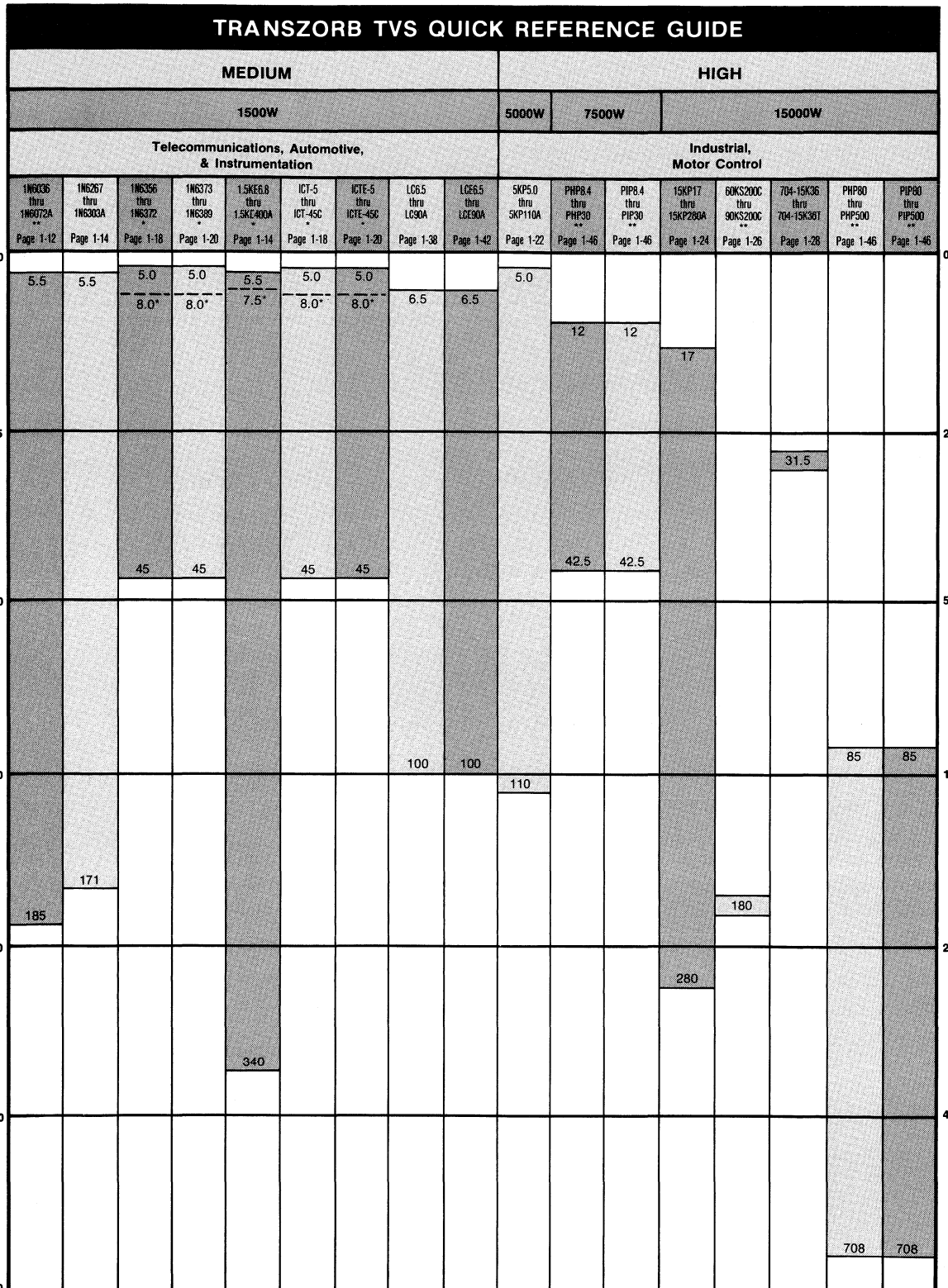
NOTE: Arrow indicates surface mount devices available with "Gull-Wing" and modified J-Bend leads.

Note 1: A TransZorb TVS is normally selected according to the reverse "Stand-Off Voltage" (V_R) defined as the applied voltage to assure a nonconductive condition.

How to use the "TransZorb TVS Quick Reference Guide":

1) Determine the required Stand-Off Voltage. On the Quick Reference Guide the Stand-Off Voltage is represented by the first column of figures to the left—reading top to bottom: **0, 25, 50** etc.
2) At the required Stand-Off Voltage, read horizontally to the right to the required Peak Pulse Power rating—reading from left to right **500W, 600W, 700W** etc.
3) At the intersecting area of the required Stand-Off Voltage and Peak Pulse Power rating, jot down the part series numbers and the catalog page reference numbers (found at the head of the shaded columns).
4) Refer to the applicable page numbers for the series description, application and specific electrical characteristics. **Note:** A single asterisk (*) after the series numbers indicates the availability for BIDIRECTIONAL application; a double asterisk (**) indicates the series is for BIDIRECTIONAL application ONLY, series listed without asterisks are UNIDIRECTIONAL ONLY.

TRANSZORB TVS QUICK REFERENCE GUIDE



TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
1N5555 THRU 1N5558

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **MIL qualified per MIL-S-19500/434**
- **Designed for DC applications**
- **Hermetically sealed package**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 200amps, 1/120 second at 25° C
- Steady State power dissipation: 1.0 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package, glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band
- Standard Polarity — Cathode to Case
- Body marked with Logo ⁂ and type number

APPLICATION

. . .a series of Silicon Transient Suppressors for use primarily in Airborne Equipment where large voltage transients endanger voltage sensitive components. The TransZorb meets all requirements of MIL-S-19500/434. JAN and JANTX units are available.

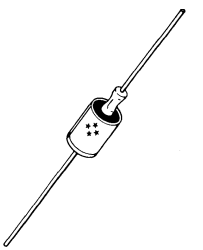
Because the response time of the TransZorb's clamping action is effectively instantaneous (better than 1×10^{-12} sec.), they can protect Integrated Circuits, MOS Fets, Hybrids and other voltage sensitive semiconductors and components. Due to the high surge capability and fast response time, they have also been proven effective EMP suppressors.

DESCRIPTION

These devices were designed with MIL-STD-704 as the controlling specification. In most cases the source impedance is not specified and can vary from .2 ohm to 150 ohms. The TransZorb will operate with a minimum of 1 ohm source impedance. If the source impedance is known to be less, either an inductive or resistive load should be added in series to limit the current flow.

Energy within a voltage transient is not infinite and thus will decay when shunted by the TransZorb, reflecting some energy back to the source or distributed impedance. In case of a severe, abnormal transient beyond the maximum ratings, the TransZorb will initially fail "short" thus tripping the system's circuit breaker or fuse while protecting the entire circuit.

CASE DO-13



CASE OUTLINE

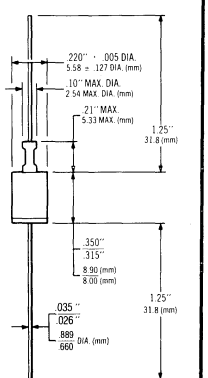


FIGURE 1—Peak Pulse Power vs Pulse Time

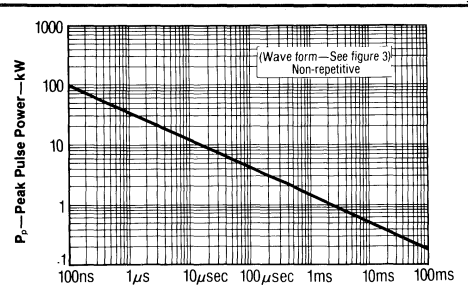
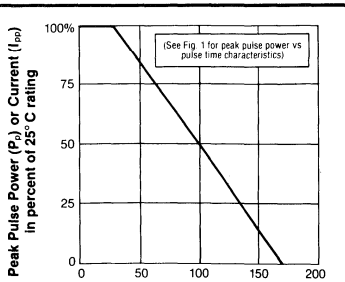


FIGURE 2—Derating Curve



TRANSZORB® UNIDIRECTIONAL 1N5555 THRU 1N5558

ELECTRICAL CHARACTERISTICS @ 25°C

JEDEC TYPE NUMBER**	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1 mA BV VOLTS	MAXIMUM CLAMPING VOLTAGE @I_{pp} (FIG. 3) V_C VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{pp} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
1N5555	30.5	33.0	47.5	5	32	31
1N5556	40.3	43.7	63.5	5	24	48
1N5557	49.0	54.0	78.5	5	19	65
1N5558	175.0	191.0	265.0	5	5.7	210

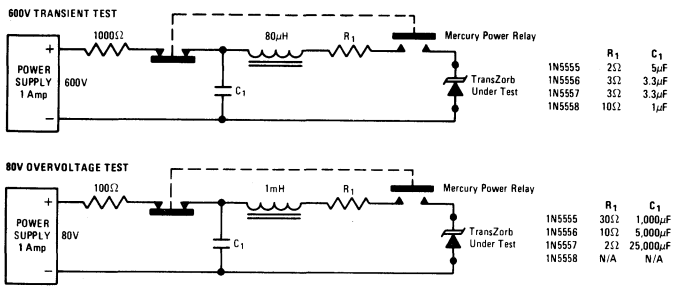
JEDEC Registered Data

Available in JAN, JANTX and JANTXV per MIL-S-19500/434

V_f at 100 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

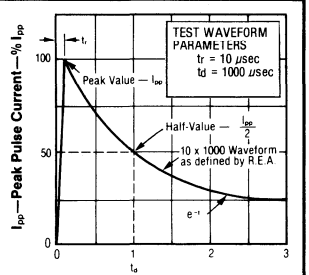
**For Bipolar applications, consult factory.

TYPICAL TEST CIRCUITS FOR SYSTEM CAPABILITY



For applications requiring higher surge devices, refer to Part Number 60KS200C for equivalent conditions; or Part Number 704-15K36T for equivalent DC conditions.

FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)

BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25° C.

V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} Peak Pulse Current — See Figure 3

P_p Peak Pulse Power

I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
1N5629 THRU 1N5665A

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 5.5 to 171 volts**
- **MIL qualified per MIL-S-19500/500**
- **Hermetically sealed package**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 200amps, 1/120 second at 25° C
- Steady State power dissipation: 1.0 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package, glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band
- Standard Polarity — Cathode to Case
- Body marked with Logo ⁂ and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

APPLICATION

This specification sheet defines a series of Silicon Transient Suppressors used in applications where large voltage transients can permanently damage voltage-sensitive components.

APPLICATION CONT'D

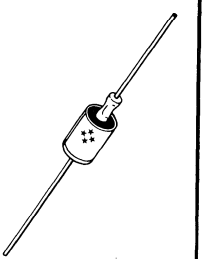
The TransZorb® can be use in applications where induced lightning or rural or remote transmission lines presents a hazard to electronic circuitry (reg: R.E.A. specification P.E. 60). The response time of TransZorb clamping action is theoretically instantaneous (1×10^{-12} sec.); therefore, they can protect Integrated Circuits, MOS devices, Hybrids, and other voltage-sensitive semiconductors and components. TransZorbs can also be used in series or parallel to increase the peak power ratings.

This series of devices has proven very effective as EMP Suppressors — as described in Defense Department report AD 909267L.

DESCRIPTION

TransZorbs are characterized by their high surge capability, extremely fast response time, and low shunt resistance (R_{on}). The shunt resistance is less than 1 ohm and therefore, is not specified as a parameter value. During a high current pulse, as much as 50% to 70% of the observed clamping voltage can be due to thermal effects. A clamping factor is provided to determine the maximum clamping voltage (V_C) at a specified breakdown voltage (BV). In case of a severe current overload or abnormal transient beyond the maximum ratings, the TransZorb will initially fail "short" thus tripping the system's circuit breaker or fuse while protecting the entire circuit. Curves depicting clamping voltage vs. various current pulses are available from the factory. Extended power curves vs. pulse time are also available.

CASE DO-13



CASE OUTLINE

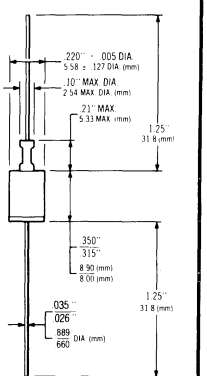


FIGURE 1—Peak Pulse Power vs Pulse Time

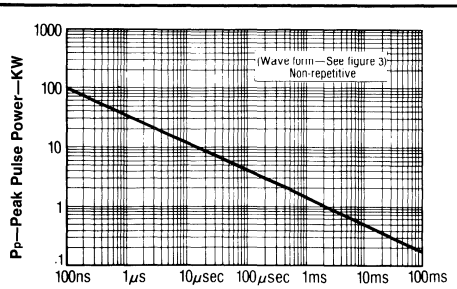
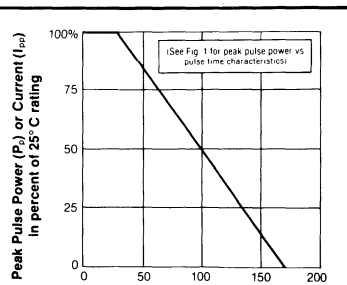


FIGURE 2—Derating Curve



TransZorb® UNIDIRECTIONAL

1N5629 THRU 1N5665A

ELECTRICAL CHARACTERISTICS @ 25°C (JEDEC Registered Data)

JEDEC TYPE NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS MIN.	BREAKDOWN VOLTAGE BV VOLTS MAX.	@ I_T mA	MAXIMUM CLAMPING VOLTAGE @I_{pp} (FIG. 3) V_C VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R uA	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{pp} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
1N5629	5.50	6.12	7.48	10	10.8	1000	139	5.0
1N5629A	5.80	6.45	7.14	10	10.5	1000	143	5.0
1N5630	6.05	6.75	8.25	10	11.7	500	128	5.0
1N5630A	6.40	7.13	7.88	10	11.3	500	132	5.0
1N5631	6.63	7.38	9.02	10	12.5	200	120	6.0
1N5631A	7.02	7.79	8.61	10	12.1	200	124	6.0
1N5632	7.37	8.19	10.0	1	13.8	50	109	7.0
1N5632A	7.78	8.65	9.55	1	13.4	50	112	7.0
1N5633	8.10	9.00	11.0	1	15.0	10	100	8.0
1N5633A	8.55	9.5	10.5	1	14.5	10	103	8.0
1N5634	8.92	9.9	12.1	1	16.2	5	93	9.0
1N5634A	9.40	10.5	11.6	1	15.6	5	96	9.0
1N5635	9.72	10.8	13.2	1	17.3	5	87	10
1N5635A	10.2	11.4	12.6	1	16.7	5	90	10
1N5636	10.5	11.7	14.3	1	19.0	5	79	11
1N5636A	11.1	12.4	13.7	1	18.2	5	82	11
1N5637	12.1	13.5	16.5	1	22.0	5	68	13
1N5637A	12.8	14.3	15.8	1	21.2	5	71	12
1N5638	12.9	14.4	17.6	1	23.5	5	64	16
1N5638A	13.6	15.2	16.8	1	22.5	5	67	14
1N5639	14.5	16.2	19.8	1	26.5	5	56.5	17
1N5639A	15.3	17.1	18.9	1	25.2	5	59.5	19
1N5640	16.2	18.0	22.0	1	29.1	5	51.5	20
1N5640A	17.1	19.0	21.0	1	27.7	5	54	19
1N5641	17.8	19.8	24.2	1	31.9	5	47	21
1N5641A	18.8	20.9	23.1	1	30.6	5	49	20
1N5642	19.4	21.6	26.4	1	34.7	5	43	25
1N5642A	20.5	22.8	25.2	1	33.2	5	45	23
1N5643	21.8	24.3	29.7	1	39.1	5	38.5	28
1N5643A	23.1	25.7	28.4	1	37.5	5	40	25
1N5644	24.3	27.0	33.0	1	43.5	5	34.5	31
1N5644A	25.6	28.5	31.5	1	41.4	5	36	28
1N5645	26.8	29.7	36.3	1	47.7	5	31.5	31
1N5645A	28.2	31.4	34.7	1	45.7	5	33	30
1N5646	29.1	32.4	39.6	1	52.0	5	29	35
1N5646A	30.8	34.2	37.8	1	49.9	5	30	31
1N5647	31.6	35.1	42.9	1	56.4	5	26.5	39
1N5647A	33.3	37.1	41.0	1	53.9	5	28	36
1N5648	34.8	38.7	47.3	1	61.9	5	24	46
1N5648A	36.8	40.9	45.2	1	59.3	5	25.3	44
1N5649	38.1	42.3	51.7	1	67.8	5	22.2	50
1N5649A	40.2	44.7	49.4	1	64.8	5	23.2	48
1N5650	41.3	45.9	56.1	1	73.5	5	20.4	55
1N5650A	43.6	48.5	53.6	1	70.1	5	21.4	51
1N5651	45.4	50.4	61.6	1	80.5	5	18.6	58
1N5651A	47.8	53.2	58.8	1	77.0	5	19.5	56
1N5652	50.2	55.8	68.2	1	89.0	5	16.9	65
1N5652A	53.0	58.9	65.1	1	85.0	5	17.7	62
1N5653	55.1	61.2	74.8	1	98.0	5	15.3	71
1N5653A	58.1	64.6	71.4	1	92.0	5	16.3	69
1N5654	60.7	67.5	82.5	1	108.0	5	13.9	80
1N5654A	64.1	71.3	78.8	1	103.0	5	14.6	76
1N5655	66.4	73.8	90.2	1	118.0	5	12.7	90
1N5655A	70.1	77.9	86.1	1	113.0	5	13.3	86
1N5656	73.7	81.9	100.0	1	131.0	5	11.4	99
1N5656A	77.8	86.5	95.5	1	125.0	5	12.0	94
1N5657	81.0	90.0	110.0	1	144.0	5	10.4	109
1N5657A	85.5	95.0	105.0	1	137.0	5	11.0	104
1N5658	89.2	99.0	121.0	1	158.0	5	9.5	120
1N5658A	94.0	105.0	116.0	1	152.0	5	9.9	115
1N5659	97.2	108.0	132.0	1	173.0	5	8.7	131
1N5659A	102.0	114.0	126.0	1	165.0	5	9.1	125
1N5660	105.0	117.0	143.0	1	187.0	5	8.0	142
1N5660A	111.0	124.0	137.0	1	179.0	5	8.4	136
1N5661	121.0	135.0	165.0	1	215.0	5	7.0	164
1N5661A	128.0	143.0	158.0	1	207.0	5	7.2	157
1N5662	130.0	144.0	176.0	1	230.0	5	6.5	175
1N5662A	136.0	152.0	168.0	1	219.0	5	6.8	167
1N5663	138.0	153.0	187.0	1	244.0	5	6.2	186
1N5663A	145.0	162.0	179.0	1	234.0	5	6.4	188
1N5664	146.0	162.0	198.0	1	258.0	5	5.8	197
1N5664A	154.0	171.0	189.0	1	246.0	5	6.1	188
1N5665	162.0	180.0	220.0	1	287.0	5	5.2	219
1N5665A	171.0	190.0	210.0	1	274.0	5	5.5	209

V_f at 100 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

Available in JAN, JTX & JTXV per MIL-S-19500/500.

FIGURE 3—Pulse Waveform

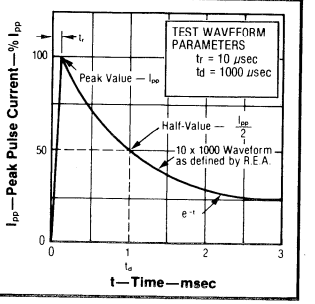
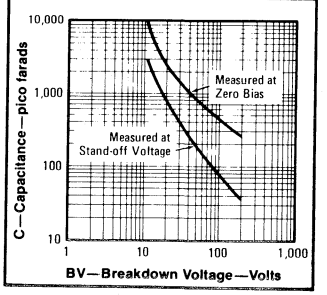


FIGURE 4—Typical Capacitance vs Breakdown Voltage



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)

BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} Peak Pulse Current — See Figure 3

P_p Peak Pulse Power

I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
1N5907 AND 1N5908

FEATURES

- **5.0 volts Reverse Stand-Off voltage**
- **Designed for T²L Logic protection**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 200amps, 1/120 second at 25° C
- Steady State power dissipation: 1N5907 — 1.0 watt; 1N5908 — 5.0 watts at T_L = 75° C, Lead Length = 3/8"
- Repetition rate (duty cycle): 1N5907 — .01%, 1N5908 — .05%

MECHANICAL CHARACTERISTICS

- 1N5907 — Standard DO-13 package, hermetically sealed
- 1N5908 — Molded Case — Case 1
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band
- Body marked with Logo and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual V_c (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

Capacitance: 15,000 pF at 0 Volts (typical).

APPLICATION

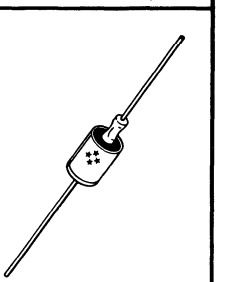
...Silicon Transient Suppressors introduced and registered by General Semiconductor Industries for the protection of 5.0 volt logic circuits. The 1N5907 and 1N5908 protect TTL, ECL, DTL,MOS and MSI integrated circuits requiring 5.0 volt or lower power supplies. These devices are rated for a peak pulse power of 1500 watts for 1 millisecond.

DESCRIPTION

The 1N5907 TransZorb®, packaged in a hermetically sealed glass-to-metal package, is available in JAN, JANTX and JANTXV qualified to MIL-S-19500/500.

These devices are specified at high current pulses, such type that would be seen from inductive switching transients. They provide both protection from line transients as well as preventing transients from being injected onto the line. Both hermetic seal and molded types are available, depending upon the application and environmental conditions.

CASE DO-13



CASE 1

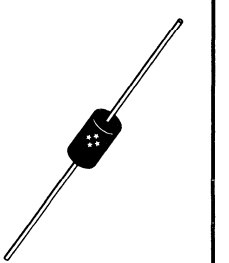


FIGURE 1—Peak Pulse Power vs Pulse Time

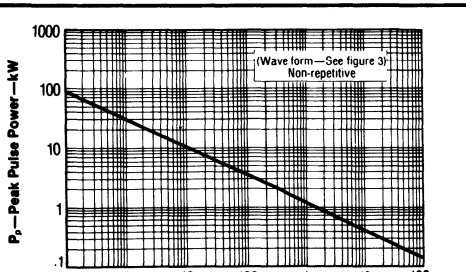
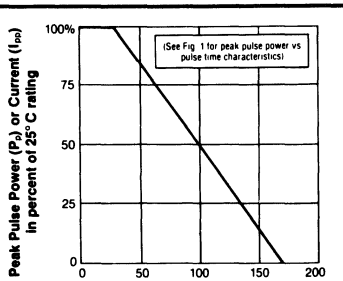


FIGURE 2—Derating Curve



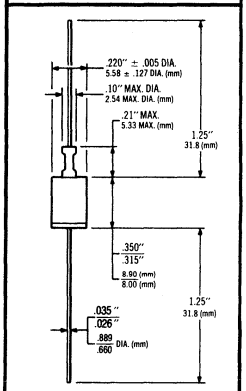
TRANSZORB® UNIDIRECTIONAL 1N5907 AND 1N5908

ELECTRICAL CHARACTERISTICS @ 25°C (JEDEC Registered Data)

JEDEC TYPE NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1 mA V_C VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @I_{pp1} (FIG. 3) V_C VOLTS	PEAK PULSE CURRENT (FIG. 3) I_{pp1} A	MAXIMUM CLAMPING VOLTAGE @I_{pp2} (FIG. 3) V_C VOLTS	PEAK PULSE CURRENT (FIG. 3) I_{pp2} A	MAXIMUM CLAMPING VOLTAGE @I_{pp3} (FIG. 3) V_C VOLTS	PEAK PULSE CURRENT (FIG. 3) I_{pp3} A
1N5907	5.0	6.0	300	7.6	30	8.0	60	8.5	120
1N5908	5.0	6.0	300	7.6	30	8.0	60	8.5	120

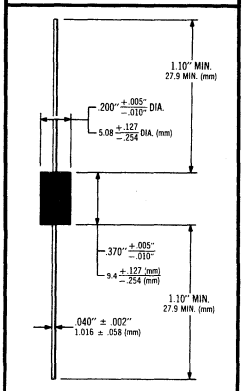
Available in JAN, JTX & JTXV per MIL-S-19500/500.

CASE OUTLINE



CASE DO-13

CASE OUTLINE

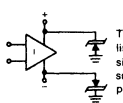


CASE 1

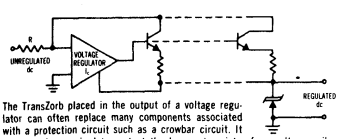
APPLICATION NOTES

The **1N5907** and **1N5908** TransZorbs are characterized by the reverse stand-off voltage (VR). They are compatible with the integrated circuit power supply voltage. The breakdown voltage (BV) is that point at which the TransZorb is in avalanche breakdown. This point is temperature dependent and has a positive temperature coefficient. Allowance has been made in establishing the minimum breakdown voltage at 25°C to provide safe operation over the full military temperature range.

DC LINE APPLICATIONS

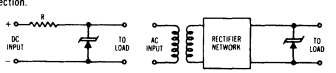


The TransZorb suppressor on the power line prevents IC failure caused by transients (electrostatic discharge), power supply reversals or during switching of the power supply to on or off.



The TransZorb placed in the output of a voltage regulator can often replace many components associated with a protection circuit such as a crowbar circuit. It may also be required to protect the bypass transistor from voltage spikes across the collector to emitter terminals.

Typical power sources employing the TransZorb for Voltage Transient Protection.



The TransZorb is chosen in which the reverse stand-off voltage is equal to or greater than the DC output voltage. For certain applications it may be more desirable to replace the series resistor (R) with an inductor. In most applications, a fuse in the line is desirable. Elimination of a transformer will require an LC filter on the line for most industrial applications, when the TransZorb is placed on the input to the power supply and with an input voltage greater than 40 volts.

FIGURE 3—Pulse Waveform

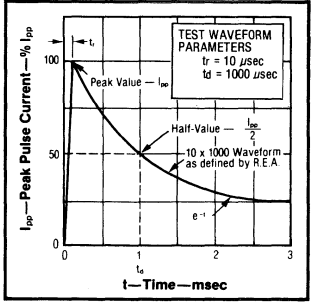
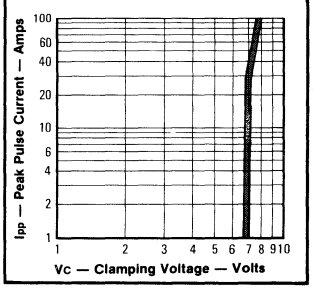


FIG.4—Typical Clamping Voltage (V_C) vs Peak Pulse Current (I_{PP})



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
1N6036 THRU 1N6072A

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 5.5 to 185 volts**
- **MIL qualified per MIL-S-19500/507**
- **Hermetically sealed package**
- **BIDIRECTIONAL**
- **UL Recognized (1N6070A thru 1N6072A)**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25°C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-9} second (theoretical)
- Operating and Storage temperatures: -65° to +175°C
- Steady State power dissipation: 1.0 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package, glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Body marked with Logo and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

APPLICATION

. . .a series of Bidirectional Silicon Transient Suppressors used in AC applications where large voltage transients can permanently damage voltage-sensitive components.

The TransZorb® can be used in applications where induced lightning on rural or remote transmission lines presents a hazard to electronic circuitry (ref: R.E.A. specifications P.E. 60). The response time of TransZorb clamping action is less than (5×10^{-9} sec.); therefore, they can protect Integrated Circuits, MOS devices, Hybrids, and other voltage-sensitive semiconductors and components. These devices have been proven effective EMP Suppressors.

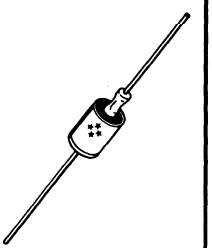
DESCRIPTION

These devices are manufactured using two silicon PN, junction in a back to back configuration. They are characterized by their high surge capability, extremely fast response time, and low impedance, (R_{on}).

The electrical characteristics are specified as peak values, and apply in both directions. For reference to RMS voltages, multiply the TransZorb voltage characteristics by .707 (example: $V_R \times .707 = V_{R(rms)}$) to obtain the equivalent RMS voltage characteristic.

Also available as JAN, JANTX, and JANTXV devices per MIL-S-19500/507.

CASE DO-13



CASE OUTLINE

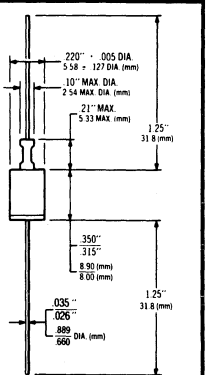


FIGURE 1—Peak Pulse Power vs Pulse Time

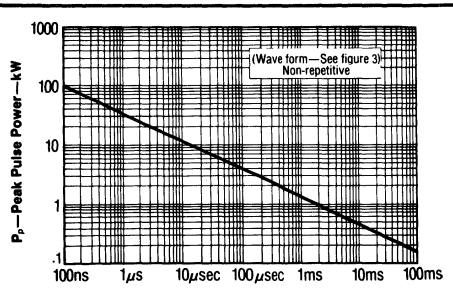
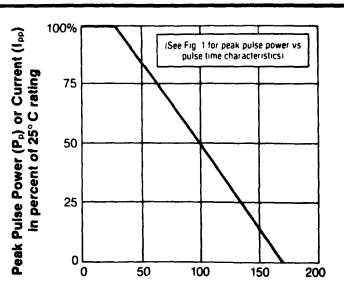


FIGURE 2—Derating Curve



ELECTRICAL CHARACTERISTICS @ 25°C (JEDEC Registered Data)

JEDEC TYPE NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS MIN.	BREAKDOWN VOLTAGE BV VOLTS MAX.	@ I_T mA	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{PP} (FIG. 3) V_C VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{PP} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
1N6036	5.5	6.75	8.25	10	1000	11.7	128	5.0
1N6036A	6.0	7.13	7.88	10	1000	11.3	132	5.0
1N6037	6.5	7.38	9.02	10	500	12.5	120	5.0
1N6037A	7.0	7.79	8.61	10	500	12.1	124	5.0
1N6038	7.0	8.19	10.0	10	200	13.8	109	7.0
1N6038A	7.5	8.65	9.55	10	200	13.4	112	7.0
1N6039	8.0	9.00	11.0	1	50	15.0	100	7.0
1N6039A	8.5	9.5	10.5	1	50	14.5	103	7.0
1N6040	8.5	9.9	12.1	1	10	16.2	93	8.0
1N6040A	9.0	10.5	11.6	1	10	15.6	96	8.0
1N6041	9.0	10.8	13.2	1	5	17.3	87	9.0
1N6041A	10.0	11.4	12.6	1	5	16.7	90	9.0
1N6042	10.0	11.7	14.3	1	5	19.0	79	10
1N6042A	11.0	12.4	13.7	1	5	18.2	82	10
1N6043	11.0	13.5	16.5	1	5	22.0	68	11
1N6043A	12.0	14.3	15.8	1	5	21.2	71	12
1N6044	12.0	14.4	17.6	1	5	23.5	64	12
1N6044A	13.0	15.2	16.8	1	5	22.5	67	13
1N6045	14.0	16.2	19.8	1	5	26.5	56.5	14
1N6045A	15.0	17.1	18.9	1	5	25.2	59.5	15
1N6046	16.0	18.0	22.0	1	5	29.1	51.5	17
1N6046A	17.0	19.0	21.0	1	5	27.7	54	18
1N6047	17.0	19.8	24.2	1	5	31.9	47	19
1N6047A	18.0	20.9	23.1	1	5	30.6	49	20
1N6048	19.0	21.6	26.4	1	5	34.7	43	24
1N6048A	20.0	22.8	25.2	1	5	33.2	45	24
1N6049	21.0	24.3	29.7	1	5	39.1	38.5	27
1N6049A	22.0	25.7	28.4	1	5	37.5	40	28
1N6050	24.0	27.0	33.0	1	5	43.5	34.5	36
1N6050A	25.0	28.5	31.5	1	5	41.4	36	31
1N6051	26.0	29.7	36.3	1	5	47.7	31.5	32
1N6051A	28.0	31.4	34.7	1	5	45.7	33	34
1N6052	29.0	32.4	39.6	1	5	52.0	29	36
1N6052A	30.0	34.2	37.8	1	5	49.9	30	37
1N6053	31.0	35.1	42.9	1	5	56.4	26.5	39
1N6053A	33.0	37.1	41.0	1	5	53.9	28	40
1N6054	34.0	38.7	47.3	1	5	61.9	24	44
1N6054A	36.0	40.9	45.2	1	5	59.3	25.3	43
1N6055	38.0	42.3	51.7	1	5	67.8	22.2	49
1N6055A	40.0	44.7	49.4	1	5	64.8	23.2	47
1N6056	41.0	45.9	56.1	1	5	73.5	20.4	53
1N6056A	43.0	48.5	53.6	1	5	70.1	21.4	51
1N6057	45.0	50.4	61.6	1	5	80.5	18.6	58
1N6057A	47.0	53.2	58.8	1	5	77.0	19.5	56
1N6058	48.0	55.8	68.2	1	5	89.0	16.9	64
1N6058A	53.0	58.9	65.1	1	5	85.0	17.7	62
1N6059	55.0	61.2	74.8	1	5	98.0	15.3	70
1N6059A	58.0	64.6	71.4	1	5	92.0	16.3	68
1N6060	60.0	67.5	82.5	1	5	108.0	13.9	77
1N6060A	64.0	71.3	78.8	1	5	103.0	14.6	75
1N6061	66.0	73.8	90.2	1	5	118.0	12.7	84
1N6061A	70.0	77.9	86.1	1	5	113.0	13.3	82
1N6062	73.0	81.9	100.0	1	5	131.0	11.4	90
1N6062A	75.0	86.5	95.5	1	5	125.0	12.0	86
1N6063	81.0	90.0	110.0	1	5	144.0	10.4	99
1N6063A	82.0	95.0	105.0	1	5	137.0	11.0	94
1N6064	90.0	99.0	121.0	1	5	158.0	9.5	109
1N6064A	94.0	105.0	116.0	1	5	152.0	9.9	104
1N6065	95.0	108.0	132.0	1	5	176.0	8.5	120
1N6065A	100.0	114.0	126.0	1	5	168.0	8.9	115
1N6066	105.0	117.0	143.0	1	5	191.0	7.8	131
1N6066A	110.0	124.0	137.0	1	5	182.0	8.2	125
1N6067	121.0	135.0	165.0	1	5	223.0	6.7	142
1N6067A	128.0	143.0	158.0	1	5	213.0	7.0	136
1N6068	137.0	153.0	187.0	1	5	258.0	5.8	164
1N6068A	145.0	162.0	179.0	1	5	245.0	6.1	157
1N6069	145.0	162.0	198.0	1	5	274.0	5.5	175
1N6069A	150.0	171.0	189.0	1	5	261.0	5.7	167
1N6070	155.0	171.0	210.0	1	5	292.0	5.1	186
1N6070A†	160.0	181.0	200.0	1	5	278.0	5.4	188
1N6071	165.0	180.0	220.0	1	5	308.0	4.9	197
1N6071A†	170.0	190.0	210.0	1	5	294.0	5.1	188
1N6072	175.0	198.0	242.0	1	5	344.0	4.3	219
1N6072A†	185.0	209.0	231.0	1	5	328.0	4.6	209

Available in JAN & JANTX per MIL-S-19500/507A. †UL Listed. TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

TRANSZORB®
BIDIRECTIONAL
1N6036 THRU 1N6072A

FIGURE 3—Pulse Waveform

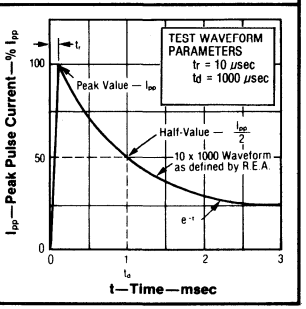
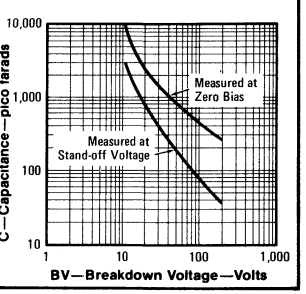


FIGURE 4—Typical Capacitance vs Breakdown Voltage



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25° C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
1N6267 THRU 1N6303A
1.5KE6.8 THRU 1.5KE400A

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Fast Response**
- **Available in ranges from 6.8 to 400 volts**
- **Bidirectional types available**
- **UL Recognized (Ⓤ 1.5KE200CA and 1.5KE220CA)**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25°C
- Operating and storage temperatures: -65° to +175°C
- Forward surge current 200A, 1/120 sec half cycle @ 25°C (Unidirectional only)
- Steady State power dissipation: 5.0 watts at T_L = 75°C, Lead Length = ⅜"
- Repetition Rate (Duty Cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band (unidirectional only)
- Body marked with Logo ✲ and type number

APPLICATION

This series of Silicon Transient Suppressors is used in applications where large voltage transients can permanently damage voltage-sensitive components.

The TransZorb® diode can be used in applications where induced lightning on rural or remote transmission lines presents a hazard to electronic circuitry (ref: R.E.A. specification P.E. 60).

DESCRIPTION

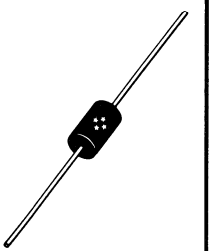
This TransZorb TVS diode has a pulse power rating of 1500 watts for one millisecond. The response time of TransZorb TVS diode clamping action is theoretically instantaneous (1 x 10^{-12} sec); therefore, they can protect integrated circuits, MOS devices, hybrids, and other voltage sensitive semiconductors and components. TransZorb TVS diodes can also be used in series or parallel to increase the peak power ratings.

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual Vc (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

CASE 1



CASE OUTLINE

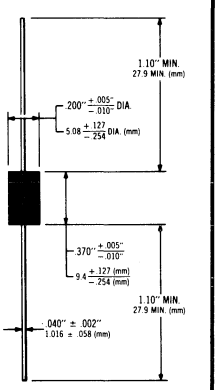


FIGURE 1—Peak Pulse Power vs Pulse Time

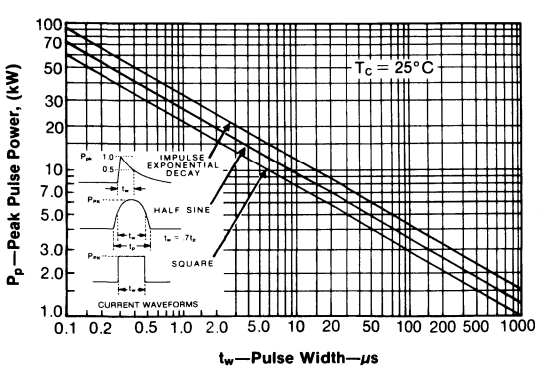
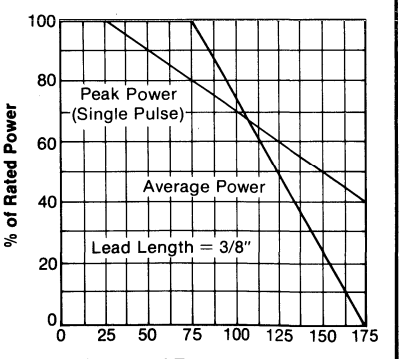


FIGURE 2—Derating Curve



TransZorb® UNIDIRECTIONAL & BIDIRECTIONAL 1N6267 THRU 1N6303A 1.5KE6.8 THRU 1.5KE400A

ELECTRICAL CHARACTERISTICS @ 25°C

JEDEC TYPE NUMBER	GENERAL SEMICONDUCTOR PART NUMBER (NOTE 1)	REVERSE STAND-OFF VOLTAGE (NOTE 2) V_R VOLTS	BREAKDOWN VOLTAGE V_{BR} VOLTS MIN.	BREAKDOWN VOLTAGE V_{BR} VOLTS MAX.	@ IT mA	MAXIMUM REVERSE LEAKAGE @ VR (NOTE 3) IR uA	MAXIMUM CLAMPING VOLTAGE @ Ipp (FIG. 3) VC(MAX) VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) Ipp(MAX) A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV OV(MAX) mV/°C
1N6267	1.5KE6.8*	5.50	6.12 -	7.48	10	1000	10.8	139.0	5.0
1N6267A	1.5KE6.8A*	5.80	6.45 -	7.14	10	1000	10.5	143.0	5.0
1N6268	1.5KE7.5	6.05	6.75 -	8.25	10	500	11.7	128.0	5.0
1N6268A	1.5KE7.5A	6.40	7.13 -	7.88	10	500	11.3	132.0	5.0
1N6269	1.5KE8.2	6.63	7.38 -	9.02	10	200	12.5	120.0	6.0
1N6269A	1.5KE8.2A	7.02	7.79 -	8.61	10	200	12.1	124.0	6.0
1N6270	1.5KE9.1	7.37	8.19 -	10.00	1	50	13.8	109.0	7.0
1N6270A	1.5KE9.1A	7.78	8.65 -	9.55	1	50	13.4	112.0	7.0
1N6271	1.5KE10	8.10	9.00 -	11.00	1	10	15.0	100.0	8.0
1N6271A	1.5KE10A	8.55	9.50 -	10.50	1	10	14.5	103.0	8.0
1N6272	1.5KE11	8.92	9.90 -	12.10	1	5	16.2	93.0	9.0
1N6272A	1.5KE11A	9.40	10.50 -	11.60	1	5	15.6	96.0	9.0
1N6273	1.5KE12	9.72	10.80 -	13.20	1	5	17.3	87.0	10
1N6273A	1.5KE12A	10.20	11.40 -	12.60	1	5	16.7	90.0	10
1N6274	1.5KE13	10.50	11.70 -	14.30	1	5	19.0	79.0	11
1N6274A	1.5KE13A	11.10	12.40 -	13.70	1	5	18.2	82.0	11
1N6275	1.5KE15	12.10	13.50 -	16.50	1	5	22.0	68.0	13
1N6275A	1.5KE15A	12.80	14.30 -	15.80	1	5	21.2	71.0	12
1N6276	1.5KE16	12.90	14.40 -	17.60	1	5	23.5	64.0	16
1N6276A	1.5KE16A	13.60	15.20 -	16.80	1	5	22.5	67.0	14
1N6277	1.5KE18	14.50	16.20 -	19.80	1	5	26.5	56.5	17
1N6277A	1.5KE18A	15.30	17.10 -	18.90	1	5	25.2	59.5	19
1N6278	1.5KE20	16.20	18.00 -	22.00	1	5	29.1	51.5	20
1N6278A	1.5KE20A	17.10	19.00 -	21.00	1	5	27.7	54.0	19
1N6279	1.5KE22	17.80	19.80 -	24.20	1	5	31.9	47.0	21
1N6279A	1.5KE22A	18.80	20.90 -	23.10	1	5	30.6	49.0	20
1N6280	1.5KE24	19.40	21.60 -	26.40	1	5	34.7	43.0	25
1N6280A	1.5KE24A	20.50	22.80 -	25.20	1	5	33.2	45.0	23
1N6281	1.5KE27	21.80	24.30 -	29.70	1	5	39.1	38.5	28
1N6281A	1.5KE27A	23.10	25.70 -	28.40	1	5	37.5	40.0	25
1N6282	1.5KE30	24.30	27.00 -	33.00	1	5	43.5	34.5	31
1N6282A	1.5KE30A	25.60	28.50 -	31.50	1	5	41.4	36.0	28
1N6283	1.5KE33	26.80	29.70 -	36.30	1	5	47.7	31.5	31
1N6283A	1.5KE33A	28.20	31.40 -	34.70	1	5	45.7	33.0	30
1N6284	1.5KE36	29.10	32.40 -	39.60	1	5	52.0	29.0	35
1N6284A	1.5KE36A	30.80	34.20 -	37.80	1	5	49.9	30.0	31
1N6285	1.5KE39	31.60	35.10 -	42.90	1	5	56.4	26.5	39
1N6285A	1.5KE39A	33.30	37.10 -	41.00	1	5	53.9	28.0	36
1N6286	1.5KE43	34.80	38.70 -	47.30	1	5	61.9	24.0	46
1N6286A	1.5KE43A	36.80	40.90 -	45.20	1	5	59.3	25.3	44
1N6287	1.5KE47	38.10	42.30 -	51.70	1	5	67.8	22.2	50
1N6287A	1.5KE47A	40.20	44.70 -	49.40	1	5	64.8	23.2	48
1N6288	1.5KE51	41.30	45.90 -	56.10	1	5	73.5	20.4	55
1N6288A	1.5KE51A	43.60	48.50 -	53.60	1	5	70.1	21.4	51
1N6289	1.5KE56	45.60	50.40 -	61.60	1	5	80.5	18.6	58
1N6289A	1.5KE56A	47.80	53.20 -	58.80	1	5	77.0	19.5	56
1N6290	1.5KE62	50.20	55.80 -	68.20	1	5	89.0	16.9	65
1N6290A	1.5KE62A	53.00	58.90 -	65.10	1	5	85.0	17.7	62
1N6291	1.5KE68	55.10	61.20 -	74.80	1	5	98.0	15.3	71
1N6291A	1.5KE68A	58.10	64.60 -	71.40	1	5	92.0	16.3	69
1N6292	1.5KE75	60.70	67.50 -	82.50	1	5	108.0	13.9	80
1N6292A	1.5KE75A	64.10	71.30 -	78.80	1	5	103.0	14.6	76
1N6293	1.5KE82	66.40	73.80 -	90.20	1	5	118.0	12.7	90
1N6293A	1.5KE82A	70.10	77.90 -	86.10	1	5	113.0	13.3	86
1N6294	1.5KE91	73.70	81.90 -	100.00	1	5	131.0	11.4	99
1N6294A	1.5KE91A	77.80	86.50 -	95.50	1	5	125.0	12.0	94
1N6295	1.5KE100	81.00	90.00 -	110.00	1	5	144.0	10.4	109
1N6295A	1.5KE100A	85.50	95.00 -	105.00	1	5	137.0	11.0	104
1N6296	1.5KE110	89.20	99.00 -	121.00	1	5	158.0	9.5	120
1N6296A	1.5KE110A	94.00	105.00 -	116.00	1	5	152.0	9.9	115
1N6297	1.5KE120	97.20	108.00 -	132.00	1	5	173.0	8.7	131
1N6297A	1.5KE120A	102.00	114.00 -	126.00	1	5	165.0	9.1	125
1N6298	1.5KE130	105.00	117.00 -	143.00	1	5	187.0	8.0	142
1N6298A	1.5KE130A	111.00	124.00 -	137.00	1	5	179.0	8.4	136
1N6299	1.5KE150	121.00	135.00 -	165.00	1	5	215.0	7.0	164
1N6299A	1.5KE150A	128.00	143.00 -	158.00	1	5	207.0	7.2	157
1N6300	1.5KE160	130.00	144.00 -	176.00	1	5	230.0	6.5	175
1N6300A	1.5KE160A	136.00	152.00 -	168.00	1	5	219.0	6.8	167
1N6301	1.5KE170	138.00	153.00 -	187.00	1	5	244.0	6.2	186
1N6301A	1.5KE170A	145.00	162.00 -	179.00	1	5	234.0	6.4	188
1N6302	1.5KE180	146.00	162.00 -	198.00	1	5	258.0	5.8	197
1N6302A	1.5KE180A	154.00	171.00 -	189.00	1	5	246.0	6.1	188
1N6303	1.5KE200	162.00	180.00 -	220.00	1	5	287.0	5.2	219
1N6303A	†1.5KE200A	171.00	190.00 -	210.00	1	5	274.0	5.5	209
	1.5KE220	175.00	198.00 -	242.00	1	5	344.0	4.3	240
	†1.5KE220A	185.00	209.00 -	231.00	1	5	328.0	4.6	230
	1.5KE250	202.00	225.00 -	275.00	1	5	360.0	5.0	270
	1.5KE250A	214.00	237.00 -	263.00	1	5	344.0	5.0	260
	1.5KE300	243.00	270.00 -	330.00	1	5	430.0	5.0	330
	1.5KE300A	256.00	285.00 -	315.00	1	5	414.0	5.0	315
	1.5KE350	284.00	315.00 -	385.00	1	5	504.0	4.0	385
	1.5KE350A	300.00	332.00 -	368.00	1	5	482.0	4.0	368
	1.5KE400	324.00	360.00 -	440.00	1	5	574.0	4.0	440
	1.5KE400A	342.00	380.00 -	420.00	1	5	548.0	4.0	420

†UL Listed 1.5KE200CA and 1.5KE220CA. *Not available as bidirectional

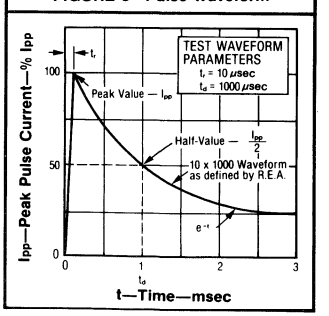
ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 2)
- V_{BR} Breakdown Voltage.
- $V_{C(max)}$ Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb suppressor when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltage is the sum of a voltage rise due to diode series resistance and an increase in breakdown voltage caused by the junction temperature rise.
- I_{pp} Peak Pulse Current—See Figure 3.
- P_P Peak Pulse Power.
- I_R Reverse Leakage.
- ΔV_C Rise in voltage above the breakdown voltage caused by current flow.

NOTES

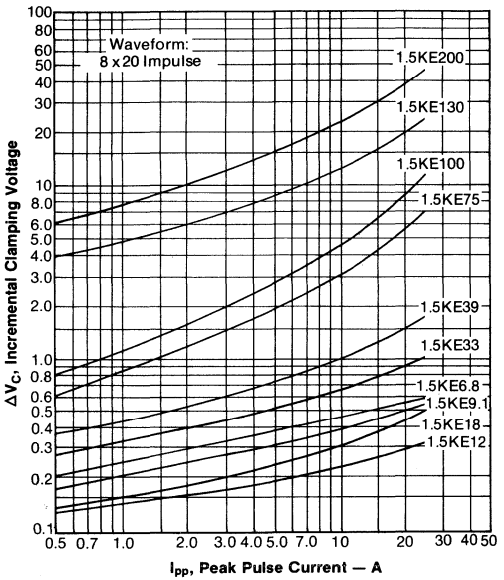
1. Part numbers shown are for unidirectional diodes. Add C or CA suffix to specify bidirectional suppressors. (General Semiconductor parts ONLY—1N62XX parts not available as bidirectional.) General Semi. 1.5KE6.8 is available as unidirectional only.
2. A TransZorb suppressor is normally selected according to the reverse "Stand-Off Voltage" (V_R) which should be slightly greater than the maximum dc or continuous peak operating voltage level.
3. For bidirectional types having V_R or 10 volts and under, the I_R limit is doubled.
4. For unidirectional diodes $V_{F(max)} = 3.5V$ at I_F = 100A, 1/2 sine wave of 8.33ms pulse width.

FIGURE 3—Pulse Waveform



CLAMPING VOLTAGE 8 x 20 IMPULSE
$\Delta V_C = V_C - V_{BR}$

FIGURE 4—Unidirectional



CLAMPING VOLTAGE 10 x 1000 IMPULSE
$\Delta V_C = V_C - V_{BR}$

FIGURE 5—Unidirectional

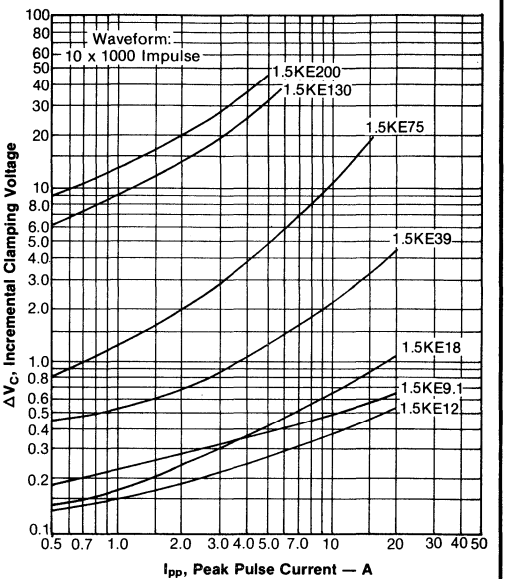


FIGURE 6—Bidirectional

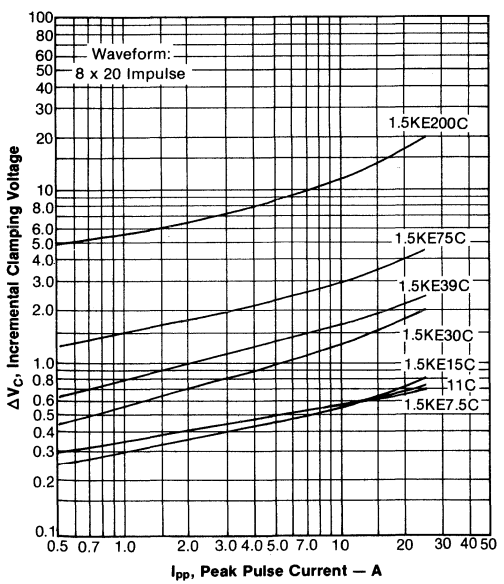
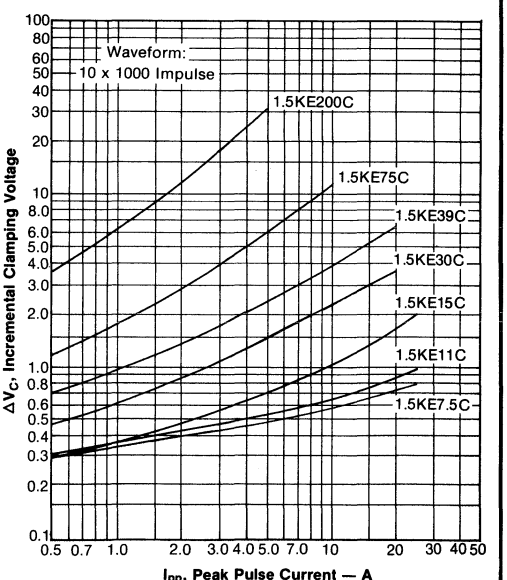


FIGURE 7—Bidirectional



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 8—Capacitance

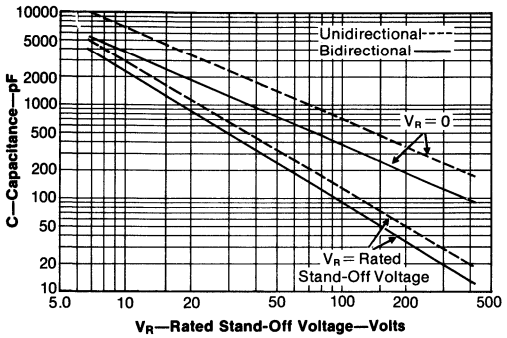


FIGURE 9—Forward Voltage

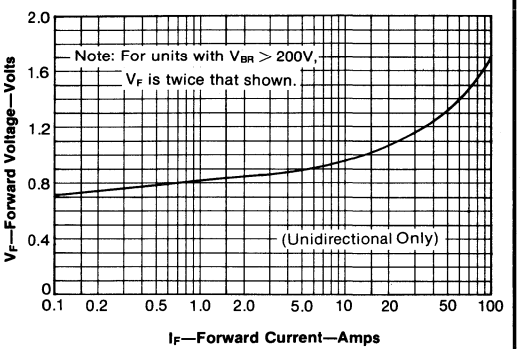


FIGURE 10—Model Parameters

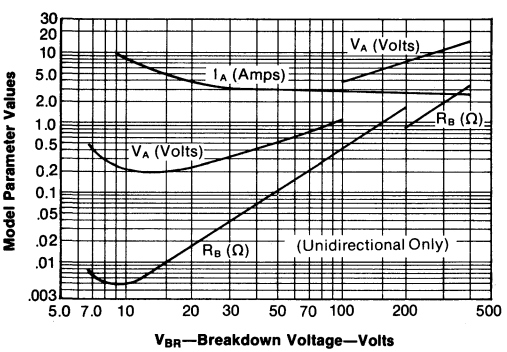


FIGURE 11
Breakdown Voltage Temperature Coefficient

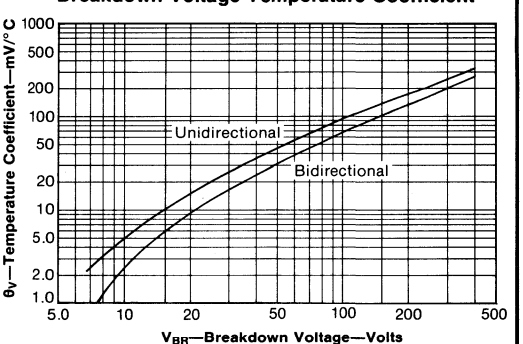
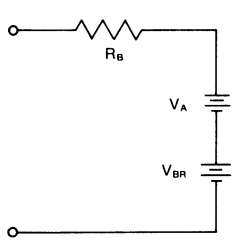


FIGURE 12—High Current Model



Over a restricted current range, TransZorb® diodes may be modeled as shown in the adjoining figure. The battery V_{BR} represents the breakdown voltage, the battery V_A represents the effect of avalanche resistance, and the resistance R_B represents the bulk silicon resistance. At a critical current I_A, the incremental avalanche resistance, which is inversely proportional to current, becomes negligible; its net effect is represented by the battery V_A. The voltage at currents above I_O is obtained by adding a term $R_B \times I_{pp}$ to the sum of the battery voltages. Values for the model parameters are shown on Figure 10. The model is not valid for bidirectional suppressors.

The major effect of temperature is upon the breakdown voltage, V_{BR}. It is adjusted by adding a term Θ_V (T_J - 25° C). Values for Θ_V are shown in Figure 11; T_J is calculated using standard techniques.

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS

1N6356 THRU 1N6372	ICT-5 THRU ICT-45C

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 5.0 to 45 volts**
- **Transient protection for CMOS, MOS and BIPOLAR MICROPROCESSORS**
- **Low clamping factor**
- **Hermetically sealed package**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Unipolar, Less than 1×10^{-12} second; Bidirectional, Less than 5×10^{-9} second
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 200amps, 1/120 second at 25° C
  (Applies to Unipolar or single direction only)
- Steady State power dissipation: 1.0 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package, glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band (except Bidirectional types)
- Body marked with Logo ⁂ and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

APPLICATION

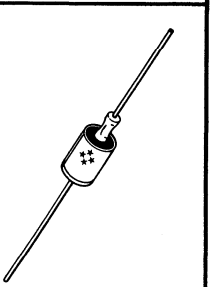
. . .a premium series of transient voltage suppressors specifically designed and tested to protect Bipolar, MOS and Schottky improved integrated circuits from electrical disturbances. Transients and noise pulses are generated by electromechanical switching, electro magnetic coupling, capacitive or inductive load switching, voltage reversals, and electrostatic discharge.

DESCRIPTION

The TransZorb is desired over a crowbar circuit, a LC or RC network and a catch or clamping diode because of: fewer components; speed of response; high power or energy absorption and low clamping factor.

Providing protection for the most popular IC voltage levels, these devices are available for either unidirectional or bidirectional applications. These units are hermetically sealed — capable of meeting the screening specifications of military requirements.

CASE DO-13



CASE OUTLINE

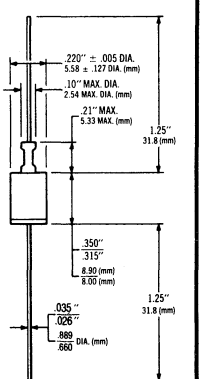


FIGURE 1—Peak Pulse Power vs Pulse Time

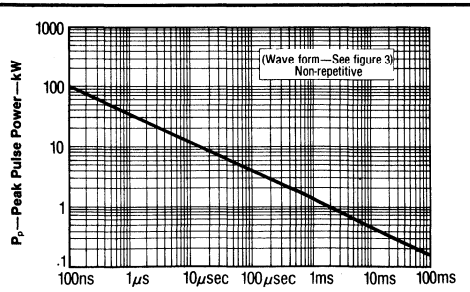
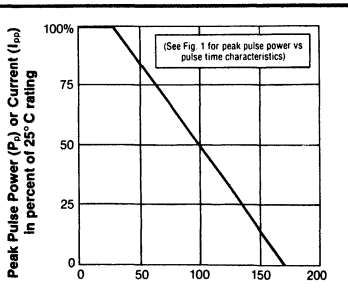


FIGURE 2—Derating Curve



TRANSZORB®
UNIDIRECTIONAL & BIDIRECTIONAL

1N6356 THRU 1N6372 — ICT-5 THRU ICT-45C

ELECTRICAL CHARACTERISTICS @ 25°C (JEDEC Registered Data)

JEDEC TYPE NUMBER	GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	MINIMUM** BREAKDOWN VOLTAGE @ 1mA BV(min) VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @I_{pp1} = 1A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE @I_{pp2} = 10A V_C VOLTS	MAXIMUM PEAK PULSE CURRENT I_{pp3} A
1N6356	ICT-5*	5.0	6.0	300	7.1	7.5	160
1N6357	ICT-8	8.0	9.4	25	11.3	11.5	100
1N6358	ICT-10	10.0	11.7	2	13.7	14.1	90
1N6359	ICT-12	12.0	14.1	2	16.1	16.5	70
1N6360	ICT-15	15.0	17.6	2	20.1	20.6	60
1N6361	ICT-18	18.0	21.2	2	24.2	25.2	50
1N6362	ICT-22	22.0	25.9	2	29.8	32.0	40
1N6363	ICT-36	36.0	42.4	2	50.6	54.3	23
1N6364	ICT-45	45.0	52.9	2	63.3	70.0	19

V_f at 100 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

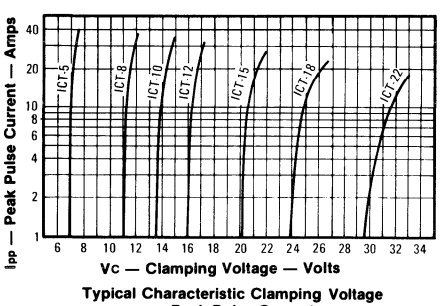
ELECTRICAL CHARACTERISTICS @ 25°C (Test Both Polarities)

1N6365	ICT-8C	8.0	9.4	50	11.4	11.6	100
1N6366	ICT-10C	10.0	11.7	2	14.1	14.5	90
1N6367	ICT-12C	12.0	14.1	2	16.7	17.1	70
1N6368	ICT-15C	15.0	17.6	2	20.8	21.4	60
1N6369	ICT-18C	18.0	21.2	2	24.8	25.5	50
1N6370	ICT-22C	22.0	25.9	2	30.8	32.0	40
1N6371	ICT-36C	36.0	42.4	2	50.6	54.3	23
1N6372	ICT-45C	45.0	52.9	2	63.3	70.0	19

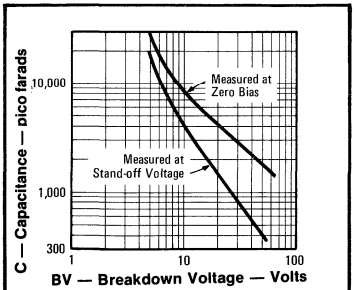
C Suffix indicates Bipolar

*ICT-5 not available as Bipolar.

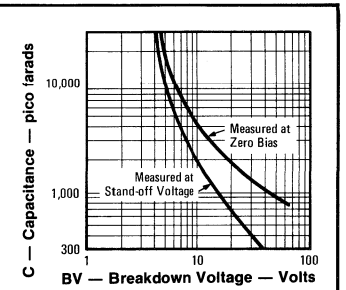
**The minimum breakdown voltage as shown takes into consideration the ±1 volt tolerance normally specified for power supply regulation on most integrated circuit manufacturers data sheets. Similar TransZorb devices are available with reduced clamping voltages where tighter regulated power supply voltages are employed.



Typical Characteristic Clamping Voltage vs Peak Pulse Current

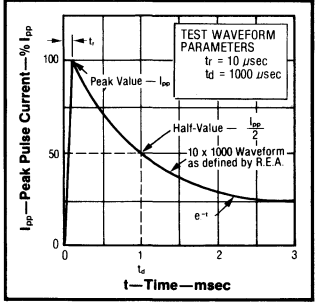


Typical Capacitance vs Breakdown Voltage (Unidirectional Types)



Typical Capacitance vs Breakdown Voltage (Bidirectional Types)

FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction *does not occur prior* to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS

1N6373 THRU 1N6389
ICTE-5 THRU ICTE-45C

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 5.0 to 45 volts**
- **Transient protection for CMOS, MOS and BIPOLAR MICROPROCESSORS**
- **Low clamping factor**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Unipolar, Less than 1×10^{-12} second; Bidirectional, Less than 5×10^{-9} second
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 200amps, 1/120 second at 25° C
  (Applies to Unipolar or single direction only)
- Steady State power dissipation: 5.0W at T_L = 75° C, Lead Length = 3/8"
- Repetition rate (duty cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band (except Bidirectional types)
- Body marked with Logo and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.33 at full rated power
1.20 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

APPLICATION

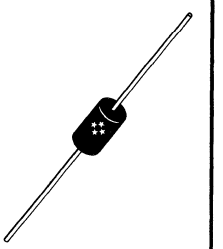
. . .a premium series of transient voltage suppressors specifically designed and tested to protect Bipolar, MOS and Schottky improved integrated circuits from electrical disturbances. Transients and noise pulses are generated by electromechanical switching, electromagnetic coupling, capacitive or inductive load switching, voltage reversals, and electrostatic discharge.

DESCRIPTION

The TransZorb is desired over a crowbar circuit, a LC or RC network and a catch or clamping diode, because of: fewer components; speed of response; high power or energy absorption and low clamping factor.

Providing protection for the most popular IC voltage levels, these devices are available for either unidirectional or bidirectional applications. These devices are designed to dissipate 1500 watts of peak pulse power for 1 millisecond.

CASE 1



CASE OUTLINE

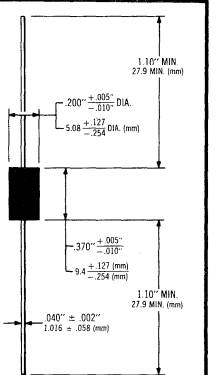


FIGURE 1—Peak Pulse Power vs Pulse Time

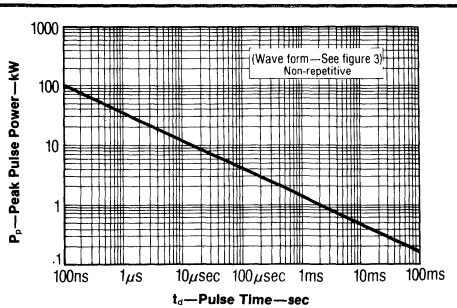
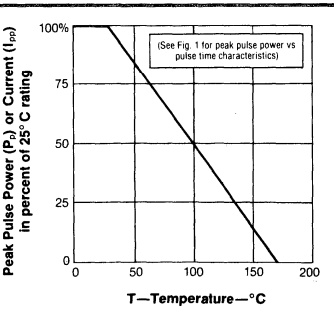


FIGURE 2—Derating Curve



TRANSZORB® UNIDIRECTIONAL & BIDIRECTIONAL

1N6373 THRU 1N6389 — ICTE-5 THRU ICTE-45C

ELECTRICAL CHARACTERISTICS @ 25°C (JEDEC Registered Data)

JEDEC TYPE NUMBER	GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	MINIMUM** BREAKDOWN VOLTAGE @ 1mA BV(min) VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @I_{pp1} = 1A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE @I_{pp2} = 10A V_C VOLTS	MAXIMUM PEAK PULSE CURRENT I_{pp3} A
1N6373	ICTE-5*	5.0	6.0	300	7.1	7.5	160
1N6374	ICTE-8	8.0	9.4	25	11.3	11.5	100
1N6375	ICTE-10	10.0	11.7	2	13.7	14.1	90
1N6376	ICTE-12	12.0	14.1	2	16.1	16.5	70
1N6377	ICTE-15	15.0	17.6	2	20.1	20.6	60
1N6378	ICTE-18	18.0	21.2	2	24.2	25.2	50
1N6379	ICTE-22	22.0	25.9	2	29.8	32.0	40
1N6380	ICTE-36	36.0	42.4	2	50.6	54.3	23
1N6381	ICTE-45	45.0	52.9	2	63.3	70.0	19

V_f at 100 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

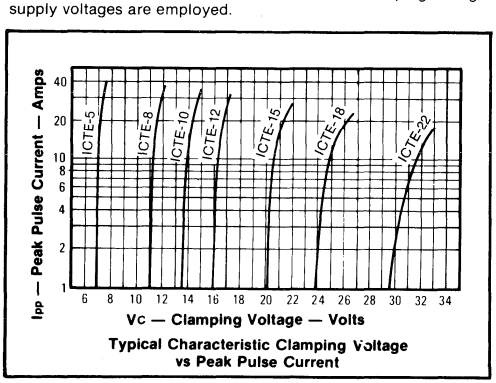
ELECTRICAL CHARACTERISTICS @ 25°C (Test Both Polarities)

1N6382	ICTE-8C	8.0	9.4	50	11.4	11.6	100
1N6383	ICTE-10C	10.0	11.7	2	14.1	14.5	90
1N6384	ICTE-12C	12.0	14.1	2	16.7	17.1	70
1N6385	ICTE-15C	15.0	17.6	2	20.8	21.4	60
1N6386	ICTE-18C	18.0	21.2	2	24.8	25.5	50
1N6387	ICTE-22C	22.0	25.9	2	30.8	32.0	40
1N6388	ICTE-36C	36.0	42.4	2	50.6	54.3	23
1N6389	ICTE-45C	45.0	52.9	2	63.3	70.0	19

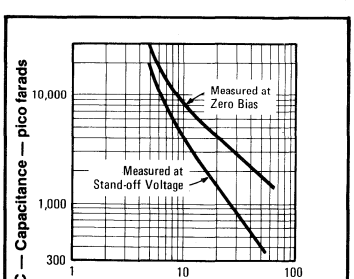
C Suffix indicates Bipolar

*ICTE-5 not available as Bipolar.

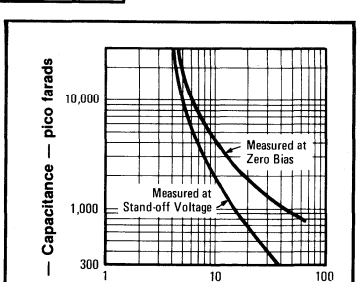
**The minimum breakdown voltage as shown takes into consideration the ±1 volt tolerance normally specified for power supply regulation on most integrated circuit manufacturers data sheets. Similar TransZorb devices are available with reduced clamping voltages where tighter regulated power supply voltages are employed.



Typical Characteristic Clamping Voltage vs Peak Pulse Current



Typical Capacitance vs Breakdown Voltage (Unidirectional Types)



Typical Capacitance vs Breakdown Voltage (Bidirectional Types)

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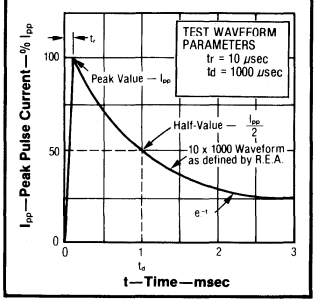
FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
5KP5.0 THRU 5KP110A

FEATURES

- **5000 watts Peak Pulse Power dissipation**
- **Available in ranges from 5.0 to 110 volts**
- **Designed for DC power supply applications**
- **Each device 100% tested**

MAXIMUM RATINGS

- 5,000 watts of Peak Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1 x 10^{-12} second (theoretical)
- Operating and Storage temperatures: -55° to + 175° C
- Steady State power dissipation: 8.0 watt at T_L = 75° C, Lead Length = ⅜"
- Repetition rate (duty cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded (Plastic) Case
- Weight: 4 grams (approximate)
- Positive terminal marked with band
- Body marked with Logo ⁂ and type number

APPLICATION

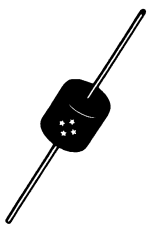
. . .a series of high power transient voltage suppressors designed to be used on the output of switching power supplies. These devices may be used to replace crowbar circuits. Both the 5 and 10 percent voltage tolerances are referenced to the power supply output voltage level.

DESCRIPTION

The 5KP is designed to withstand a higher level of peak current while allowing a circuit breaker to trip or a fuse blow before shorting. This will enable the user to reset the breaker or replace the fuse and continue operation. For this type operation, it is recommended that a sufficient mounting surface be used for dissipating the heat generated by the TransZorb during the transient or over-voltage condition.

TransZorbs are Silicon PN Junction **devices designed for absorption of** high voltage transients associated with power disturbances, switching and induced lighting effects. This series is available from 5.0 volts thru 110 volts.

CASE 31



CASE OUTLINE

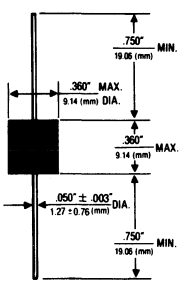


FIGURE 1—Peak Pulse Power vs Pulse Time

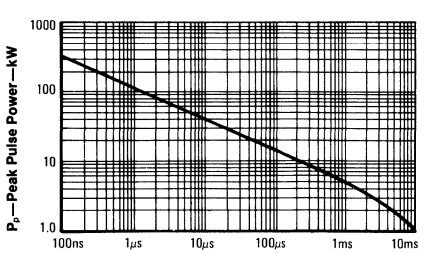
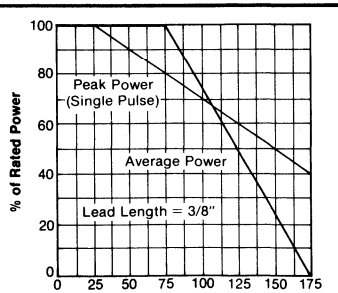


FIGURE 2—Derating Curve



TransZorb® UNIDIRECTIONAL 5KP5.0 THRU 5KP110A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS MIN.	@ IT mA	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{pp} [FIG. 3] V_C VOLTS	MAXIMUM PEAK PULSE CURRENT [FIG. 3] I_{pp} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
5KP5.0	5.0	6.40	50	2000	9.6	520	4.0
5KP5.0A	5.0	6.40	50	2000	9.2	543	4.0
5KP6.0	6.0	6.67	50	5000	11.4	439	4.0
5KP6.0A	6.0	6.67	50	5000	10.3	485	4.0
5KP6.5	6.5	7.22	50	2000	12.3	407	4.0
5KP6.5A	6.5	7.22	50	2000	11.2	447	4.0
5KP7.0	7.0	7.78	50	1000	13.3	378	5.0
5KP7.0A	7.0	7.78	50	1000	12.0	417	5.0
5KP7.5	7.5	8.33	5	250	14.3	350	6.0
5KP7.5A	7.5	8.33	5	250	12.9	388	6.0
5KP8.0	8.0	8.89	5	150	15.0	333	6.0
5KP8.0A	8.0	8.89	5	150	13.6	367	6.0
5KP8.5	8.5	9.44	5	50	15.9	314	7.0
5KP8.5A	8.5	9.44	5	50	14.4	347	7.0
5KP9.0	9.0	10.0	5	20	16.9	295	8.0
5KP9.0A	9.0	10.0	5	20	15.4	325	8.0
5KP10	10	11.1	5	15	18.8	266	9.0
5KP10A	10	11.1	5	15	17.0	294	9.0
5KP11	11	12.2	5	10	20.1	249	10
5KP11A	11	12.2	5	10	18.2	274	10
5KP12	12	13.3	5	10	22.0	227	11
5KP12A	12	13.3	5	10	19.9	251	11
5KP13	13	14.4	5	10	23.8	210	12
5KP13A	13	14.4	5	10	21.5	232	12
5KP14	14	15.6	5	10	25.8	194	13
5KP14A	14	15.6	5	10	23.2	215	13
5KP15	15	16.7	5	10	26.9	188	15
5KP15A	15	16.7	5	10	24.4	206	15
5KP16	16	17.8	5	10	28.8	176	18
5KP16A	16	17.8	5	10	26.0	192	16
5KP17	17	18.9	5	10	30.5	164	19
5KP17A	17	18.9	5	10	27.6	181	18
5KP18	18	20.0	5	10	32.2	155	20
5KP18A	18	20.0	5	10	29.2	172	19
5KP20	20	22.2	5	10	35.8	139	24
5KP20A	20	22.2	5	10	32.4	154	22
5KP22	22	24.4	5	10	39.4	127	27
5KP22A	22	24.4	5	10	35.5	141	24
5KP24	24	26.7	5	10	43.0	116	30
5KP24A	24	26.7	5	10	38.9	128	27
5KP26	26	28.9	5	10	46.6	107	33
5KP26A	26	28.9	5	10	42.1	119	29
5KP28	28	31.1	5	10	50.1	99	34
5KP28A	28	31.1	5	10	45.5	110	30
5KP30	30	33.3	5	10	53.5	93	38
5KP30A	30	33.3	5	10	48.4	103	35
5KP33	33	36.7	5	10	59.0	85	41
5KP33A	33	36.7	5	10	53.3	94	38
5KP36	36	40.0	5	10	64.3	78	45
5KP36A	36	40.0	5	10	58.1	86	40
5KP40	40	44.4	5	10	71.4	70	50
5KP40A	40	44.4	5	10	64.5	78	45
5KP43	43	47.8	5	10	76.7	65	54
5KP43A	43	47.8	5	10	69.4	72	49
5KP45	45	50.0	5	10	80.3	62	57
5KP45A	45	50.0	5	10	72.7	69	51
5KP48	48	53.3	5	10	85.5	58	62
5KP48A	48	53.3	5	10	77.4	65	55
5KP51	51	56.7	5	10	91.1	55	65
5KP51A	51	56.7	5	10	82.4	61	60
5KP54	54	60.0	5	10	96.3	52	70
5KP54A	54	60.0	5	10	87.1	57	64
5KP58	58	64.4	5	10	103.0	49	77
5KP58A	58	64.4	5	10	93.6	53	69
5KP60	60	66.7	5	10	107.0	47	79
5KP60A	60	66.7	5	10	96.8	52	70
5KP64	64	71.1	5	10	114.0	44	85
5KP64A	64	71.1	5	10	103.0	49	75
5KP70	70	77.8	5	10	125	40	93
5KP70A	70	77.8	5	10	113	44	84
5KP75	75	83.3	5	10	134	37	100
5KP75A	75	83.3	5	10	121	41	90
5KP78	78	86.7	5	10	139	36	104
5KP78A	78	86.7	5	10	126	40	94
5KP85	85	94.4	5	10	151	33	113
5KP85A	85	94.4	5	10	137	36	102
5KP90	90	100	5	10	160	31	120
5KP90A	90	100	5	10	146	34	109
5KP100	100	111	5	10	179	28	134
5KP100A	100	111	5	10	162	31	122
5KP110	110	122	5	10	196	26	147
5KP110A	110	122	5	10	177	28	132

V_f at 100 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

FIGURE 3—Pulse Waveform

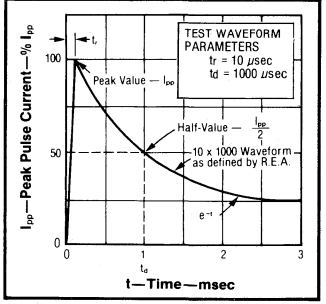
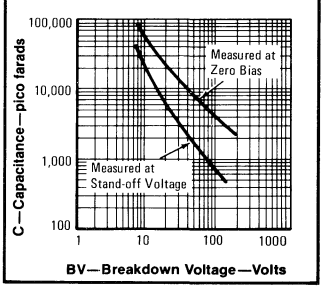


FIGURE 4—Typical Capacitance vs Breakdown Voltage



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- I_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS 15KP17 THRU 15KP280A

FEATURES

- **15,000 watts Peak Pulse Power dissipation**
- **Available in ranges from 17 to 280 volts**
- **Easy mounting to printed circuit board**
- **Each device 100% tested**

MAXIMUM RATINGS

- 15,000 watts of Peak Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1 x 10^{-12} second (theoretical)
- Operating and Storage temperatures: -55° to + 150° C
- Steady State power dissipation: 5.0 watts at T_A=25°C, Lead Length=3/8"
- Repetition rate (duty cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded (Plastic) Case
- Weight: 13 grams (approximate)
- Positive terminal marked with dot
- Body marked with Logo and type number

APPLICATION

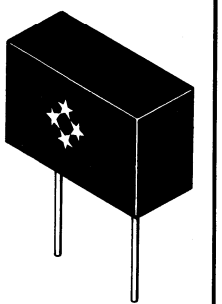
. . .a series of high power, medium voltage TransZorbs®, Transient Voltage Suppressors, designed for the protection of Precision Industrial Electronic Equipment.

TransZorbs are Silicon PN Junction devices designed for absorbtion of high voltage transients associated with power disturbances, switching, and induced lightning effects.

DESCRIPTION

These devices are rated for a peak pulse power of 15,000 watts for 1 millisecond. This series is available from 17 volts through 280 volts. Special voltages are available from the factory. For extended power handling capability on a circuit board, the 15KP offers the user a 15,000 watt device. In the case of extended or long duration power surge, it is recommended to use this series product. It is required to have a large metalized land surface for heat dissipation for long duration transients.

CASE 24



CASE OUTLINE

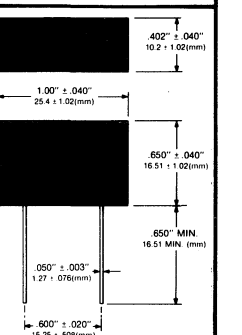


FIGURE 1—Peak Pulse Power vs Pulse Time

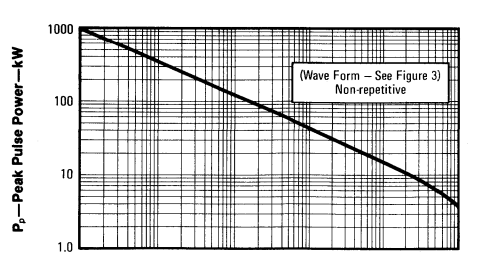
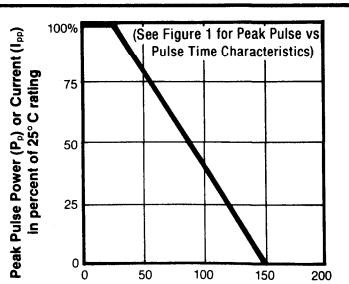


FIGURE 2—Derating Curve



TRANSZORB® UNIDIRECTIONAL 15KP17 THRU 15KP280A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE [NOTE 1] V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS MIN.	@ IT mA	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{pp} [FIG. 3] V_C VOLTS	MAXIMUM PEAK PULSE CURRENT [FIG. 3] I_{pp} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
15KP17	17	18.9	50	5000	32.3	464	19
15KP17A	17	18.9	50	5000	29.3	512	17
15KP18	18	20.0	50	5000	34.2	439	20
15KP18A	18	20.0	50	5000	30.9	485	18
15KP20	20	22.2	20	1500	37.9	396	24
15KP20A	20	22.2	20	1500	34.3	437	21
15KP22	22	24.4	10	500	41.1	365	27
15KP22A	22	24.4	10	500	37.1	404	24
15KP24	24	26.7	5	150	45.0	333	30
15KP24A	24	26.7	5	150	40.7	369	27
15KP26	26	28.9	5	50	48.7	308	32
15KP26A	26	28.9	5	50	44.0	341	29
15KP28	28	31.1	5	25	52.4	286	35
15KP28A	28	31.1	5	25	47.5	316	31
15KP30	30	33.3	5	15	56.2	267	27
15KP30A	30	33.3	5	15	50.7	296	34
15KP33	33	36.7	5	10	60.6	248	42
15KP33A	33	36.7	5	10	54.8	274	38
15KP36	36	40.0	5	10	66.0	227	46
15KP36A	36	40.0	5	10	59.7	251	41
15KP40	40	44.4	5	10	72.8	206	51
15KP40A	40	44.4	5	10	65.8	228	46
15KP43	43	47.8	5	10	77.1	195	55
15KP43A	43	47.8	5	10	69.7	215	50
15KP45	45	50.0	5	10	80.7	186	57
15KP45A	45	50.0	5	10	73.0	205	52
15KP48	48	53.3	5	10	85.9	175	62
15KP48A	48	53.3	5	10	77.7	193	56
15KP51	51	56.7	5	10	91.5	164	66
15KP51A	51	56.7	5	10	82.8	181	60
15KP54	54	60.0	5	10	96.8	155	70
15KP54A	54	60.0	5	10	87.5	171	63
15KP58	58	64.4	5	10	104.0	144	76
15KP58A	58	64.4	5	10	94.0	160	68
15KP60	60	66.7	5	10	107.0	140	78
15KP60A	60	66.7	5	10	97.3	154	71
15KP64	64	71.1	5	10	115	130	84
15KP64A	64	71.1	5	10	104	144	76
15KP70	70	77.8	5	10	126	119	92
15KP70A	70	77.8	5	10	114	132	83
15KP75	75	83.3	5	10	135	111	100
15KP75A	75	83.3	5	10	122	123	89
15KP78	78	86.7	5	10	140	107	104
15KP78A	78	86.7	5	10	126	119	93
15KP85	85	94.4	5	10	152	99	113
15KP85A	85	94.4	5	10	137	109	102
15KP90	90	100.0	5	10	160	94	120
15KP90A	90	100.0	5	10	146	103	109
15KP100	100	111	5	10	179	84	134
15KP100A	100	111	5	10	162	93	121
15KP110	110	122	5	10	196	77	147
15KP110A	110	122	5	10	178	84	133
15KP120	120	133	5	10	214	70	161
15KP120A	120	133	5	10	193	78	145
15KP130	130	144	5	10	231	65	174
15KP130A	130	144	5	10	209	72	157
15KP150	150	167	5	10	268	56	202
15KP150A	150	167	5	10	243	62	183
15KP160	160	178	5	10	287	52	216
15KP160A	160	178	5	10	259	58	195
15KP170	170	189	5	10	304	49	229
15KP170A	170	189	5	10	275	55	207
15KP180	180	200	5	10	321	47	242
15KP180A	180	200	5	10	291	52	219
15KP200	200	222	5	10	356	42	269
15KP200A	200	222	5	10	322	47	243
15KP220	220	245	5	10	393	38	297
15KP220A	220	245	5	10	356	42	269
15KP240	240	267	5	10	428	35	324
15KP240A	240	267	5	10	388	39	293
15KP260	260	289	5	10	464	32	352
15KP260A	260	289	5	10	419	36	317
15KP280	280	311	5	10	500	30	378
15KP280A	280	311	5	10	452	33	342

V_f at 200 amps peak, 1/2 sine wave = 7.5 volts maximum.

FIGURE 3—Pulse Waveform

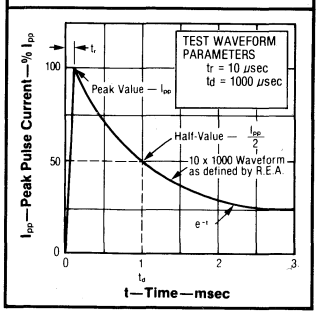
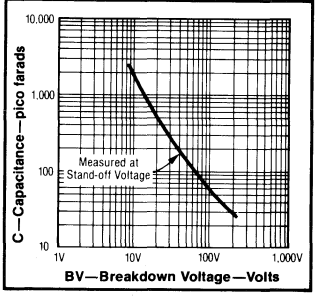


FIGURE 4—Typical Capacitance vs Breakdown Voltage



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
BIDIRECTIONAL
60KS200C
90KS200C

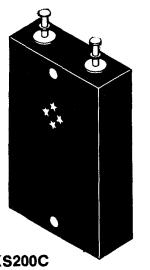
FEATURES

- **60,000 watts Peak Pulse Power & 90,000 watts Peak Pulse Power**
- **200 volts BIDIRECTIONAL**
- **Exceeds MIL-STD-1399 requirements**
- **Each Device 100% Tested**

APPLICATION

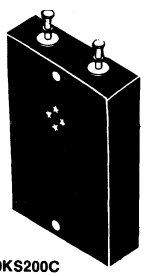
. . .a Bidirectional Silicon Transient Suppressor for use in shipboard equipment and other power servicing equipment where large voltage transients endanger voltage sensitive components.

CASE 22



60KS200C

CASE 32



90KS200C

MAXIMUM RATINGS

- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-8} second (theoretical)
- Operating and Storage temperatures: -65° to +150°C
- Steady State power dissipation: 10 watts

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 50 grams (approximate)
- Body marked with Logo ⁂ and type number

DESCRIPTION

This device was designed with DOD-STD-1399, Section 300 (formerly MIL-STD-1399), Interface Standard for Shipboard Systems, Electrical Power, Alternating Current, as the controlling specification. It has been proven reliable for the protection against power interruptions and shore power switch-over. The TransZorb meets all applicable environmental requirements of MIL-E-16400. The individual submodules can be selected for higher voltage applications as well as increased power capability. The subcomponents can also be tested or screened for military requirements prior to encapsulation into the complete module. The screening would consist of 100% TX level environmental testing per MIL-S-19500/507A (Para. 4.3). For ordering these options, use the following suffix:

H1 — Submodule Screening,
H2 — Submodule and Module Screening,
H3 — Submodule and Module Screening. Module Group B & C lot testing. See Appendix for Processing Test Plan.

ABBREVIATIONS & SYMBOLS

V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)

BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a 40 millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} Peak Pulse Current — See Figure 3

P_p Peak Pulse Power

I_R Reverse Leakage

FIGURE 1—Peak Pulse Power vs Pulse Time

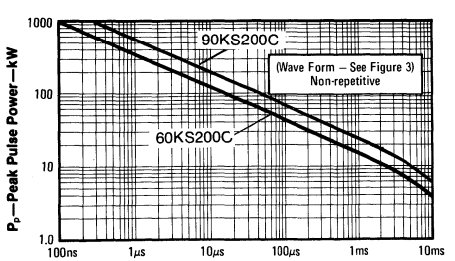
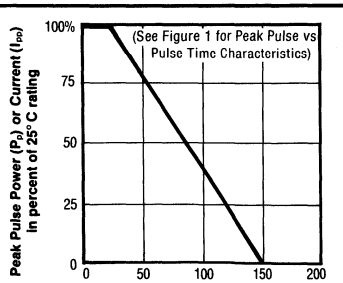


FIGURE 2—Derating Curve



TRANSZORB®

BIDIRECTIONAL
60KS200C
90KS200C

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE @ 1mA BV VOLTS MIN.	BREAKDOWN VOLTAGE @ 1mA BV VOLTS MAX.	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{PP} (FIG. 3) V_C VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{PP} A
60KS200C*	180	200	225	10	335	180
90KS200C*	180	200	225	0.5	280	180

*Other voltages available upon request. Consult factory.

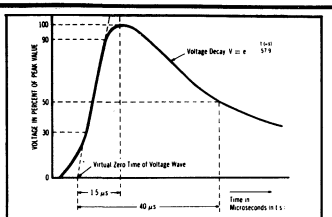


FIGURE 5— Spike Voltage (Short Time Transient) Wave Shape

MIL-STD-1399, Section 103 does not define or specify source impedance of the transient wave form depicted in Fig. 1, Page 10 (see GSI Figure 5). However, Naval Ship Engineering Center has as of 25 Nov. 1975 issued guidelines which are meaningful in determining the transient source impedance.

. . . a computer study had been made of shipboard electrical systems and an average of the data calculated was:

R = 3.5 ohms resistance of system under transient conditions

X_L = 10 ohms @ 167 KHz – reactance of system under transient conditions

$Freq_u$ = 165 KHz to 250 KHz – The slope of the voltage wave at these frequencies is approximately the same as the leading edge of the spike voltage wave in MIL-STD-1399 Sec 103 Fig. 1 on Page 10

V = 2500 volts – spike voltage amplitude

Additional calculations were made concerning the surge or characteristic impedance of the system.

Z_O = 16Ω to 26Ω

General Semiconductor has subjected the 60KS200C TransZorb to pulses generated by a special transient simulator (schematic shown in Figure 5). Figure 7 is the current pulse wave form monitored at point A and Figure 8 is the voltage for the device under test monitored at point C.

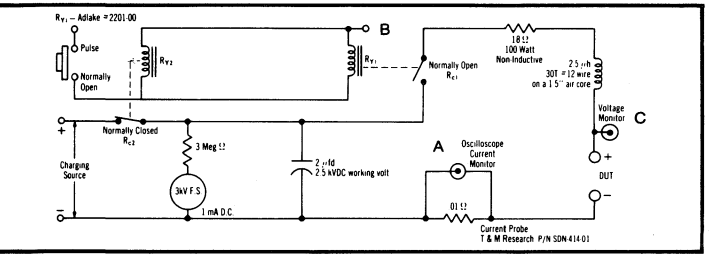


FIGURE 6—Test Circuit

FIGURE 7—
Current Pulse Wave Form
Vertical: 50A/cm
Horizontal: 20 μsec/cm

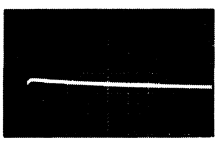


FIGURE 8—
Voltage Pulse Wave Form With TransZorb Under Test
Vertical: 100V/cm
Horizontal: 20 μsec/cm

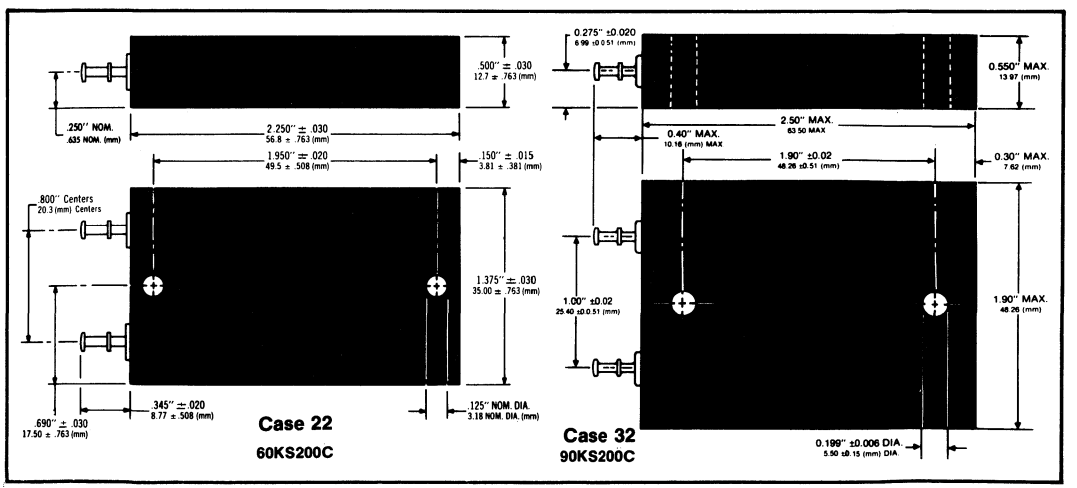
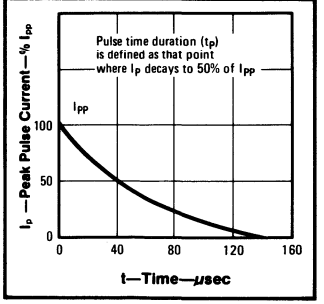


FIGURE 3—Pulse Waveform (1.5 x 40 usec)



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
704-15K36
AND
704-15K36T

FEATURES

- **15,000 watts Peak Pulse Power dissipation**
- **28 volt power supply protection**
- **Can be supplied with TX screening**
- **Each device 100% tested**

MAXIMUM RATINGS

- Peak Pulse power dissipation at 25° C: 15,000 watts at 1 msec.
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} second (theoretical)
- Operating and Storage temperatures: −65° to +150° C
- Forward surge rating: half cycle 300amps, 1/120 second at 25° C
- Steady State power dissipation: 10 watts
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Molded Case
- Polarity: Positive terminal indicated
- Weight: 704-14K36 — 38 grams
  704-15K36T — 65 grams
- Body marked with Logo and type number

APPLICATION

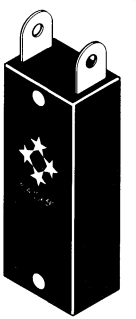
. . .a series of Silicon Transient Suppressors for use primarily in Airborne Equipment where large voltage transients endanger voltage-sensitive components. The TransZorb® meets all applicable environmental requirements of MIL-S-19500. The 704-15K36 is designed for high current, short peak pulse transients applications. Where as the 704-15K36T is designed for extended peak pulse transients greater than 1 millisecond.

DESCRIPTION

These devices were designed with MIL-STD-704 (Characteristics and Utilization of Aircraft Electric Power) as the controlling specification. These 15kW assemblies are designed typically to operate with a minimum source impedance of .25 ohms for transients. Although designed for 28 volt aircraft requirements, the 704-15K36 and 36T voltage levels can be special-ordered for specific applications. These deviations are given a special house part number for identification. Subcomponents can be screened for military requirements. The screening would consist of 100% TX level environmental testing per MIL-S-19500/507A (Para. 4.3). For ordering these options, use the following suffix:

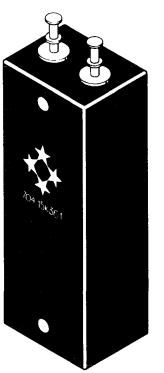
H1 — Submodule Screening,
H2 — Submodule and Module Screening,
H3 — Submodule and Module Screening. Module Group B & C lot testing. See Appendix for Processing Test Plan.

CASE 2



704-15K36

CASE 3



704 15K36T

FIGURE 1—Peak Pulse Power vs Pulse Time

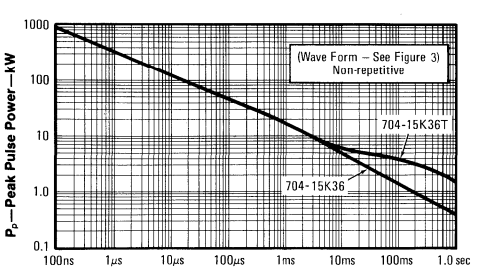
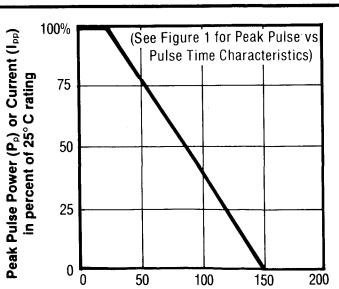


FIGURE 2—Derating Curve

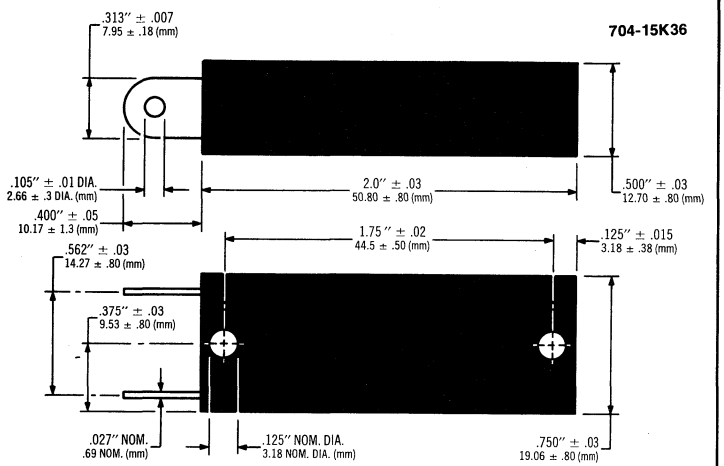


TRANSZORB® UNIDIRECTIONAL 704-15K36 AND 704-15K36T

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE [NOTE 1] V_R VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 10 mA BV VOLTS	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{PP} [FIG. 3] V_C VOLTS	MAXIMUM PEAK PULSE CURRENT [FIG. 3] I_{PP} A	MAXIMUM FORWARD VOLTAGE V_F @ ~ 8.3 msec. 100A VOLTS DC
704-15K36	31.5	36	100	51	300	3.0
704-15K36T	31.5	36	500	51	300	15.0

CASE OUTLINE — CASE 2



CASE OUTLINE — CASE 3

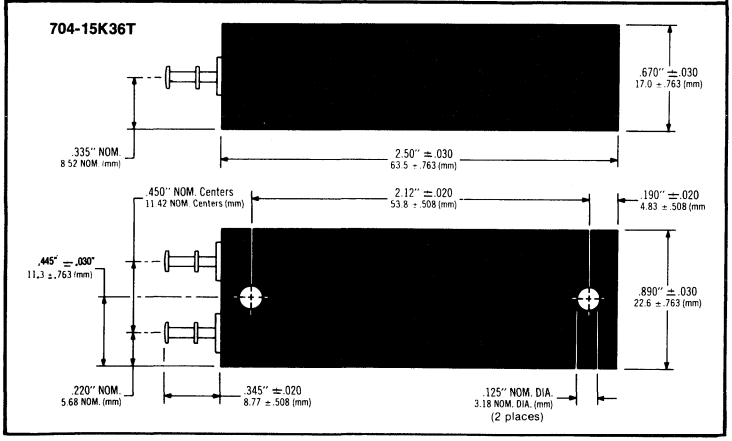
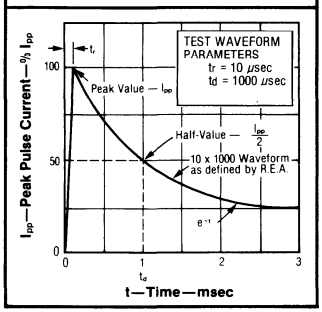


FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{PP} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

NEW

DIODE ARRAY
TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSOR
8 PIN
UNIDIRECTIONAL & BIDIRECTIONAL
5.0 THRU 24 VOLTS

FEATURES

- **500 watt peak pulse power**
- **Data and Bus Line Applications**
- **Unidirectional & Bidirectional Capabilities**
- **Standard Dual-in-Line Package**
- **Common Ground Configuration**

DESCRIPTION

This family of arrays uses the proven TransZorb® TVS technology to provide transient voltage suppression at low clamping voltages for sensitive data lines. They are also ideal for the protection of board level standard TTL and MOS power bus lines.

These arrays can be used to protect combinations of 4 or 6 unidirectional or bidirectional lines (see reverse side).

CASE

Standard 8 pin Plastic DIP

ABBREVIATIONS & SYMBOLS

V_D **Stand Off Voltage:** Applied Reverse Voltage to assure a nonconductive condition. (See Note.)

V_C **Maximum Clamping Voltage:** The maximum peak voltage appearing across the TransZorb TVS when subjected to the peak pulse current waveform of 8 by 20µs. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{PP} **Peak Pulse Current**

P_P **Peak Pulse Power**

I_D **Reverse Leakage**

NOTE: A TransZorb TVS is normally selected according to the Reverse Stand Off Voltage (V_D) which should be equal to or greater than the dc or continuous peak operating voltage level.

MECHANICAL CHARACTERISTICS

- Molded 8 pin DIP
- Terminals: Solder dipped
- Body marked with type code and logo
- Pin no. 1 marked with dot on top of package
- Pin nos. 1 and 8 common grounds (notched end)

MAXIMUM RATINGS

- Peak Pulse Power (8/20µs): 500 watts
- Operating and StorageTemperature Range: -55°C to +150°C
- Forward Surge Rating unidirectional only: 10 amps (1/120 sec @ 25°C)
- Repetition Rate (duty cycle): .01%

FIGURE 1 -- Peak Pulse Power vs Pulse Time

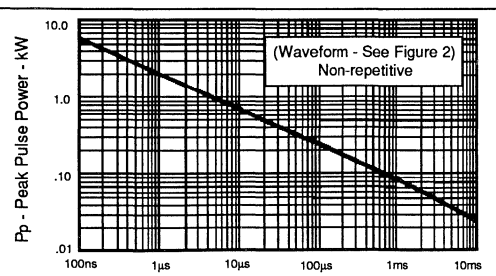
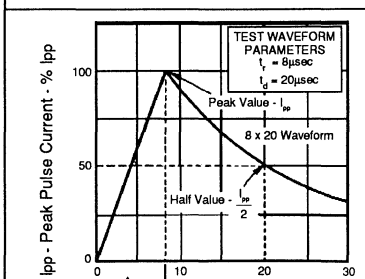


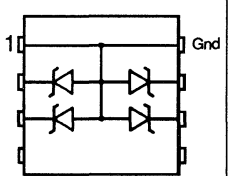
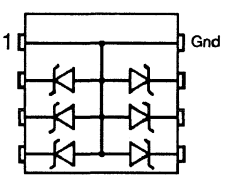
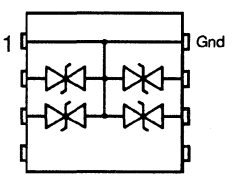
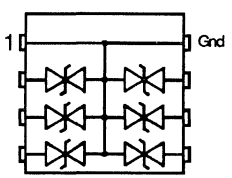
FIGURE 2 -- Pulse Waveform



ELECTRICAL CHARACTERISTICS @ 25°C

GSI PART NUMBER	UNIDIRECTIONAL STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @1mA	LEAKAGE CURRENT @ V_D	MAXIMUM CLAMPING VOLTAGE @10A (See Figure 2)	CAPACITANCE @ OV, 1MHz	BIDIRECTIONAL STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @1mA	LEAKAGE CURRENT @ V_D	MAXIMUM CLAMPING VOLTAGE @10A (See Figure 2)	CAPACITANCE @ OV, 1MHz
	V_D Volts	B_V Volts	I_D µA	V_C Volts	C pF	V_D Volts	B_V Volts	I_D µA	V_C Volts	C pF
See matrix below	5	6.0	200	12.5	880	5	6.0	400	12.5	500
	12	13.3	2	26.0	440	12	13.3	4	26.0	385
	15	16.7	2	33.0	400	15	16.7	4	33.0	300
	24	26.7	2	52.1	275	24	26.7	4	52.1	200

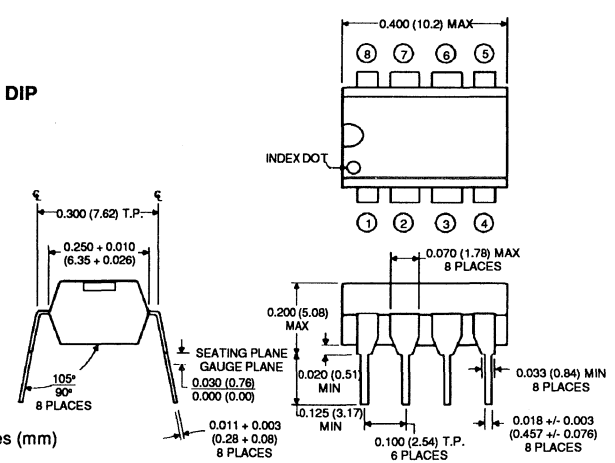
GSI TYPE NUMBER MATRIX AND CIRCUIT DIAGRAM

UNIDIRECTIONAL 4 Line Array	UNIDIRECTIONAL 6 Line Array	BIDIRECTIONAL 4 Line Array	BIDIRECTIONAL 6 Line Array
DA05L DA12L DA15L DA24L	DA05M DA12M DA15M DA24M	DA05CL DA12CL DA15CL DA24CL	DA05CM DA12CM DA15CM DA24CM
			

NOTE: Use DA05 for 5V Stand-Off Voltage, DA12 for 12V Stand-Off Voltage, etc.

CASE OUTLINE

8 pin plastic DIP



Measurements in inches (mm)

General Semiconductor Industries, Inc.

NEW

DIODE ARRAY
TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSOR
16 PIN
UNIDIRECTIONAL & BIDIRECTIONAL
5.0 THRU 24 VOLTS

FEATURES

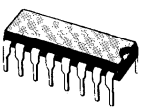
- **500 watt peak pulse power**
- **Data and Bus Line Applications**
- **Unidirectional & Bidirectional Capabilities**
- **Standard Dual-in-Line Package**
- **Common Ground Configuration**

DESCRIPTION

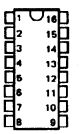
This family of arrays uses the proven TransZorb® TVS technology to provide transient voltage suppression at low clamping voltages for sensitive data lines. They are also ideal for the protection of board level standard TTL and MOS power bus lines.

These arrays can be used to protect combinations of 8 or 12 unidirectional or bidirectional lines (see reverse side).

CASE



Standard 16 pin Plastic DIP



ABBREVIATIONS & SYMBOLS

V_D **Stand Off Voltage:** Applied Reverse Voltage to assure a nonconductive condition. (See Note.)

V_c **Maximum Clamping Voltage:** The maximum peak voltage appearing across the TransZorb TVS when subjected to the peak pulse current waveform of 8 by 20µs. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} **Peak Pulse Current**

P_P **Peak Pulse Power**

I_D **Reverse Leakage**

NOTE: A TransZorb TVS is normally selected according to the Reverse Stand Off Voltage (V_D) which should be equal to or greater than the dc or continuous peak operating voltage level.

MECHANICAL CHARACTERISTICS

- Molded 16 pin DIP
- Terminals: Solder dipped
- Body marked with type code and logo
- Pin No. 1 marked with dot on top of package
- Pin Nos. 1, 8, 9 and 16 common grounds

MAXIMUM RATINGS

- Peak Pulse Power (8/20µs): 500 watts
- Operating and StorageTemperature Range: -55°C to +150°C
- Forward Surge Rating (unidirectional only): 10 amps (1/120 sec @ 25°C)
- Repetition Rate (duty cycle): .01%

FIGURE 1 -- Peak Pulse Power vs. Pulse Time

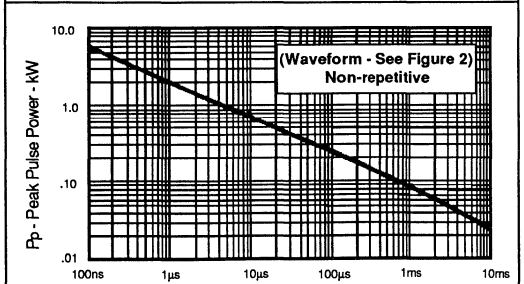
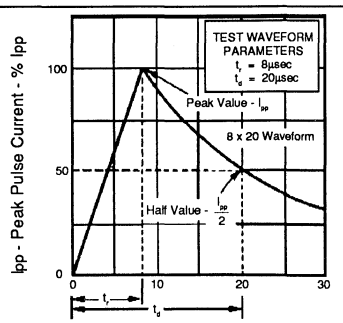


FIGURE 2 -- Pulse Waveform

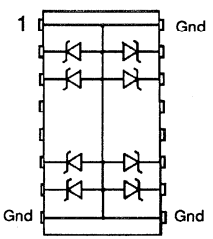
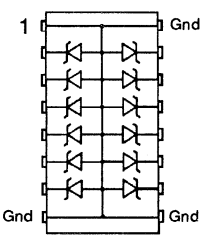
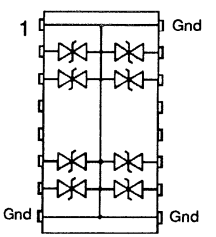
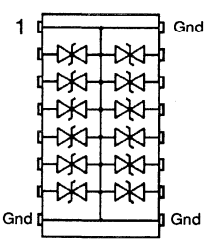


ELECTRICAL CHARACTERISTICS @ 25°C

GSI PART NUMBER	UNIDIRECTIONAL STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @ 1mA	LEAKAGE CURRENT @ V_D	MAXIMUM CLAMPING VOLTAGE @ 10A (See Figure 2)	CAPACITANCE @ 0V, 1MHz	BIDIRECTIONAL STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @ 1mA	LEAKAGE CURRENT @ V_D	MAXIMUM CLAMPING VOLTAGE @ 10A (See Figure 2)	CAPACITANCE @ 0V, 1MHz
	V_D Volts	B_V Volts	I_D µA	V_C Volts	C pF	V_D Volts	B_V Volts	I_D µA	V_C Volts	C pF
See matrix below	5	6.0	200	12.5	880	5	6.0	400	12.5	500
	12	13.3	2	26.0	440	12	13.3	4	26.0	385
	15	16.7	2	33.0	400	15	16.7	4	33.0	300
	24	26.7	2	52.1	275	24	26.7	4	52.1	200

GSI reserves the right to change electrical or mechanical characteristics as specified herein.

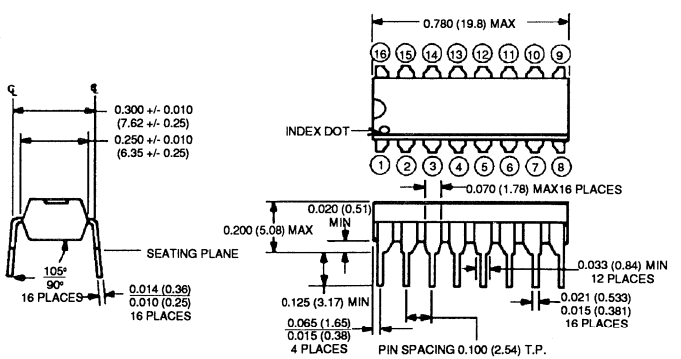
GSI TYPE NUMBER MATRIX AND CIRCUIT DIAGRAM

UNIDIRECTIONAL 8 Line Array	UNIDIRECTIONAL 12 Line Array	BIDIRECTIONAL 8 Line Array	BIDIRECTIONAL 12 Line Array
DA05N DA12N DA15N DA24N	DA05P DA12P DA15P DA24P	DA05CN DA12CN DA15CN DA24CN	DA05CP DA12CP DA15CP DA24CP
			

NOTE: Use DA05 for 5V Stand-Off Voltage, DA12 for 12V Stand-Off Voltage, etc.

CASE OUTLINE

16 pin plastic DIP



Measurements in inches

General Semiconductor Industries, Inc.

DLZ-5 THRU 30 SERIES
DATA LINE ZORB® TRANSZORB® FAMILY

FEATURES

- **Multiple TransZorb® TVS Array**
- **Unidirectional or Bidirectional**
- **Military Environment Capability**
- **Dual-In-Line, 16 pin Hermetic Package**
- **Available with high reliability processing per MIL-S-19500**
- **μP/mP Compatible Package**
- **Low Capacitance**
- **Voltage range of 5V to 100V available**
- **Common Bus Configuration**

MAXIMUM RATINGS

- 500 Watts Peak Pulse Power/Position (@25° C) (8 x 20μs)
- $t_{clamping}$ (0 volts to BV min.) Less than 1×10^{-12} seconds (theoretical) (unipolar); 5×10^{-9} seconds (bi-polar) (theoretical)
- Operating and Storage Temperatures: -55° C to +150° C
- Forward Surge Rating: 10 Amps, 1/120 sec. @ 25° C (uni-polar)
- Rep Rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Ceramic, 16 pin Dual-in-Line Case (.300" row spacing)
- Weight: 3.5 grams (approximate)
- Pin No. 1 marked with flag on lead and dot on top of package. Body marked with Logo and type Number

DESCRIPTION

The TransZorb TVS family of devices is packaged in a dual-in-line, ceramic, hermetically sealed package. Developed specifically for *military environments*, these components offer *15 protective devices; unidirectional and bidirectional,* common bus connections, per package. The dual-in-line design allows *compatible* packaging for microprocessors, memories, and controllers and is designed specifically for *data line protection*, at the PC board level, TTL and MOS voltages are available for protection of input/output data circuits.

DLZ series TransZorb TVS arrays are available with MIL processing to JANTX equivalent levels per MIL-S-19500. Specify DLZ part number with suffix "-H1" for 100% TX-level screening, and suffix "-H2" for 100% screening with Group B processing. See Appendix B for MIL processing.

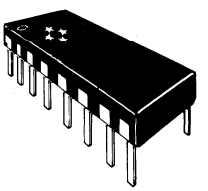
BENEFITS

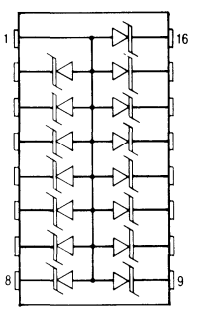
- Saves Space
- Saves Production Time
- Military Compatibility
- Ease of Design
- Protection for Data Lines
- EMP/ESD Protection
- Satisfies Military NEMP requirements
- Protection of I/O Devices

DEVICE TYPES AVAILABLE

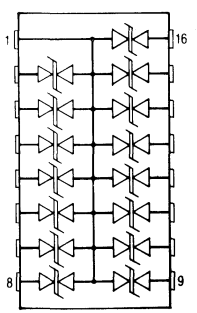
UNIDIRECTIONAL	BIDIRECTIONAL
DLZ-5, A	DLZ-8C, CA
DLZ-12, A	DLZ-13C, CA
DLZ-17, A	DLZ-19C, CA
DLZ-24, A	DLZ-30C, CA
DLZ-30, A	

CASE 29





Typical Uni-polar Schematic



Typical Bi-polar Schematic

FIGURE 1 — Peak Pulse Power vs Pulse Time (per position)

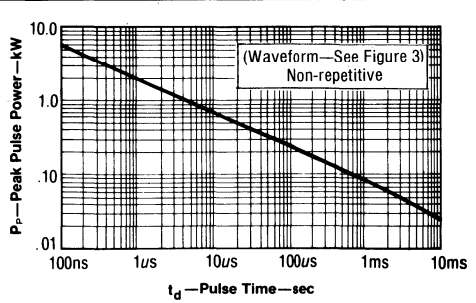
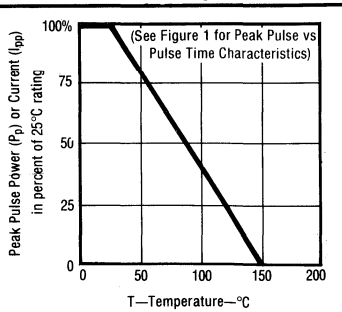


FIGURE 2 — Derating Curve

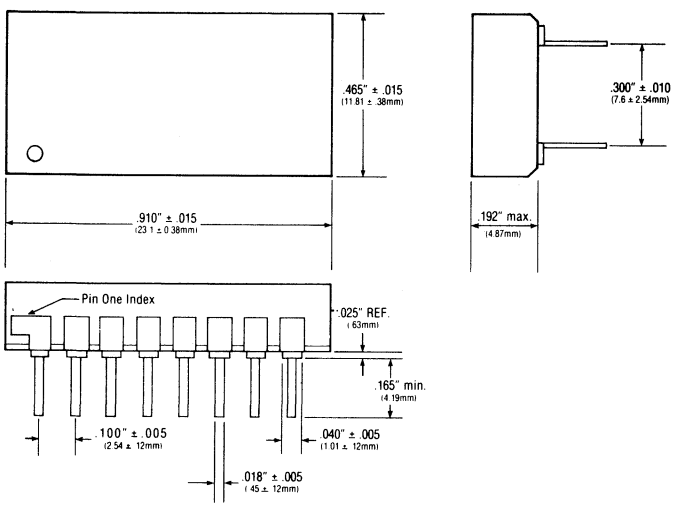


ELECTRICAL CHARACTERISTICS @ 25°C AMBIENT

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE VR VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1ma BV (min) VOLTS	MAXIMUM CLAMPING VOLTAGE @ Ipp1 1A (8 x 20μsec) VC1 VOLTS	MAXIMUM CLAMPING VOLTAGE @ Ipp2 10A (8 x 20μsec) VC2 VOLTS	MAXIMUM REVERSE LEAKAGE @ VR IR μA	MAXIMUM CAPACITANCE @ 0V, 1MHz C pF	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV MV/°C
UNI-POLAR							
DLZ-5	5	6.0	10.2	12.5	200	880	5
DLZ-5A	5	6.0	9.5	10.6	200	880	5
DLZ-12	12	13.3	21.1	26.0	2	440	18
DLZ-12A	12	13.3	19.1	23.5	2	440	18
DLZ-17	17	19.2	30.4	37.4	2	330	20
DLZ-17A	17	19.2	27.5	33.9	2	330	20
DLZ-24	24	26.7	42.3	52.1	2	275	31
DLZ-24A	24	26.7	38.3	47.2	2	275	31
DLZ-30	30	33.3	52.8	65.0	2	220	39
DLZ-30A	30	33.3	47.8	58.8	2	220	39
BI-POLAR							
DLZ-8C	8	8.5	13.4	16.6	10	440	9
DLZ-8CA	8	8.5	12.2	15.0	10	440	9
DLZ-13C	13	14.4	22.8	28.1	4	385	18
DLZ-13CA	13	14.4	20.6	25.4	4	385	18
DLZ-19C	19	21.6	34.2	42.1	4	275	24
DLZ-19CA	19	21.6	31.0	38.1	4	275	24
DLZ-30C	30	33.3	52.8	65.0	4	165	39
DLZ-30CA	30	33.3	47.8	58.8	4	165	39

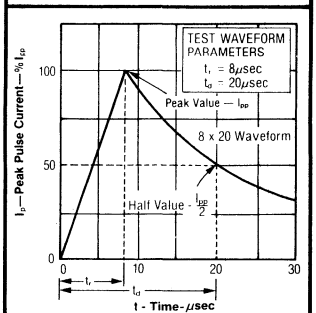
"A", "CA" suffix denotes selected clamping voltage.

CASE OUTLINE — CASE 29



DLZ-5 THRU 30 SERIES
DATA LINE ZORB®
UNIDIRECTIONAL & BIDIRECTIONAL

FIGURE 3 — Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)

BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} Peak Pulse Current — See Figure 3

I_p Peak Pulse Power

I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
GMP-5 SERIES

FEATURES

- **500 watts Peak Pulse Power dissipation**
- **Low voltage transient suppressor**
- **Static Memory, CMOS, MOS, transient protection**
- **Each device 100% tested**

MAXIMUM RATINGS

- 500 watts of Peak Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1 x 10^{-12} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 100 amps, 1/120 second at 25° C
- Steady State power dissipation: 5.0W at $T_L = 75°C$, Lead Length = 3/8"
- Repetition rate (duty cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band
- Body marked with Logo and type number

APPLICATION

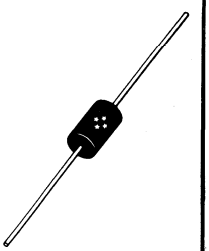
The GMP-5 series is a premium 500 watt transient voltage suppressor designed for low voltage protection of MOS memories. Because of the low clamping factor, they provide a high degree of protection to VMOS, HMOS, NMOS, and CMOS circuits susceptible to 5-volt line transients. The TransZorb is desired over a crowbar circuit which can be false triggered and must be turned off to reset.

DESCRIPTION

TransZorbs are characterized by their high surge capability, extremely fast response time and low on resistance. They are effective in providing protection against pulses generated by electromechanical switching, electromagnetic coupling, capacitive or inductive load switching, voltage reversals and electrostatic discharge. MOS circuits are more prone to damage from these pulses.

External system disturbances, such as electrostatic discharges, result in transient voltages exceeding 20,000 volts. TransZorbs having a low-series resistance(R_{on})will effectively shunt out unwanted transients while maintaining the circuit level for continuous system operation.

CASE 7



CASE OUTLINE

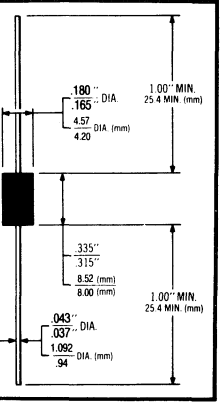


FIGURE 1—Peak Pulse Power vs Pulse Time

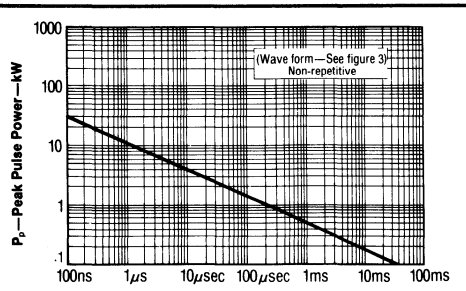
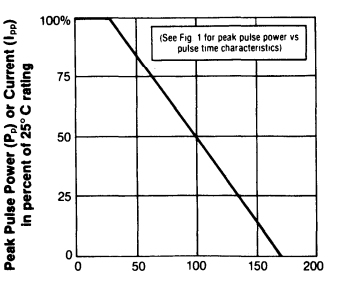


FIGURE 2—Derating Curve



TRANSZORB® UNIDIRECTIONAL GMP-5 SERIES

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	MAXIMUM REVERSE LEAKAGE @V_R I_R μA	MINIMUM BREAKDOWN VOLTAGE @ 1mA BV(min) VOLTS	MAXIMUM CLAMPING VOLTAGE @I_{pp1} = 1A (FIG. 3) V_{C1} VOLTS	MAXIMUM CLAMPING VOLTAGE @I_{pp2} = 10A (FIG. 3) V_{C2} VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{pp3} A	MAXIMUM PEAK PULSE CURRENT (1.2 x 50μsec) A
GMP-5	5.0	300	5.3	6.7	6.9	70	215
GMP-5A	5.0	100	5.5	6.7	6.9	70	215
GMP-5B	5.0	300	5.3	6.4	6.6	70	215

V_f at 50 amps peak, 8.3 msec sine wave = 3.5 volts maximum.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

FIGURE 3—Pulse Waveform

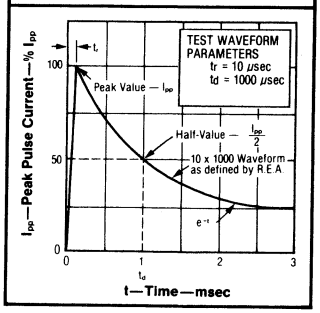
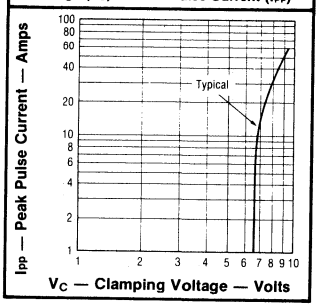


FIGURE 4—Typical Characteristic Clamping Voltage (V_C) vs Peak Pulse Current (I_{PP})



General Semiconductor Industries, Inc.

TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS

LOW CAPACITANCE

LC6.5 THRU LC90A

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 6.5 to 90**
- **Low capacitance ac signal protection**
- **Hermetically sealed package**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 5×10^{-9} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Steady State power dissipation: 1.0 watt
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Standard DO-13 package, glass and metal hermetically sealed
- Weight: 1.5 grams (approximate)
- Polarity band on cathode end of the TransZorb (positive potential applied)
- Body marked with Logo ⁂ and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.40 at full rated power
1.30 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

Note: When pulse testing, test in TransZorb Avalanche direction. DO NOT pulse in forward direction.

APPLICATION

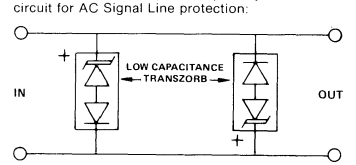
This specification sheet defines a series of low-capacitance silicon transient suppressors for the protection of ac signal line. This series employs a standard TransZorb® in series with a rectifier with the same transient capabilities as the TransZorb. The rectifier is also used to reduce the effective capacitance up thru 100MHz with a minimum amount of signal loss or deformation. The low-capacitance TransZorb may be applied directly across the signal line to prevent induced transients from lightning, power interruptions, or static discharge.

DESCRIPTION

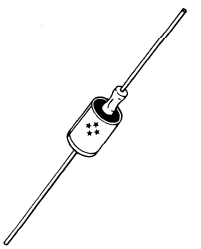
This series of device types is manufactured in a hermetic seal, DO-13 package. They are capable of being screened to the military specification.

If bipolar transient capability is required, two low-capacitance TransZorbs must be used in parallel, opposite in polarity for complete ac protection. For additional reduction in capacitance, these units can be used in conjunction with a bridge network. This will allow a lower capacitance with no change in peak pulse power capability of 1500 watts.

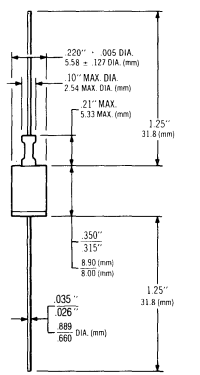
APPLICATION NOTE: Devices must be used with two units in parallel, opposite in polarity, as shown in circuit for AC Signal Line protection:



CASE DO-13



CASE OUTLINE



SCHEMATIC

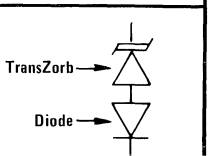


FIGURE 1—Peak Pulse Power vs Pulse Time

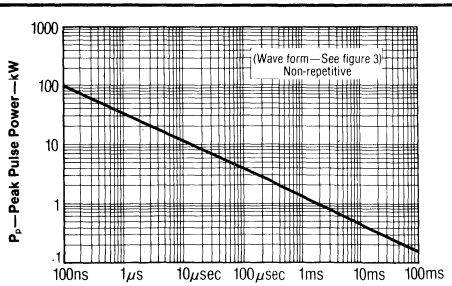
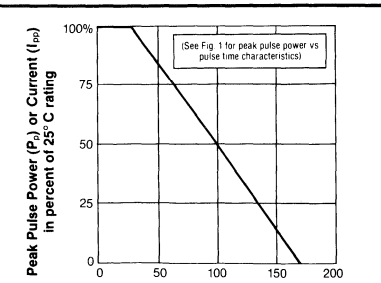


FIGURE 2—Derating Curve

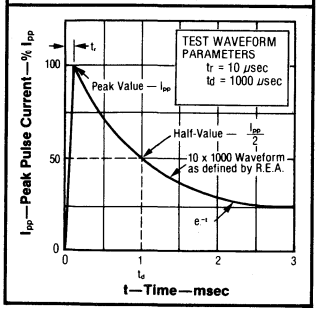


TRANSZORB®
UNIDIRECTIONAL
LOW CAPACITANCE
LC6.5 THRU LC90A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMI. PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE BV @ I_T VOLTS Min.	Max.	mA	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{PP} V_C VOLTS	MAX. PEAK PULSE CURRENT (FIG.3) I_{PP} AMPS	CAPACITANCE @ 0 VOLTS pF	WORKING INVERSE BLOCKING VOLTAGE V_{WIB} VOLTS	INVERSE BLOCKING LEAKAGE CURRENT @ V_{WIB} I_{IB} mA (Max)	PEAK INVERSE BLOCKING VOLTAGE V_{PIB} VOLTS
LC6.5	6.5	7.22	8.82	10	1000	12.3	100	100	75	1	100
LC6.5A	6.5	7.22	7.98	10	1000	11.2	100	100	75	1	100
LC7.0	7.0	7.78	9.51	10	500	13.3	100	100	75	1	100
LC7.0A	7.0	7.78	8.60	10	500	12.0	100	100	75	1	100
LC7.5	7.5	8.33	10.2	10	250	14.3	100	100	75	1	100
LC7.5A	7.5	8.33	9.21	10	250	12.9	100	100	75	1	100
LC8.0	8.0	8.89	10.9	1	100	15.0	100	100	75	1	100
LC8.0A	8.0	8.89	9.83	1	100	13.6	100	100	75	1	100
LC8.5	8.5	9.44	11.5	1	50	15.9	94	100	75	1	100
LC8.5A	8.5	9.44	10.4	1	50	14.4	100	100	75	1	100
LC9.0	9.0	10.0	12.2	1	10	16.9	89	100	75	1	100
LC9.0A	9.0	10.0	11.1	1	10	15.4	97	100	75	1	100
LC10	10	11.1	13.6	1	5	18.8	80	100	75	1	100
LC10A	10	11.1	12.3	1	5	17.0	88	100	75	1	100
LC11	11	12.2	14.9	1	5	20.1	74	100	75	1	100
LC11A	11	12.2	13.5	1	5	18.2	82	100	75	1	100
LC12	12	13.3	16.3	1	5	22.0	68	100	75	1	100
LC12A	12	13.3	14.7	1	5	19.9	75	100	75	1	100
LC13	13	14.4	17.6	1	5	23.8	63	100	75	1	100
LC13A	13	14.4	15.9	1	5	21.5	70	100	75	1	100
LC14	14	15.6	19.1	1	5	25.8	58	100	75	1	100
LC14A	14	15.6	17.2	1	5	23.2	65	100	75	1	100
LC15	15	16.7	20.4	1	5	26.9	56	100	75	1	100
LC15A	15	16.7	18.5	1	5	24.4	61	100	75	1	100
LC16	16	17.8	21.8	1	5	28.8	52	100	75	1	100
LC16A	16	17.8	19.7	1	5	26.0	57	100	75	1	100
LC17	17	18.9	23.1	1	5	30.5	49	100	75	1	100
LC17A	17	18.9	20.9	1	5	27.6	54	100	75	1	100
LC18	18	20.0	24.4	1	5	32.2	46	100	75	1	100
LC18A	18	20.0	22.1	1	5	29.2	51	100	75	1	100
LC20	20	22.2	27.1	1	5	35.8	42	100	75	1	100
LC20A	20	22.2	24.5	1	5	32.4	46	100	75	1	100
LC22	22	24.4	29.8	1	5	39.4	38	100	75	1	100
LC22A	22	24.4	26.9	1	5	35.5	42	100	75	1	100
LC24	24	26.7	32.6	1	5	43.0	35	100	75	1	100
LC24A	24	26.7	29.5	1	5	38.9	39	100	75	1	100
LC26	26	28.9	35.3	1	5	46.6	32	100	75	1	100
LC26A	26	28.9	31.9	1	5	42.1	36	100	75	1	100
LC28	28	31.1	38.0	1	5	50.1	30	100	75	1	100
LC28A	28	31.1	34.4	1	5	45.5	33	100	75	1	100
LC30	30	33.3	40.7	1	5	53.5	28	100	75	1	100
LC30A	30	33.3	36.8	1	5	48.4	31	100	75	1	100
LC33	33	36.7	44.9	1	5	59.0	25.4	100	75	1	100
LC33A	33	36.7	40.6	1	5	53.3	28.1	100	75	1	100
LC36	36	40.0	48.9	1	5	64.3	23.3	100	75	1	100
LC36A	36	40.0	44.2	1	5	58.1	25.8	100	75	1	100
LC40	40	44.4	54.3	1	5	71.4	21.0	100	75	1	100
LC40A	40	44.4	49.1	1	5	64.5	23.3	100	75	1	100
LC43	43	47.8	58.4	1	5	76.7	19.5	100	150	1	200
LC43A	43	47.8	52.8	1	5	69.4	21.6	100	150	1	200
LC45	45	50.0	61.1	1	5	80.3	18.7	100	150	1	200
LC45A	45	50.0	55.3	1	5	72.7	20.6	100	150	1	200
LC48	48	53.3	65.1	1	5	85.5	17.5	100	150	1	200
LC48A	48	53.3	58.9	1	5	77.4	19.4	100	150	1	200
LC51	51	56.7	69.3	1	5	91.1	16.5	100	150	1	200
LC51A	51	56.7	62.7	1	5	82.4	18.2	100	150	1	200
LC54	54	60.0	73.3	1	5	96.3	15.6	100	150	1	200
LC54A	54	60.0	66.3	1	5	87.1	17.2	100	150	1	200
LC58	58	64.4	78.7	1	5	103.0	14.6	100	150	1	200
LC58A	58	64.4	71.2	1	5	93.6	16.0	100	150	1	200
LC60	60	66.7	81.5	1	5	107.0	14.0	90	150	1	200
LC60A	60	66.7	73.7	1	5	96.8	15.5	90	150	1	200
LC64	64	71.1	86.9	1	5	114.0	13.2	90	150	1	200
LC64A	64	71.1	78.6	1	5	103.0	14.6	90	150	1	200
LC70	70	77.8	95.1	1	5	125	12.0	90	150	1	200
LC70A	70	77.8	86.0	1	5	113	13.3	90	150	1	200
LC75	75	83.3	102.0	1	5	134	11.2	90	150	1	200
LC75A	75	83.3	92.1	1	5	121	12.4	90	150	1	200
LC80	80	88.7	108	1	5	142	10.6	90	150	1	200
LC80A	80	88.7	98.0	1	5	129	11.6	90	150	1	200
LC90	90	100	122	1	5	160	9.4	90	300	1	200
LC90A	90	100	111	1	5	146	10.3	90	300	1	200

FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

General Semiconductor Industries, Inc.

NEW

BIDIRECTIONAL LOW CAPACITANCE

DIODE ARRAY TRANSZORB® TVS

LCA Series

FEATURES

- **500 watts peak pulse power**
- **RS422/423 and RS485 protection**
- **Low capacitance**
- **JEDEC registered package outline**
- **Multiple-diode array**

MAXIMUM RATINGS (per line)

- Peak Pulse Power (8/20μs): 500 watts
- Operating and Storage Temperature Range: -55°C to +150°C
- Soldering Temperature: +230°C (for less than 10 sec.)
- Rep Rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Molded 16 pin DIP
- Terminals: Solder dipped
- Body marked with part number, logo and date code
- Pins 1, 8, 9 and 16 are locating pins.

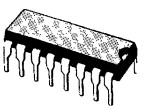
APPLICATION

The LCDA TVS devices are designed specifically for transient voltage suppression across signal or data lines at the board level. These devices can be used at the board interface or as protection of multiple IC components. Each device contains six (6) diode-TVS pairs for six bidirectional signal applications (pin #s 1, 8, 9 and 16 are inactive).

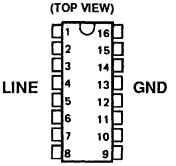
DESCRIPTION

The LCA TVS is a low capacitance, diode array designed to protect multiple data or signal lines. It is packaged in a16 pin dual-in-line package (DIP) to accomodate thru-hole circuit designs. Each pair of line/ground pins are electrically independent for multiple I/O port protection. The 16 pin device will protect up to six bidirectional lines.

CASE

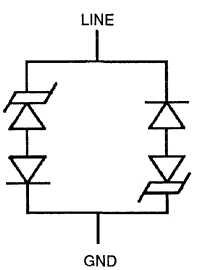


(TOP VIEW)



(No common internal ground.)

CIRCUIT DIAGRAM



Schematic

ABBREVIATIONS & SYMBOLS

V_D **Stand Off Voltage:** Applied Reverse Voltage to assure a nonconductive condition. (See Note.)

V_C **Maximum Clamping Voltage:** The maximum peak voltage appearing across the TransZorb TVS when subjected to the peak pulse current waveform of 8 x 20μs. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{PP} **Peak Pulse Current**

P_P **Peak Pulse Power**

I_D **Reverse Leakage**

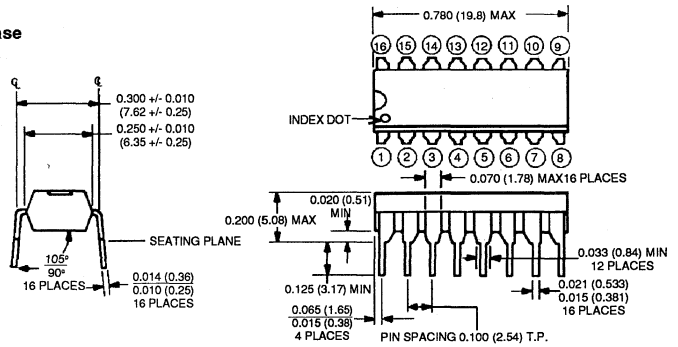
NOTE: A TransZorb® TVS is normally selected according to the Reverse Stand Off Voltage (V_D) which should be equal to or greater than the dc or continuous peak operating voltage level.

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @ 1mA	LEAKAGE CURRENT @ V_D	MAXIMUM CLAMPING VOLTAGE @ 1A (See Figure 2)	MAXIMUM CLAMPING VOLTAGE @ 10A (See Figure 2)	CAPACITANCE @ 0V, 1MHz
	V_D Volts	B_V Volts	I_D μA	V_C Volts	V_C Volts	C pF
LCA05C	5	6.0	400	9.8	12.5	25
LCA12C	12	13.3	4	19.1	23.5	25

CASE OUTLINES

16 pin plastic case



Measurements in inches (mm)

FIGURE 1 -- Peak Pulse Power vs. Pulse Time

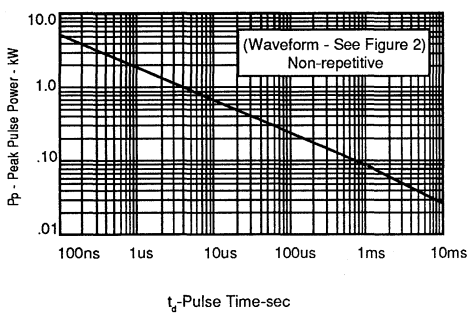


FIGURE 2 -- Pulse Waveform

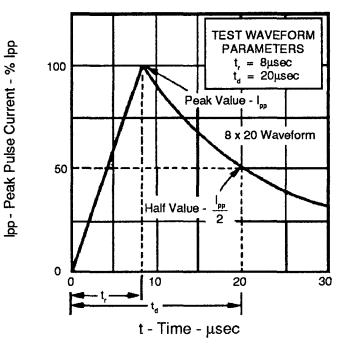
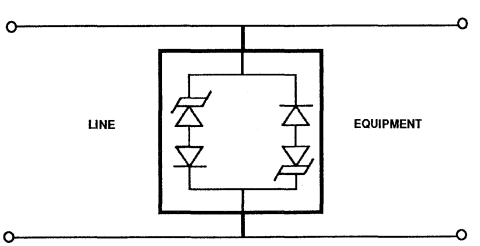


FIGURE 3 -- Data/Signal Line Protection Schematic



General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS

LOW CAPACITANCE
LCE6.5 THRU LCE90A

FEATURES

- **1500 watts Peak Pulse Power dissipation**
- **Available in ranges from 6.5 to 90**
- **Low capacitance ac signal protection**
- **Each device 100% tested**

MAXIMUM RATINGS

- 1500 watts of Peak Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 5×10^{-9} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Steady State power dissipation: 5.0W at T_L = 75°C, Lead Length = 3/8"
- Repetition rate (duty cycle): .05%

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.5 grams (approximate)
- Polarity band on cathode end of the TransZorb (positive potential applied)
- Body marked with Logo ⁂ and type number

ELECTRICAL CHARACTERISTICS

Clamping Factor: 1.40 at full rated power
1.30 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Voltage) to the BV (Breakdown Voltage) as measured on a specific device.

Note: When pulse testing, test in TransZorb Avalanche direction. DO NOT pulse in forward direction.

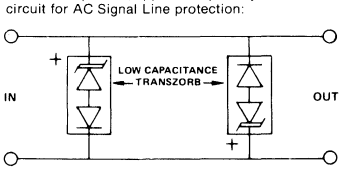
APPLICATION

This specification sheet defines a series of low-capacitance silicon transient suppressors for the protection of ac signal line. This series employs a standard TransZorb® in series with a rectifier with the same transient capabilities as the TransZorb. The rectifier is also used to reduce the effective capacitance up thru 100MHz with a minimum amount of signal loss or deformation. The low-capacitance TransZorb may be applied directly across the signal line to prevent induced transients from lightning, power interruptions, or static discharge.

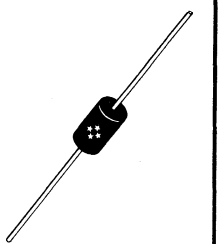
DESCRIPTION

Designed for commercial applications, this series offers pricing advantages. They have the same characteristics as the standard TransZorb, that is, high surge capability and extremely fast response time. If bipolar transient capability is required, two low-capacitance TransZorbs must be used in parallel, opposite in polarity for complete ac protection. For additional reduction in capacitance, these units can be used in conjunction with a bridge network. This will allow a lower capacitance with no change in peak pulse power capability of 1500 watts.

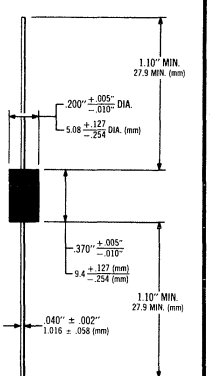
APPLICATION NOTE: Devices must be used with two units in parallel, opposite in polarity, as shown in circuit for AC Signal Line protection:



CASE 1



CASE OUTLINE



SCHEMATIC

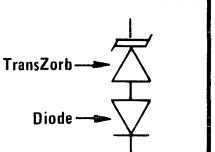


FIGURE 1—Peak Pulse Power vs Pulse Time

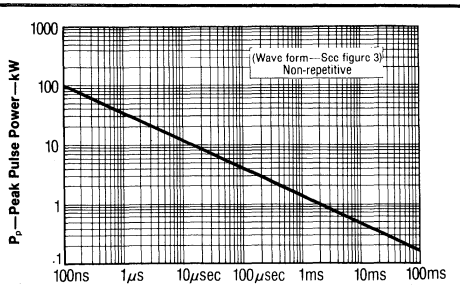
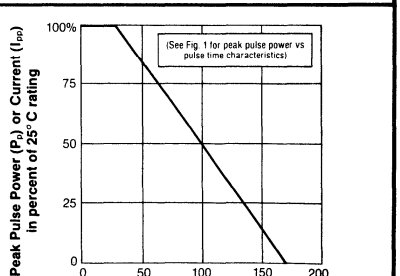


FIGURE 2—Derating Curve



TransZorb®

UNIDIRECTIONAL

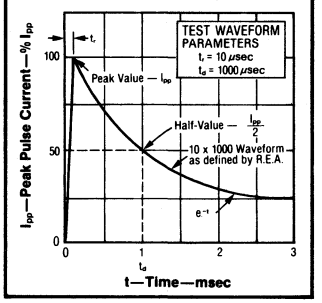
LOW CAPACITANCE

LCE6.5 THRU LCE90A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMI. PART NUMBER	REVERSE STAND-OFF VOLTAGE V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS @ I_T Min.	Max.	mA	MAXIMUM REVERSE LEAKAGE @ V_R I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{pp} V_C VOLTS	MAX. PEAK PULSE CURRENT (FIG. 3) I_{pp} AMPS	CAPACITANCE @ 0 VOLTS pF	WORKING INVERSE BLOCKING VOLTAGE V_{WIB} VOLTS	INVERSE BLOCKING LEAKAGE CURRENT @ V_{WIB} I_{IB} mA (Max)	PEAK INVERSE BLOCKING VOLTAGE V_{PIB} VOLTS
LCE6.5	6.5	7.22	8.82	10	1000	12.3	100	100	75	1	100
LCE6.5A	6.5	7.22	7.98	10	1000	11.2	100	100	75	1	100
LCE7.0	7.0	7.78	9.51	10	500	13.3	100	100	75	1	100
LCE7.0A	7.0	7.78	8.60	10	500	12.0	100	100	75	1	100
LCE7.5	7.5	8.33	10.2	10	250	14.3	100	100	75	1	100
LCE7.5A	7.5	8.33	9.21	10	250	12.9	100	100	75	1	100
LCE8.0	8.0	8.89	10.9	1	100	15.0	100	100	75	1	100
LCE8.0A	8.0	8.89	9.83	1	100	13.6	100	100	75	1	100
LCE8.5	8.5	9.44	11.5	1	50	15.9	94	100	75	1	100
LCE8.5A	8.5	9.44	10.4	1	50	14.4	100	100	75	1	100
LCE9.0	9.0	10.0	12.2	1	10	16.9	89	100	75	1	100
LCE9.0A	9.0	10.0	11.1	1	10	15.4	97	100	75	1	100
LCE10	10	11.1	13.6	1	5	18.8	80	100	75	1	100
LCE10A	10	11.1	12.3	1	5	17.0	88	100	75	1	100
LCE11	11	12.2	14.9	1	5	20.1	74	100	75	1	100
LCE11A	11	12.2	13.5	1	5	18.2	82	100	75	1	100
LCE12	12	13.3	16.3	1	5	22.0	68	100	75	1	100
LCE12A	12	13.3	14.7	1	5	19.9	75	100	75	1	100
LCE13	13	14.4	17.6	1	5	23.8	63	100	75	1	100
LCE13A	13	14.4	15.9	1	5	21.5	70	100	75	1	100
LCE14	14	15.6	19.1	1	5	25.8	58	100	75	1	100
LCE14A	14	15.6	17.2	1	5	23.2	65	100	75	1	100
LCE15	15	16.7	20.4	1	5	26.9	56	100	75	1	100
LCE15A	15	16.7	18.5	1	5	24.4	61	100	75	1	100
LCE16	16	17.8	21.8	1	5	28.8	52	100	75	1	100
LCE16A	16	17.8	19.7	1	5	26.0	57	100	75	1	100
LCE17	17	18.9	23.1	1	5	30.5	49	100	75	1	100
LCE17A	17	18.9	20.9	1	5	27.6	54	100	75	1	100
LCE18	18	20.0	24.4	1	5	32.2	46	100	75	1	100
LCE18A	18	20.0	22.1	1	5	29.2	51	100	75	1	100
LCE20	20	22.2	27.1	1	5	35.8	42	100	75	1	100
LCE20A	20	22.2	24.5	1	5	32.4	46	100	75	1	100
LCE22	22	24.4	29.8	1	5	39.4	38	100	75	1	100
LCE22A	22	24.4	26.9	1	5	35.5	42	100	75	1	100
LCE24	24	26.7	32.6	1	5	43.0	35	100	75	1	100
LCE24A	24	26.7	29.5	1	5	38.9	39	100	75	1	100
LCE26	26	28.9	35.3	1	5	46.6	32	100	75	1	100
LCE26A	26	28.9	31.9	1	5	42.1	36	100	75	1	100
LCE28	28	31.1	38.0	1	5	50.1	30	100	75	1	100
LCE28A	28	31.1	34.4	1	5	45.5	33	100	75	1	100
LCE30	30	33.3	40.7	1	5	53.5	28	100	75	1	100
LCE30A	30	33.3	36.8	1	5	48.4	31	100	75	1	100
LCE33	33	36.7	44.9	1	5	59.0	25.4	100	75	1	100
LCE33A	33	36.7	40.6	1	5	53.3	28.1	100	75	1	100
LCE36	36	40.0	48.9	1	5	64.3	23.3	100	75	1	100
LCE36A	36	40.0	44.2	1	5	58.1	25.8	100	75	1	100
LCE40	40	44.4	54.3	1	5	71.4	21.0	100	75	1	100
LCE40A	40	44.4	49.1	1	5	64.5	23.3	100	75	1	100
LCE43	43	47.8	58.4	1	5	76.7	19.5	100	150	1	200
LCE43A	43	47.8	52.8	1	5	69.4	21.6	100	150	1	200
LCE45	45	50.0	61.1	1	5	80.3	18.7	100	150	1	200
LCE45A	45	50.0	55.3	1	5	72.7	20.6	100	150	1	200
LCE48	48	53.3	65.1	1	5	85.5	17.5	100	150	1	200
LCE48A	48	53.3	58.9	1	5	77.4	19.4	100	150	1	200
LCE51	51	56.7	69.3	1	5	91.1	16.5	100	150	1	200
LCE51A	51	56.7	62.7	1	5	82.4	18.2	100	150	1	200
LCE54	54	60.0	73.3	1	5	96.3	15.6	100	150	1	200
LCE54A	54	60.0	66.3	1	5	87.1	17.2	100	150	1	200
LCE58	58	64.4	78.7	1	5	103.0	14.6	100	150	1	200
LCE58A	58	64.4	71.2	1	5	93.6	16.0	100	150	1	200
LCE60	60	66.7	81.5	1	5	107.0	14.0	90	150	1	200
LCE60A	60	66.7	73.7	1	5	96.8	15.5	90	150	1	200
LCE64	64	71.1	86.9	1	5	114.0	13.2	90	150	1	200
LCE64A	64	71.1	78.6	1	5	103.0	14.6	90	150	1	200
LCE70	70	77.8	95.1	1	5	125	12.0	90	150	1	200
LCE70A	70	77.8	86.0	1	5	113	13.3	90	150	1	200
LCE75	75	83.3	102.0	1	5	134	11.2	90	150	1	200
LCE75A	75	83.3	92.1	1	5	121	12.4	90	150	1	200
LCE80	80	88.7	108	1	5	142	10.6	90	150	1	200
LCE80A	80	88.7	98.0	1	5	129	11.6	90	150	1	200
LCE90	90	100	122	1	5	160	9.4	90	300	1	200
LCE90A	90	100	111	1	5	146	10.3	90	300	1	200

FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R — Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) — This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) — Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} — Peak Pulse Current — See Figure 3
- P_p — Peak Pulse Power
- I_R — Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS
P6KE6.8 THRU P6KE400A

FEATURES

- **600 watts Peak Pulse Power dissipation**
- **Available in ranges from 6.8 to 400V volts**
- **BIDIRECTIONAL types available**
- **Each device 100% tested**

MAXIMUM RATINGS

- 600 watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1×10^{-12} second (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: half cycle 100A, 1/120 sec @ 25° C (Unidirectional)
- Steady State power dissipation: 5W at T_L = 75°C, Lead Length = 3/8"
- Repetition rate (duty cycle): .01%

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.5 grams (approximate)
- Positive terminal marked with band (except Bidirectional)
- Body marked with Logo and type number

APPLICATION

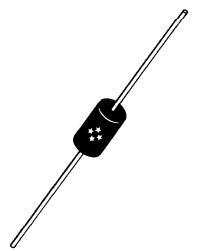
This TransZorb® series is a low cost commercial product for use in applications where large voltage transients can permanently damage voltage-sensitive components. It has a peak pulse power rating of 600 watts for one millisecond. The response time of TransZorbs clamping action is theoretically instantaneous (1×10^{-12} sec.); therefore, they can protect Integrated Circuits, MOS devices, Hybrids, and other voltage-sensitive components. TransZorbs can also be used in series or parallel to increase the peak pulse power ratings. This is only one of many series of Transient Voltage Suppressors available from General Semiconductor Industries.

DESCRIPTION

The P6KE series device types are designed in a small package size where power and space is a consideration. They are characterized by their high surge capability, extremely fast response time, and low impedance, (R_{on}). Because of the unpredictable nature of transients and the variation of the impedance with respect to these transients, impedance, per se, is not specified as a parametric value. However, a minimum voltage at low current conditions (BV) and a maximum clamping voltage (V_C) at a maximum peak pulse current is specified.

In some instances, the thermal effect (see V_C Clamping Voltage) may be responsible for 50% to 70% of the observed voltage differential when subjected to high current pulses for several duty cycles, thus making a maximum impedance specification insignificant. In case of a severe current overload or abnormal transient beyond the maximum ratings, the TransZcrb will initially fail "short" thus tripping the system's circuit breaker or fuse while protecting the entire circuit. Curves depicting clamping voltage vs. various current pulses are available from the factory. Extended power curves vs. pulse time are also available.

CASE 7



CASE OUTLINE

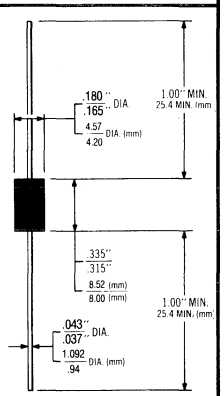


FIGURE 1—Peak Pulse Power vs Pulse Time

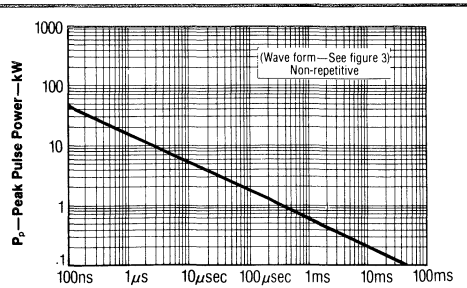
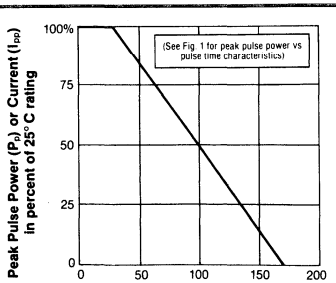


FIGURE 2—Derating Curve



TRANSZORB® UNIDIRECTIONAL & BIDIRECTIONAL P6KE6.8 THRU P6KE400A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE BV VOLTS @ I_T MIN.	MAX.	mA	MAXIMUM REVERSE LEAKAGE @ V_R [NOTE 2] I_R μA	MAXIMUM CLAMPING VOLTAGE @ I_{pp} (FIG. 3) V_C VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{pp} A	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV mV/°C
*P6KE6.8	5.50	6.12	7.48	10	1000	10.8	56	5.0
*P6KE6.8A	5.80	6.45	7.14	10	1000	10.5	57	5.0
P6KE7.5	6.05	6.75	8.25	10	500	11.7	51	5.0
P6KE7.5A	6.40	7.13	7.88	10	500	11.3	53	5.0
P6KE8.2	6.63	7.38	9.02	10	200	12.5	48	6.0
P6KE8.2A	7.02	7.79	8.61	10	200	12.1	50	6.0
P6KE9.1	7.37	8.19	10.0	1	50	13.8	44	7.0
P6KE9.1A	7.78	8.65	9.55	1	50	13.4	45	7.0
P6KE10	8.10	9.00	11.0	1	10	15.0	40	8.0
P6KE10A	8.55	9.5	10.5	1	10	14.5	41	8.0
P6KE11	8.92	9.9	12.1	1	5	16.2	37	9.0
P6KE11A	9.40	10.5	11.6	1	5	15.6	38	9.0
P6KE12	9.72	10.8	13.2	1	5	17.3	35	10
P6KE12A	10.2	11.4	12.6	1	5	16.7	36	10
P6KE13	10.5	11.7	14.3	1	5	19.0	32	11
P6KE13A	11.1	12.4	13.7	1	5	18.2	33	11
P6KE15	12.1	13.5	16.5	1	5	22.0	27	13
P6KE15A	12.8	14.3	15.8	1	5	21.2	28	12
P6KE16	12.9	14.4	17.6	1	5	23.5	26	16
P6KE16A	13.6	15.2	16.8	1	5	22.5	27	14
P6KE18	14.5	16.2	19.8	1	5	26.5	23	17
P6KE18A	15.3	17.1	18.9	1	5	25.2	24	19
P6KE20	16.2	18.0	22.0	1	5	29.1	21	20
P6KE20A	17.1	19.0	21.0	1	5	27.7	22	19
P6KE22	17.8	19.8	24.2	1	5	31.9	19	21
P6KE22A	18.8	20.9	23.1	1	5	30.6	20	20
P6KE24	19.4	21.6	26.4	1	5	34.7	17	25
P6KE24A	20.5	22.8	25.2	1	5	33.2	18	23
P6KE27	21.8	24.3	29.7	1	5	39.1	15	28
P6KE27A	23.1	25.7	28.4	1	5	37.5	16	25
P6KE30	24.3	27.0	33.0	1	5	43.5	14	31
P6KE30A	25.6	28.5	31.5	1	5	41.4	14.4	28
P6KE33	26.8	29.7	36.3	1	5	47.7	12.6	31
P6KE33A	28.2	31.4	34.7	1	5	45.7	13.2	20
P6KE36	29.1	32.4	39.6	1	5	52.0	11.6	35
P6KE36A	30.8	34.2	37.8	1	5	49.9	12.0	31
P6KE39	31.6	35.1	42.9	1	5	56.4	10.6	39
P6KE39A	33.3	37.1	41.0	1	5	53.9	11.2	36
P6KE43	34.8	38.7	47.3	1	5	61.9	9.6	46
P6KE43A	36.8	40.9	45.2	1	5	59.3	10.1	44
P6KE47	38.1	42.3	51.7	1	5	67.8	8.9	50
P6KE47A	40.2	44.7	49.4	1	5	64.8	9.3	48
P6KE51	41.3	45.9	56.1	1	5	73.5	8.2	55
P6KE51A	43.6	48.5	53.6	1	5	70.1	8.6	51
P6KE56	45.4	50.4	61.6	1	5	80.5	7.4	58
P6KE56A	47.8	53.2	58.8	1	5	77.0	7.8	56
P6KE62	50.2	55.8	68.2	1	5	89.0	6.8	65
P6KE62A	53.0	58.9	65.1	1	5	85.0	7.1	62
P6KE68	55.1	61.2	74.8	1	5	98.0	6.1	71
P6KE68A	58.1	64.6	71.4	1	5	92.0	6.5	69
P6KE75	60.7	67.5	82.5	1	5	108.0	5.5	80
P6KE75A	64.1	71.3	78.8	1	5	103.0	5.8	76
P6KE82	66.4	73.8	90.2	1	5	118.0	5.1	90
P6KE82A	70.1	77.9	86.1	1	5	113.0	5.3	86
P6KE91	73.7	81.9	100.0	1	5	131.0	4.5	99
P6KE91A	77.8	86.5	95.5	1	5	125.0	4.8	94
P6KE100	81.0	90.0	110.0	1	5	144.0	4.2	109
P6KE100A	85.5	95.0	105.0	1	5	137.0	4.4	104
P6KE110	89.2	99.0	121.0	1	5	158.0	3.8	120
P6KE110A	94.0	105.0	116.0	1	5	152.0	4.0	115
P6KE120	97.2	108.0	132.0	1	5	173.0	3.5	131
P6KE120A	102.0	114.0	126.0	1	5	165.0	3.6	125
P6KE130	105.0	117.0	143.0	1	5	187.0	3.2	142
P6KE130A	111.0	124.0	137.0	1	5	179.0	3.3	136
P6KE150	121.0	135.0	165.0	1	5	215.0	2.8	164
P6KE150A	128.0	143.0	158.0	1	5	207.0	2.9	157
P6KE160	130.0	144.0	176.0	1	5	230.0	2.6	175
P6KE160A	136.0	152.0	168.0	1	5	219.0	2.7	167
P6KE170	138.0	153.0	187.0	1	5	244.0	2.5	186
P6KE170A	145.0	162.0	179.0	1	5	234.0	2.6	188
P6KE180	146.0	162.0	198.0	1	5	258.0	2.3	197
P6KE180A	154.0	171.0	189.0	1	5	246.0	2.4	188
P6KE200	162.0	180.0	220.0	1	5	287.0	2.1	219
P6KE200A	171.0	190.0	210.0	1	5	274.0	2.2	209
P6KE220	175.0	198.0	242.0	1	5	344.0	2.0	240
P6KE220A	185.0	209.0	231.0	1	5	328.0	2.0	230
P6KE250	202.0	225.0	275.0	1	5	360.0	2.0	270
P6KE250A	214.0	237.0	263.0	1	5	344.0	2.0	260
P6KE300	243.0	270.0	330.0	1	5	430.0	2.0	330
P6KE300A	256.0	285.0	315.0	1	5	414.0	2.0	315
P6KE350	284.0	315.0	385.0	1	5	504.0	2.0	385
P6KE350A	300.0	333.0	368.0	1	5	482.0	2.0	368
P6KE400	324.0	360.0	440.0	1	5	574.0	2.0	440
P6KE400A	342.0	380.0	420.0	1	5	548.0	2.0	420

V_f at 50 amps peak, 8.3 msec sine wave = 3.5 volts maximum (except bidirectional device).

FOR BIDIRECTIONAL APPLICATIONS—use C or CA suffix for types P6KE7.5 through P6KE400CA.

*Not available as bidirectional.

FIGURE 3—Pulse Waveform

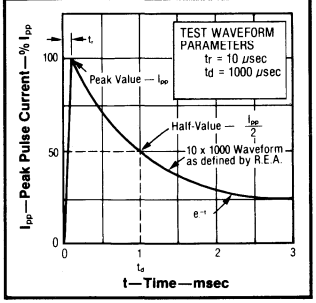
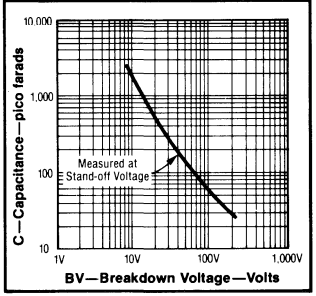


FIGURE 4—Typical Capacitance vs BV (Unidirectional Only)



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

Note 2: For Bipolar types 10 volts and under, the I_R limit is doubled.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25° C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
BIDIRECTIONAL
PHP8.4 THRU PHP500
AND
PIP8.4 THRU PIP500

FEATURES

- **7,500 and 15,000 watts Peak Pulse Power dissipation**
- **Available in ranges from 8.4 to 500 volts**
- **Designed for Military (PHP series) ‡ and commercial (PIP series)**
- **UL Recognized (PIP120)**
- **Each device 100% tested**

MAXIMUM RATINGS

- 7,500 and 15,000 watts Peak Pulse power dissipation at the 1 msec pulse and 25°C (see derating curve)
- Operating and Storage temperatures: -65° to + 150°C
- Average Steady State power dissipation at 50°C: 7.5 watts
- $t_{clamping}$ (0 volts to BV): Less than 1×10^{-8} seconds

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 46 grams (approximate)
- Bipolar for AC Applications
- Body marked with Logo and type number

‡ Military Applications: PHP SERIES Modules can have design consistency with the following MILITARY requirements as controlling specifications.

- MIL-STD-1399
- MIL-E-16400
- MIL-STD-704
- MIL-S-19500/507

APPLICATION

PHP/PIP series is designed for applications requiring "across-the-line" AC power protection. These TransZorb® modules are used in applications where extreme voltage transients can permanently damage voltage sensitive systems or components. These devices are most often used when discrete TransZorbs do not have high enough power requirements to suppress large power surges.

DESCRIPTION

TransZorb modules can be used to protect equipment from induced lightning, power surges and transients originating from inductive switching or power interrupt. The modules have been successfully used for both commercial and military applications, including telecommunications, aircraft, shipboard, central office switching and PABX, CATV distribution, computers, distributed data processing, and power supplies.

For military applications, the PHP module sub-assemblies are packaged in a hermetically sealed glass-to-metal package. The screening would consist of 100% TX level environmental testing per MIL-S-19500/507A (Para. 4.3). For ordering these options, use the following suffix.

H1 — Submodule Screening,
H2 — Submodule and Module Screening,
H3 — Submodule and Module Screening. Module Group B & C lot testing. See Appendix for Processing Test Plan.

CASE 22

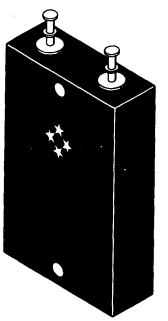


FIGURE 1—Peak Pulse Power vs Pulse Time

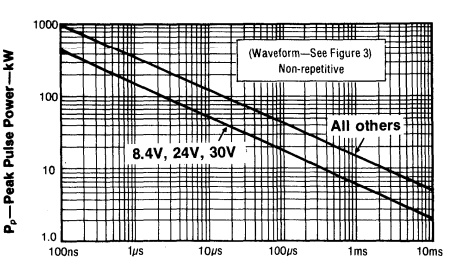
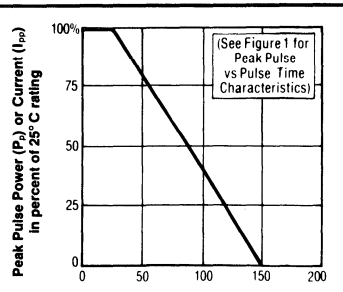


FIGURE 2—Derating Curve



TransZorb®

BIDIRECTIONAL

PHP8.4 THRU PHP500 AND PIP8.4 THRU PIP500

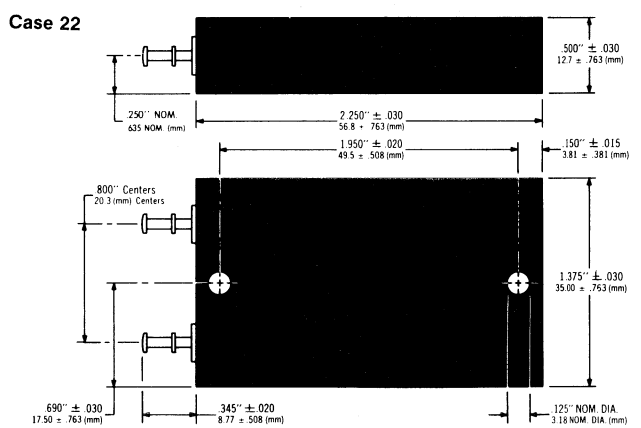
ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	AVERAGE RMS VOLTAGE VOLTAGE VOLTS AC	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS DC	MINIMUM BREAKDOWN VOLTAGE BV VOLTS	@ I_T mA	MAXIMUM REVERSE LEAKAGE (I_R) @ V_R MICRO AMPERES	MAXIMUM CLAMPING VOLTAGE V_C @ I_{PP} VOLTS DC	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{PP} A	MAXIMUM PEAK PULSE POWER (1 MSEC) (P_P) KILOWATTS
PHP 8.4	8.4	12.0	14	10	250	22	341	7.5
PHP 24	24.0	34.0	40	10	250	67	112	7.5
PHP 30	30.0	42.5	50	1.0	250	84	90	7.5
PHP 60	60.0	85.0	100	1.0	250	167	90	15.0
PHP 120*	120.0	170.0	200	1.0	250	319	47	15.0
PHP 208	208.0	295.0	347	1.0	250	536	28	15.0
PHP 250*	250.0	354.0	418	1.0	250	652	23	15.0
PHP 440	440.0	623.0	735	1.0	250	1138	13.2	15.0
PHP 500*	500.0	708.0	835	1.0	250	1292	11.6	15.0
PIP 8.4	8.4	12.0	14	10	250	22	341	7.5
PIP 24	24.0	34.0	40	10	250	67	112	7.5
PIP 30	30.0	42.5	50	1.0	250	84	90	7.5
PIP 60	60.0	85.0	100	1.0	250	167	90	15.0
PIP 120*†	120.0	170.0	200	1.0	250	319	47	15.0
PIP 208	208.0	295.0	347	1.0	250	536	28	15.0
PIP 250*	250.0	354.0	418	1.0	250	652	23	15.0
PIP 440	440.0	623.0	735	1.0	250	1138	13.2	15.0
PIP 500*	500.0	708.0	835	1.0	250	1292	11.6	15.0

Special Voltages available from factory. *Recommended for marine applications. †UL Listed.

CASE OUTLINE

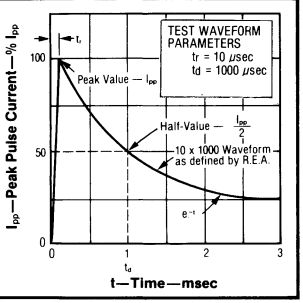
Case 22



MILITARY APPLICATIONS: PHP series sub-assemblies are packaged in a hermetically sealed glass-to-metal package, available with design consistency to MIL-S-19500/507.

COMMERCIAL APPLICATIONS: PIP series sub-assemblies are packaged in a molded epoxy case.

FIGURE 3—Pulse Waveform



NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)
- BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
- V_C(max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
- I_{pp} Peak Pulse Current — See Figure 3
- P_p Peak Pulse Power
- I_R Reverse Leakage

General Semiconductor Industries, Inc.

TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS SA5.0 THRU SA170A

FEATURES

- **500 watts Peak Pulse Power**
- **Fast Response**
- **Available in ranges from 5.0 to 170 volts**
- **Bidirectional types available**
- **Low clamping voltage**
- **Small package size**
- **Each device 100% tested**

MAXIMUM RATINGS

- 500 watts of Peak Power dissipation at 25°C
- Operating and Storage Temp.: -55° to +175°C
- Forward surge current; 70A, 1/120 sec half cycle @ 25°c (Unidirectional only)
- Steady State power dissipation: 1.0 watt at T_L = 75°C, Lead Length = ⅜"

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.0 grams (approximate)
- Unidirectional types, positive terminal marked with band
- Body marked with Logo ♦ and type number

DESCRIPTION

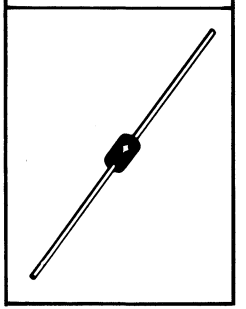
This TransZorb TVS series is a low cost, 500 watt commercial and industrial product for use in applications where space is a premium and where large voltage transients can permanently damage voltage-sensitive components.

APPLICATION

This TransZorb TVS diode has a peak pulse power rating of 500 watts for one millisecond. The response time of TransZorb TVS clamping action is theoretically instantaneous (1 x 10^{-12} sec); therefore, they can protect integrated circuits, MOS devices, hybrids, and other voltage-sensitive semiconductors and components.

TransZorb TVS diodes can be used in series or parallel to increase the peak power ratings.

CASE 25



CASE OUTLINE

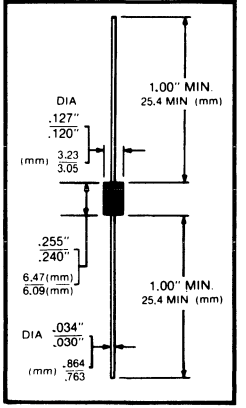


FIGURE 1—Peak Pulse Power vs Pulse Time

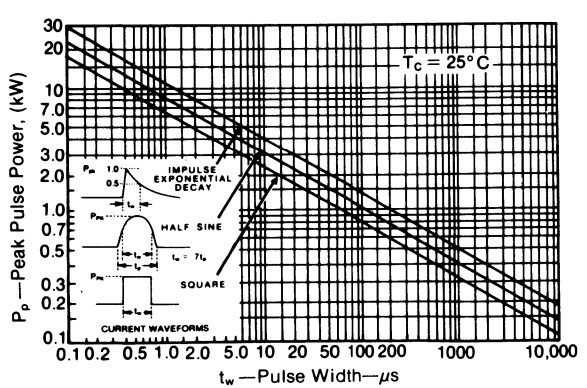
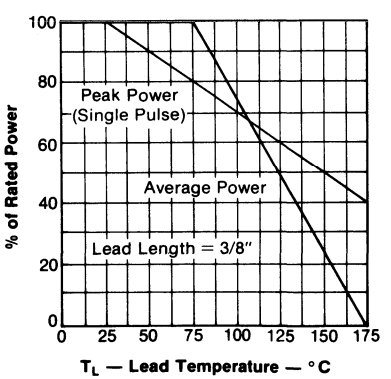


FIGURE 2—Power Derating



TRANSZORB® UNIDIRECTIONAL & BIDIRECTIONAL SA5.0 THRU SA170A

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER (NOTE 1)	REVERSE STAND-OFF VOLTAGE (NOTE 2) V_R VOLTS	BREAKDOWN VOLTAGE V_{BR} VOLTS MIN.	MAX.	@ I_T mA	MAXIMUM CLAMPING VOLTAGE @ I_{PP} (FIG. 3) V_C VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 3) I_{PP} A	MAXIMUM REVERSE LEAKAGE @ V_R (NOTE 3) I_R µA	MAXIMUM VOLTAGE TEMPERATURE VARIATION OF BV $\Delta V_{C(Max)}$ mV/°C
SA5.0*	5.0	6.40	7.30	10	9.6	52.0	600	5.0
SA5.0A*	5.0	6.40	7.00	10	9.2	54.3	600	5.0
SA6.0*	6.0	6.67	8.15	10	11.4	43.9	600	5.0
SA6.0A*	6.0	6.67	7.37	10	10.3	48.5	600	5.0
SA6.5	6.5	7.22	8.82	10	12.3	40.7	400	5.0
SA6.5A	6.5	7.22	7.98	10	11.2	44.7	400	5.0
SA7.0	7.0	7.78	9.51	10	13.3	37.8	150	6.0
SA7.0A	7.0	7.78	8.60	10	12.0	41.7	150	6.0
SA7.5	7.5	8.33	10.2	1	14.3	35.0	50	7.0
SA7.5A	7.5	8.33	9.21	1	12.9	38.8	50	7.0
SA8.0	8.0	8.89	10.9	1	15.0	33.3	25	7.0
SA8.0A	8.0	8.89	9.83	1	13.6	36.7	25	7.0
SA8.5	8.5	9.44	11.5	1	15.9	31.4	10	8.0
SA8.5A	8.5	9.44	10.4	1	14.4	34.7	10	8.0
SA9.0	9.0	10.0	12.2	1	16.9	29.5	5	9.0
SA9.0A	9.0	10.0	11.1	1	15.4	32.5	5	9.0
SA10	10	11.1	13.6	1	18.8	26.6	3	10
SA10A	10	11.1	12.3	1	17.0	29.4	3	10
SA11	11	12.2	14.9	1	20.1	24.9	3	11
SA11A	11	12.2	13.5	1	18.2	27.4	3	11
SA12	12	13.3	16.3	1	22.0	22.7	3	12
SA12A	12	13.3	14.7	1	19.9	25.1	3	12
SA13	13	14.4	17.6	1	23.8	21.0	3	13
SA13A	13	14.4	15.9	1	21.5	23.2	3	13
SA14	14	15.6	19.1	1	25.8	19.4	3	14
SA14A	14	15.6	17.2	1	23.2	21.5	3	14
SA15	15	16.7	20.4	1	26.9	18.8	3	16
SA15A	15	16.7	18.5	1	24.4	20.6	3	16
SA16	16	17.8	21.8	1	28.8	17.6	3	19
SA16A	16	17.8	19.7	1	26.0	19.2	3	17
SA17	17	18.9	23.1	1	30.5	16.4	3	20
SA17A	17	18.9	20.9	1	27.6	18.1	3	19
SA18	18	20.0	24.4	1	32.2	15.5	3	21
SA18A	18	20.0	22.1	1	29.2	17.2	3	20
SA20	20	22.2	27.1	1	35.8	13.9	3	25
SA20A	20	22.2	24.5	1	32.4	15.4	3	23
SA22	22	24.4	29.8	1	39.4	12.7	3	28
SA22A	22	24.4	26.9	1	35.5	14.1	3	25
SA24	24	26.7	32.6	1	43.0	11.6	3	31
SA24A	24	26.7	29.5	1	38.9	12.8	3	28
SA26	26	28.9	35.3	1	46.6	10.7	3	31
SA26A	26	28.9	31.9	1	42.1	11.9	3	30
SA28	28	31.1	38.0	1	50.0	9.9	3	35
SA28A	28	31.1	34.4	1	45.4	11.0	3	31
SA30	30	33.3	40.7	1	53.5	9.3	3	39
SA30A	30	33.3	36.8	1	48.4	10.3	3	36
SA33	33	36.7	44.9	1	59.0	8.5	3	42
SA33A	33	36.7	40.6	1	53.3	9.4	3	39
SA36	36	40.0	48.9	1	64.3	7.8	3	46
SA36A	36	40.0	44.2	1	58.1	8.6	3	41
SA40	40	44.4	54.3	1	71.4	7.0	3	51
SA40A	40	44.4	49.1	1	64.5	7.8	3	46
SA43	43	47.8	58.4	1	76.7	6.5	3	55
SA43A	43	47.8	52.8	1	69.4	7.2	3	50
SA45	45	50.0	61.1	1	80.3	6.2	3	58
SA45A	45	50.0	55.3	1	72.7	6.9	3	52
SA48	48	53.3	65.1	1	85.5	5.8	3	63
SA48A	48	53.3	58.9	1	77.4	6.5	3	56
SA51	51	56.7	69.3	1	91.1	5.5	3	66
SA51A	51	56.7	62.7	1	82.4	6.1	3	61
SA54	54	60.0	73.3	1	96.3	5.2	3	71
SA54A	54	60.0	66.3	1	87.1	5.7	3	65
SA58	58	64.4	78.7	1	103.0	4.9	3	78
SA58A	58	64.4	71.2	1	93.6	5.3	3	70
SA60	60	66.7	81.5	1	107.0	4.7	3	80
SA60A	60	66.7	73.7	1	96.8	5.2	3	71
SA64	64	71.1	86.9	1	114.0	4.4	3	86
SA64A	64	71.1	78.6	1	103.0	4.9	3	76
SA70	70	77.8	95.1	1	125	4.0	3	94
SA70A	70	77.8	86.0	1	113	4.4	3	85
SA75	75	83.3	102.0	1	134	3.7	3	101
SA75A	75	83.3	92.1	1	121	4.1	3	91
SA78	78	86.7	106.0	1	139	3.6	3	105
SA78A	78	86.7	95.8	1	126	4.0	3	95
SA85	85	94.4	115.0	1	151	3.3	3	114
SA85A	85	94.4	104.0	1	137	3.6	3	103
SA90	90	100	122	1	160	3.1	3	121
SA90A	90	100	111	1	146	3.4	3	110
SA100	100	111	136	1	179	2.8	3	135
SA100A	100	111	123	1	162	3.1	3	123
SA110	110	122	149	1	196	2.6	3	148
SA110A	110	122	135	1	177	2.8	3	133
SA120	120	133	163	1	214	2.3	3	162
SA120A	120	133	147	1	193	2.0	3	146
SA130	130	144	176	1	231	2.2	3	175
SA130A	130	144	159	1	209	2.4	3	158
SA150	150	167	204	1	268	1.9	3	203
SA150A	150	167	185	1	243	2.1	3	184
SA160	160	178	218	1	287	1.7	3	217
SA160A	160	178	197	1	259	1.9	3	196
SA170	170	189	231	1	304	1.6	3	230
SA170A	170	189	209	1	275	1.8	3	208

*Not available as bidirectional devices.

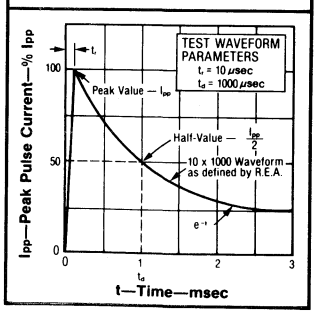
ABBREVIATIONS & SYMBOLS

- V_R Stand-Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 2)
- V_{BR} Breakdown Voltage.
- $V_{C(max)}$ Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb suppressor when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltage is the sum of a voltage rise due to diode series resistance and an increase in breakdown voltage caused by the junction temperature rise.
- I_{PP} Peak Pulse Current—See Figure 3.
- P_P Peak Pulse Power.
- I_R Reverse Leakage.
- ΔV_C Rise in voltage above the breakdown voltage caused by current flow.

NOTES

1. Part numbers shown are for unidirectional diodes. Add C or CA suffix to specify bidirectional suppressors. SA5.0 through SA6.0A are available as unidirectional only.
2. A TransZorb suppressor is normally selected according to the reverse "Stand-Off Voltage" (V_R) which should be slightly greater than the maximum dc or continuous peak operating voltage level.
3. For bidirectional types having V_R or 10 volts and under, the I_R limit is doubled.
4. For unidirectional diodes $V_{F(max)} = 3.5V$ at I_F = 35A, 1/2 sine wave of 8.33ms pulse width.

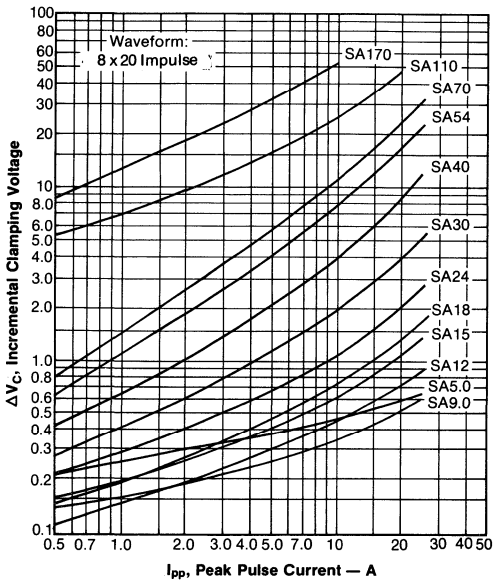
FIGURE 3—Pulse Waveform



CLAMPING VOLTAGE 8 x 20 IMPULSE

$\Delta V_C = V_C - V_{BR}$

FIGURE 4—Unidirectional



CLAMPING VOLTAGE 10 x 1000 IMPULSE

$\Delta V_C = V_C - V_{BR}$

FIGURE 5—Unidirectional

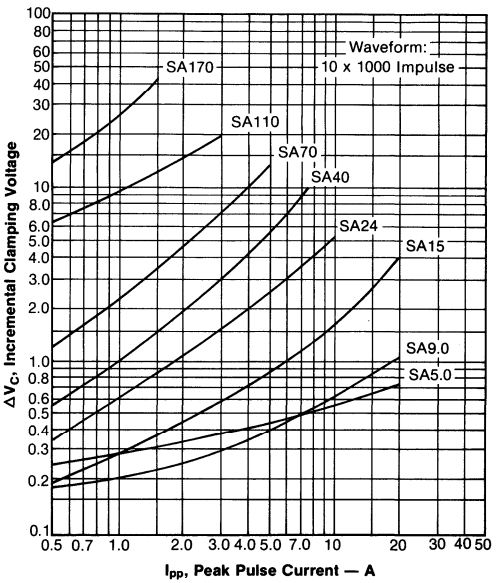


FIGURE 6—Bidirectional

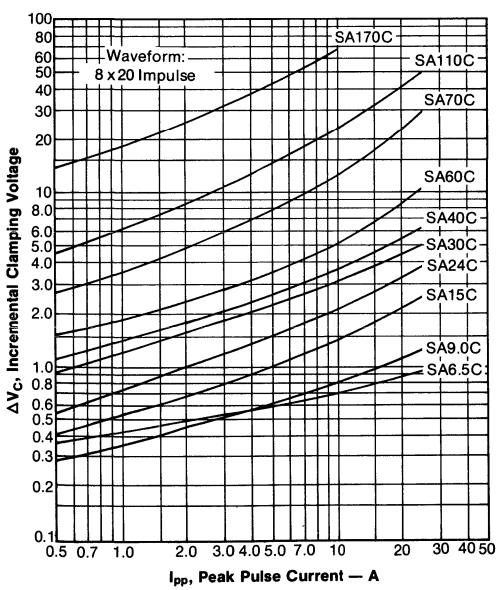
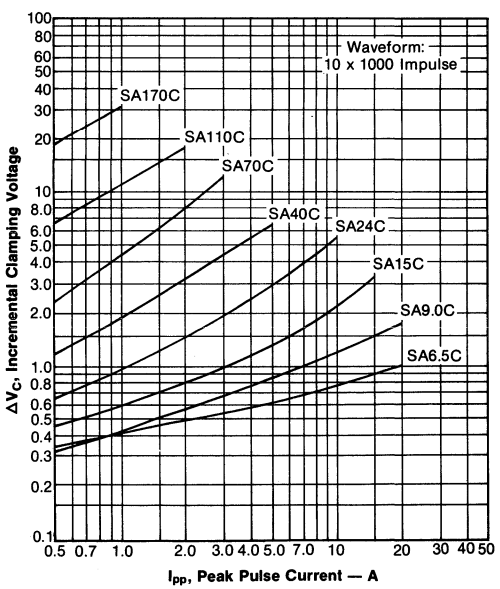


FIGURE 7—Bidirectional



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 8—Capacitance

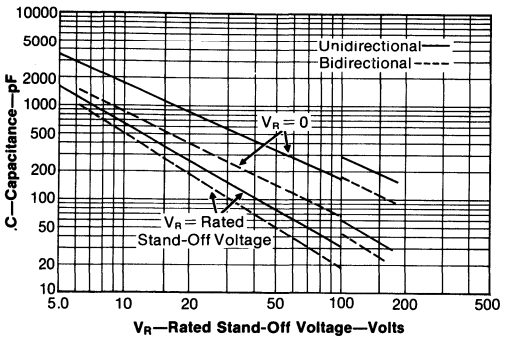


FIGURE 9—Forward Voltage

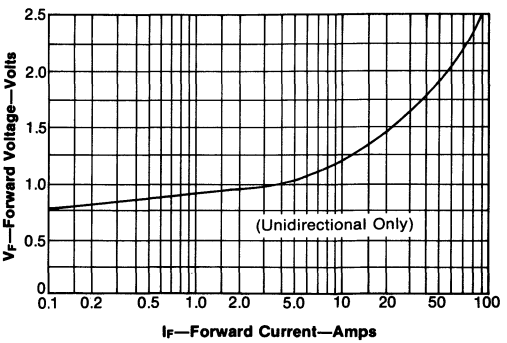


FIGURE 10—Model Parameters

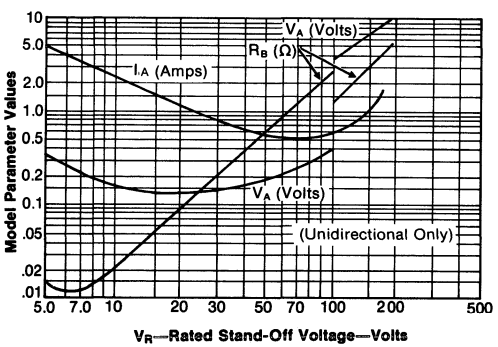


FIGURE 11
Breakdown Voltage Temperature Coefficient

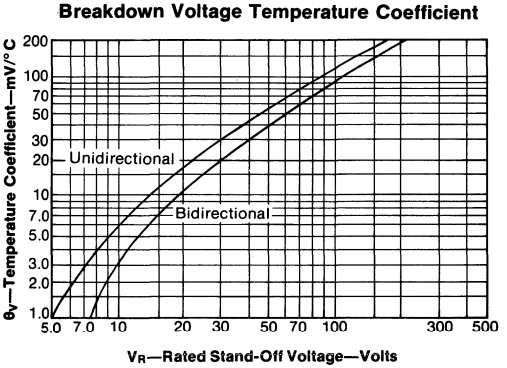
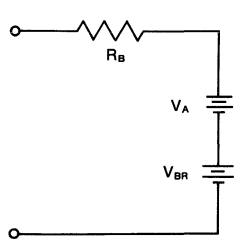


FIGURE 12—High Current Model



Over a restricted current range, TransZorb® diodes may be modeled as shown in the adjoining figure. The battery V_{BR} represents the breakdown voltage, the battery V_A represents the effect of avalanche resistance, and the resistance R_B represents the bulk silicon resistance. At a critical current I_A, the incremental avalanche resistance, which is inversely proportional to current, becomes negligible; its net effect is represented by the battery V_A. The voltage at currents above I_O is obtained by adding a term $R_B \times I_{PP}$ to the sum of the battery voltages. Values for the model parameters are shown on Figure 10. The model is not valid for bidirectional suppressors.

The major effect of temperature is upon the breakdown voltage, V_{BR}. It is adjusted by adding a term $\Theta_V (T_J - 25° C)$. Values for Θ_V are shown in Figure 11; T_J is calculated using standard techniques.

General Semiconductor Industries, Inc.

TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
UNIDIRECTIONAL
SAB5.0 THRU SAB28

FEATURES

- **Voltages from 5.0 to 28V Stand-Off (V_R)**
- **Small package size**
- **Low clamping ratio**

MAXIMUM RATINGS

- 500 Watts of Peak Pulse Power dissipation at 25° C (see derating curve)
- $t_{clamping}$ (0 volts to BV min): Less than 1 x 10^{-12} seconds (theoretical)
- Operating and Storage temperatures: -65° to +175° C
- Forward surge rating: 70 amps, 1/120 second at 25° C
- Steady State power dissipation: 1.0 watt T_L = 75° C, Lead Length = 3/8"
- Repetition rate (duty cycle); .01%

MECHANICAL CHARACTERISTICS

- Molded case
- Weight: 1 gram (approximate)
- Positive terminal marked with band
- Body marked with Logo ✦ and type number

APPLICATION

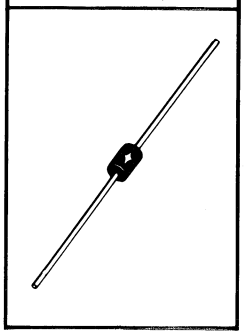
The SAB series is a low cost, 500 watt transient voltage suppressor designed for board level protection of Bipolar and MOS memories, from ESD (Electrostatic Discharge) and other transient voltages.

DESCRIPTION

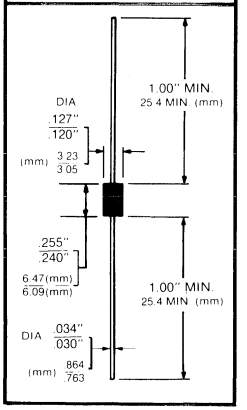
Because of the low clamping factor, these TransZorbs provide a high degree of protection of VMOS, HMOS, and CMOS circuits susceptible to line transients.

TransZorbs are characterized by their high surge capability, extremely fast response time and low series resistance. They are effective in providing protection against pulses generated by electromagnetic switching, electromagnetic coupling, capacitive or inductive load switching, voltage reversals and ESD. MOS circuits are susceptible to damage from these pulses even with various Input Protection Networks.

CASE 25



CASE OUTLINE



Note 1: A TransZorb is normally selected according to the reverse "Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	REVERSE STAND-OFF VOLTAGE V_R VOLTS	MAXIMUM REVERSE LEAKAGE CURRENT I_R @ V_R uA	MINIMUM BREAKDOWN VOLTAGE BV(MIN) @ 1mA VOLTS	MAXIMUM CLAMPING VOLTAGE (FIG. 2) V_C @ 1A VOLTS	TYPICAL CLAMPING VOLTAGE V_C @ 5A VOLTS	TYPICAL CLAMPING VOLTAGE V_C @ 10A VOLTS	MAXIMUM CLAMPING VOLTAGE (FIG. 2) V_C @ I_{pp} VOLTS	MAXIMUM PEAK PULSE CURRENT (FIG. 2) I_{pp} AMPS
SAB5.0	5.0	300	6.0	7.4		7.9	9.3	53.7
SAB10	10.0	3	11.1	13.2		14.4	16.5	30.3
SAB12	12.0	3	13.8	16.5		18.5	21.0	23.8
SAB15	15.0	3	16.7	19.7		22.2	25.2	19.8
SAB18	18.0	3	20.4	23.8	26.0		30.5	16.3
SAB24	24.0	3	28.4	32.4	37.0		42.0	11.9
SAB28	28.0	3	30.7	35.9	41.0		46.5	10.7

FIGURE 1—Peak Pulse Power vs Pulse Time

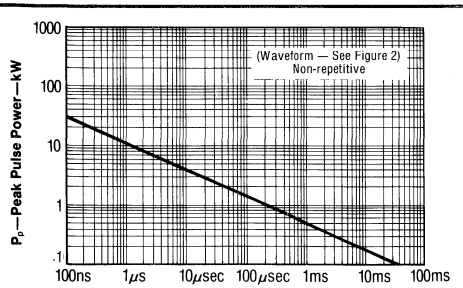
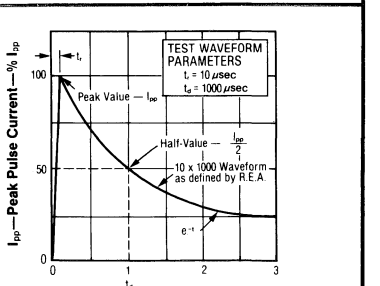


FIGURE 2—Pulse Waveform



General Semiconductor Industries, Inc.

NEW

LOW CAPACITANCE
TRANSZORB®
TRANSIENT VOLTAGE SUPPRESSORS
SAC5.0
THRU
SAC50

MAXIMUM RATINGS

- 500 Watts Peak Pulse Power Dissipation
- $t_{clamping}$ (0 volt to BV min) less than 5.0 Nanoseconds
- Operating and Storage Temp: -65° to +175°C
- Steady State Power Dissipation: 1.0 Watt @ T_C = 75°C; Lead Length = 3/8"

MECHANICAL CHARACTERISTICS

- Molded Case
- Weight: 1.0 Gram (Approximate)
- Polarity band on cathode end of the TransZorb (positive potential applied)
- Body marked with Logo ♦ and type number

ELECTRICAL CHARACTERISTICS

- Clamping Factor: 1.40 at full rated power
  1.30 at 50% rated power

Clamping Factor: The ratio of the actual V_C (Clamping Volatge) to the BV (Breakdown Voltage) as measured on a specific device.
Note: When pulse testing, test in TransZorb TVS avalanche direction. DO NOT pulse in forward direction.

DESCRIPTION

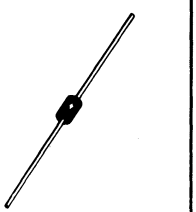
The SAC series is a low capacitance silicon transient voltage suppressor for data or signal lines. It is designed for commercial and industrial applications.This series offers pricing, size, and capacitance advantages over the higher power LCE series. This series employs a standard TransZorb® TVS in series with a rectifier which reduces the effective capacitance up through 70MHz with a minimum amount of signal loss or deformation.

If bidirectional transient protection capability is required, two low capacitance TransZorb TVS must be used in parallel, opposite in polarity for complete AC protection.

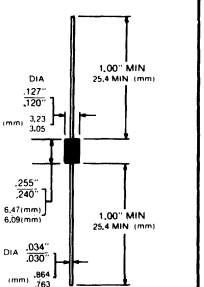
APPLICATIONS

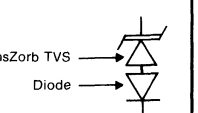
The SAC series of low capacitance silicon transient voltage suppressors, rated at 500 watts, provides board level protection for data or signal lines from the damaging effects of electrostatic discharge (ESD), and electromagnetic pulse (EMP). It will clamp the inductive overshoot voltage caused by very fast impulse rise times. The low capacitance assures minumum signal attenuation.

CASE 25



CASE OUTLINE





Schematic

FIGURE 1—Peak Pulse Power vs Pulse Time

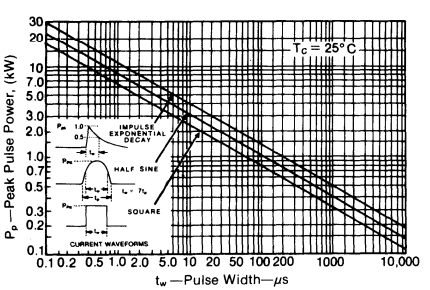
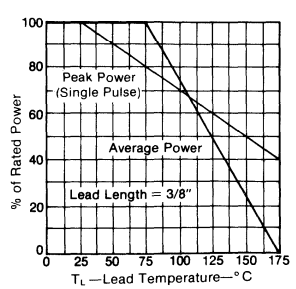


FIGURE 2—Power Derating

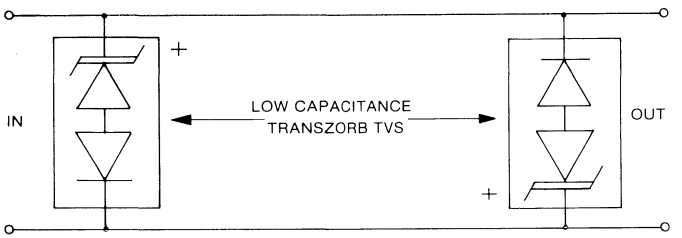


ELECTRICAL CHARACTERISTICS @ 25°C

General Semiconductor Part Number	Reverse Stand-Off Voltage (Note 1) V_R Volts	Breakdown Voltage @ I_T 1.0mA BV Volts Min.	Maximum Reverse Leakage @ V_R I_R uA	Maximum Clamping Voltage* @I_{PP} = 5.0A V_C Volts	Maximum Peak Pulse Current* Rating I_{PP} Amps	Capacitance @ 0 Volts pF	Working Inverse Blocking Voltage V_{WIB} Volts	Inverse Blocking Leakage Current @ V_{WIB} I_{IB} mA	Peak Inverse Blocking Voltage V_{PIB} Volts
SAC5.0	5.0	7.60	300	10.0	44	50	75	1	100
SAC6.0	6.0	7.90	300	11.2	41	50	75	1	100
SAC7.0	7.0	8.33	300	12.6	38	50	75	1	100
SAC8.0	8.0	8.89	100	13.4	36	50	75	1	100
SAC8.5	8.5	9.44	50	14.0	34	50	75	1	100
SAC10	10	11.10	5.0	16.3	29	50	75	1	100
SAC12	12	13.30	5.0	19.0	25	50	75	1	100
SAC15	15	16.70	5.0	23.6	20	50	75	1	100
SAC18	18	20.00	5.0	28.8	15	50	75	1	100
SAC22	22	24.40	5.0	35.4	14	50	75	1	100
SAC26	26	28.90	5.0	42.3	11.1	50	75	1	100
SAC30	30	33.30	5.0	48.6	10.0	50	75	1	100
SAC36	36	40.00	5.0	60.0	8.6	50	75	1	100
SAC45	45	50.00	5.0	77.0	6.8	50	150	1	200
SAC50	50	55.50	5.0	88.0	5.8	50	150	1	200

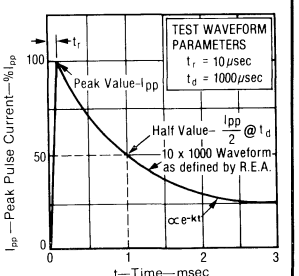
*See Figure 3.

FIGURE 4—AC Line Protection Application



APPLICATION NOTE: Devices must be used with two units in parallel, opposite in polarity, as shown in circuit for AC Signal Line protection.

FIGURE 3—Pulse Waveform



ABBREVIATIONS & SYMBOLS

V_R Stand Off Voltage: Applied Reverse Voltage to assure a nonconductive condition. (See Note 1)

BV(min) This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C (max) Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{PP} Peak Pulse Current

P_P Peak Pulse Power

I_R Reverse Leakage

NOTES

Note 1:
A TransZorb is normally selected according to the reverse "Stand Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

TRANSZORB® UNIDIRECTIONAL & BIDIRECTIONAL
SBL10 THRU SBL100C

FEATURES

- **Voltages from 10.0 to 100V Stand-Off (V_R)**
- **Low cost**
- **Unidirectional or Bidirectional**

MAXIMUM RATINGS

- 700 Watts of Peak Pulse Power dissipation at 25°C (see derating curve)
- $t_{clamping}$ (0 volts to BV min); Less than 1×10^{-2} seconds (Unidirectional)
- Operating and Storage temperatures: -55°C to +175°C
- Forward surge rating: 100 amps, (except Bidirectional)

MECHANICAL CHARACTERISTICS

- Molded case
- Weight: 1.5 grams (approximate)
- Body marked with Logo and type number
- Polarity band (except Bidirectional)

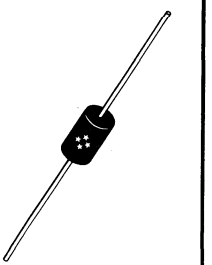
APPLICATION

This TransZorb® has a peak pulse power rating of 700 watts for 1 millisecond. The response time of the TransZorb clamping action is less than (1×10^{-12} seconds) and therefore can be used in applications where induced lightning on rural or remote transmission lines presents a hazard to electronic circuitry. They can also be used to protect Integrated Circuits, MOS devices, hybrids, and other voltage-sensitive semiconductors and components.

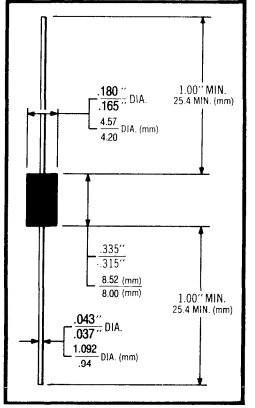
DESCRIPTION

A low cost silicon transient suppressor series specially designed and tested to protect applications in telephone switching where large voltage transients can permanently damage voltage-sensitive components.

CASE 7



CASE OUTLINE



ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER		REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R	BREAKDOWN VOLTAGE BV @ IT = 5mA VOLTS		MAXIMUM CLAMPING VOLTAGE (FIG. 2) V_C @ I_{pp}	MAXIMUM REVERSE LEAKAGE CURRENT I_R @ V_R	MAXIMUM PEAK PULSE CURRENT (FIG. 2) I_{pp}	MAXIMUM TEMPERATURE COEFFICIENT OF BV
UNIPOLAR	BIPOLAR	VOLTS	MIN.	MAX.	VOLTS	uA	AMPS	%/°C
SBL10	**SBL10C**	10	13.0 -	20.0	25	5.0	30	.10
SBL25	**SBL25C**	25	29.6 -	43.5	53	5.0	13	.11
SBL43	**SBL43C**	43	50.0 -	75.0	90	5.0	8	.12
SBL100	**SBL100C**	100	130.0 -	200.0	235	5.0	3	.12

NOTES

Note 1: A TransZorb is normally selected according to the reverse "Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or continuous peak operating voltage level.

FIGURE 1—Peak Pulse Power vs Pulse Time

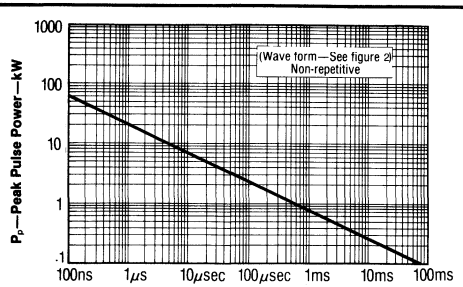
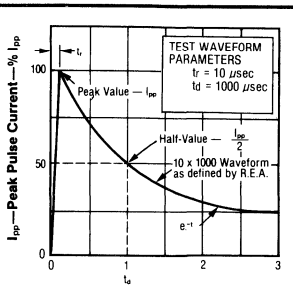


FIGURE 2—Pulse Waveform



General Semiconductor Industries, Inc.

SURFACE MOUNT
TRANSZORB®
SMB SERIES
5.0 THRU 170.0 VOLTS
600 WATTS
UNIDIRECTIONAL

FEATURES

- **600 Watts Peak Power**
- **Voltage Range: 5.0-170 Volts**
- **Low Inductance**
- **JEDEC Registered Low Profile Package for Surface Mounting**

MAXIMUM RATINGS

- 600 watts of Peak Power dissipation (10/1000μs)
- $t_{clamping}$ (0 volts to BV min): less than 1×10^{-12} seconds (theoretical)
- Forward surge rating: 100 Amps, 1/120 sec @ 25°C
- Operating and Storage Temp.: -55° to +150°C

DESCRIPTION

This series of TransZorb® transient voltage suppressors, available in small outline mountable packages, is designed to optimize board space. Packaged for use with surface mount technology automated assembly equipment, these parts can be placed on printed circuit boards and ceramic substrates to protect sensitive components from transient voltage damage.

APPLICATION

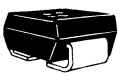
This device is designed specifically for transient voltage suppression. The wide leads assure a large surface contact for good heat dissipation, and a low resistance path for surge current flow to ground.

A 600W (SMB) device is normally selected when the threat of transients is from ESD or board level load switching components. It is also used for protection against lightning induced transients when preceded by a suitable primary protection device (gas discharge arrestor). Source impedance at component level in a system is usually high enough to limit the current to within the peak pulse current (I_{pp}) rating of this series.

MECHANICAL CHARACTERISTICS

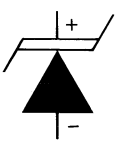
- Molded Surface Mountable Case
- Gull-wing or Modified J-bend leads
- Terminals: Tin/Lead Plated
- Positive end indicated with polarity band
- Body marked with type code (see part list) and Logo
- Standard Packaging: **12 mm tape** (see EIA Std. RS-481)

CASES



Modified J-Bend
Leads (C-Bend)
DO-214AA

Gull-Wing Leads
DO-215AA

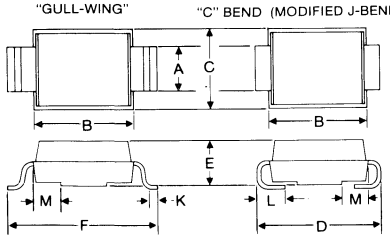


Schematic Symbol

SURFACE MOUNT CASE OUTLINES

DO-215 AA
"GULL-WING"

DO-214 AA
"C" BEND (MODIFIED J-BEND)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.077	.160	.130	.205	.075	.235	.015	.030	.038
MAX	.083	.180	.155	.220	.095	.255	.030	.060	.058
DIMENSIONS IN MILLIMETERS									
MIN	1.96	4.06	3.30	5.21	1.91	5.97	0.38	0.76	0.97
MAX	2.10	4.57	3.81	5.59	2.41	6.48	0.76	1.52	1.47

Typical Standoff Height: 0.004"-0.008" (0.1mm-0.2mm)

FIGURE 3—Derating Curve

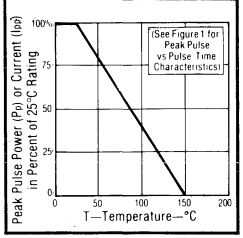


FIGURE 1—Peak Pulse Power vs Pulse Time

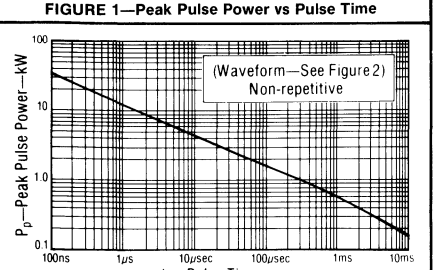


FIGURE 2—Pulse Waveform

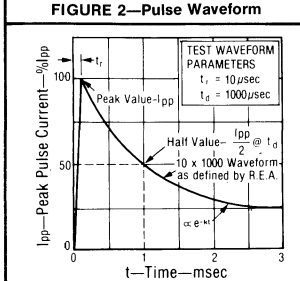
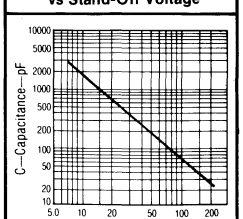


FIGURE 4
Typical Capacitance vs Stand-Off Voltage



ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER		DEVICE MARKING CODE	REVERSE STAND-OFF VOLTAGE (NOTE 1) VR	BREAKDOWN VOLTAGE BV @ IT VOLTS		MAXIMUM CLAMPING VOLTAGE @ Ipp	PEAK PULSE CURRENT (See Fig. 2)	MAXIMUM REVERSE LEAKAGE @ VR
GULL-WING LEAD	MODIFIED "J" BEND LEAD		VOLTS	MIN.	@ IT mA	VOLTS	Ipp AMPS	IR uA
SMBG5.0	SMBJ5.0	KD	5.0	6.40	10	9.6	62.5	800
SMBG5.0A	SMBJ5.0A	KE	5.0	6.40	10	9.2	65.2	800
SMBG6.0	SMBJ6.0	KF	6.0	6.67	10	11.4	52.6	800
SMBG6.0A	SMBJ6.0A	KG	6.0	6.67	10	10.3	58.3	800
SMBG6.5	SMBJ6.5	KH	6.5	7.22	10	12.3	48.7	500
SMBG6.5A	SMBJ6.5A	KK	6.5	7.22	10	11.2	53.6	500
SMBG7.0	SMBJ7.0	KL	7.0	7.78	10	13.3	45.1	200
SMBG7.0A	SMBJ7.0A	KM	7.0	7.78	10	12.0	50.0	200
SMBG7.5	SMBJ7.5	KN	7.5	8.33	1	14.3	42.0	100
SMBG7.5A	SMBJ7.5A	KP	7.5	8.33	1	12.9	46.5	100
SMBG8.0	SMBJ8.0	KQ	8.0	8.89	1	15.0	40.0	50
SMBG8.0A	SMBJ8.0A	KR	8.0	8.89	1	13.6	44.1	50
SMBG8.5	SMBJ8.5	KS	8.5	9.44	1	15.9	37.7	10
SMBG8.5A	SMBJ8.5A	KT	8.5	9.44	1	14.4	41.7	10
SMBG9.0	SMBJ9.0	KU	9.0	10.0	1	16.9	35.5	5
SMBG9.0A	SMBJ9.0A	KV	9.0	10.0	1	15.4	39.0	5
SMBG10	SMBJ10	KW	10	11.1	1	18.8	31.9	5
SMBG10A	SMBJ10A	KX	10	11.1	1	17.0	35.3	5
SMBG11	SMBJ11	KY	11	12.2	1	20.1	29.9	5
SMBG11A	SMBJ11A	KZ	11	12.2	1	18.2	33.0	5
SMBG12	SMBJ12	LD	12	13.3	1	22.0	27.3	5
SMBG12A	SMBJ12A	LE	12	13.3	1	19.9	30.2	5
SMBG13	SMBJ13	LF	13	14.4	1	23.8	25.2	5
SMBG13A	SMBJ13A	LG	13	14.4	1	21.5	27.9	5
SMBG14	SMBJ14	LH	14	15.6	1	25.8	23.3	5
SMBG14A	SMBJ14A	LK	14	15.6	1	23.2	25.8	5
SMBG15	SMBJ15	LL	15	16.7	1	26.9	22.3	5
SMBG15A	SMBJ15A	LM	15	16.7	1	24.4	24.0	5
SMBG16	SMBJ16	LN	16	17.8	1	28.8	20.8	5
SMBG16A	SMBJ16A	LP	16	17.8	1	26.0	23.1	5
SMBG17	SMbJ17	LQ	17	18.9	1	30.5	19.7	5
SMBG17A	SMBJ17A	LR	17	18.9	1	27.6	21.7	5
SMBG18	SMBJ18	LS	18	20.0	1	32.2	18.6	5
SMBG18A	SMBJ18A	LT	18	20.0	1	29.2	20.5	5
SMBG20	SMBJ20	LU	20	22.2	1	35.8	16.7	5
SMBG20A	SMBJ20A	LV	20	22.2	1	32.4	18.5	5
SMBG22	SMBJ22	LW	22	24.4	1	39.4	15.2	5
SMBG22A	SMBJ22A	LX	22	24.4	1	35.5	16.9	5
SMBG24	SMBJ24	LY	24	26.7	1	43.0	14.0	5
SMBG24A	SMBJ24A	LZ	24	26.7	1	38.9	15.4	5
SMBG26	SMBJ26	MD	26	28.9	1	46.6	12.4	5
SMBG26A	SMBJ26A	ME	26	28.9	1	42.1	14.2	5
SMBG28	SMBJ28	MF	28	31.1	1	50.0	12.0	5
SMBG28A	SMBJ28A	MG	28	31.1	1	45.4	13.2	5
SMBG30	SMBJ30	MH	30	33.3	1	53.5	11.2	5
SMBG30A	SMBJ30A	MK	30	33.3	1	48.4	12.4	5
SMBG33	SMBJ33	ML	33	36.7	1	59.0	10.2	5
SMBG33A	SMBJ33A	MM	33	36.7	1	53.3	11.3	5
SMBG36	SMBJ36	MN	36	40.0	1	64.3	9.3	5
SMBG36A	SMBJ36A	MP	36	40.0	1	58.1	10.3	5
SMBG40	SMBJ40	MQ	40	44.4	1	71.4	8.4	5
SMBG40A	SMBJ40A	MR	40	44.4	1	64.5	9.3	5
SMBG43	SMBJ43	MS	43	47.8	1	76.7	7.8	5
SMBG43A	SMBJ43A	MT	43	47.8	1	69.4	8.6	5
SMBG45	SMBJ45	MU	45	50.0	1	80.3	7.5	5
SMBG45A	SMBJ45A	MV	45	50.0	1	72.7	8.3	5
SMBG48	SMBJ48	MW	48	53.3	1	85.5	7.0	5
SMBG48A	SMBJ48A	MX	48	53.3	1	77.4	7.7	5
SMBG51	SMBJ51	MY	51	56.7	1	91.1	6.6	5
SMBG51A	SMBJ51A	MZ	51	56.7	1	82.4	7.3	5
SMBG54	SMBJ54	ND	54	60.0	1	96.3	6.2	5
SMBG54A	SMBJ54A	NE	54	60.0	1	87.1	6.9	5
SMBG58	SMBJ58	NF	58	64.4	1	103.0	5.8	5
SMBG58A	SMBJ58A	NG	58	64.4	1	93.6	6.4	5
SMBG60	SMBJ60	NH	60	66.7	1	107.0	5.6	5
SMBG60A	SMBJ60A	NK	60	66.7	1	96.8	6.2	5
SMBG64	SMBJ64	NL	64	71.1	1	114.0	5.3	5
SMBG64A	SMBJ64A	NM	64	71.1	1	103.0	5.8	5
SMBG70	SMBJ70	NN	70	77.8	1	125	4.8	5
SMBG70A	SMBJ70A	NP	70	77.8	1	113	5.3	5
SMBG75	SMBJ75	NQ	75	83.3	1	134	4.5	5
SMBG75A	SMBJ75A	NR	75	83.3	1	121	4.9	5
SMBG78	SMBJ78	NS	78	86.7	1	139	4.3	5
SMBG78A	SMBJ78A	NT	78	86.7	1	126	4.7	5
SMBG85	SMBJ85	NU	85	94.4	1	151	3.9	5
SMBG85A	SMBJ85A	NV	85	94.4	1	137	4.4	5
SMBG90	SMBJ90	NW	90	100	1	160	3.8	5
SMBG90A	SMBJ90A	NX	90	100	1	146	4.1	5
SMBG100	SMBJ100	NY	100	111	1	179	3.4	5
SMBG100A	SMBJ100A	NZ	100	111	1	162	3.7	5
SMBG110	SMBJ110	PD	110	122	1	196	3.0	5
SMBG110A	SMBJ110A	PE	110	122	1	177	3.4	5
SMBG120	SMBJ120	PF	120	133	1	214	2.8	5
SMBG120A	SMBJ120A	PG	120	133	1	193	3.1	5
SMBG130	SMBJ130	PH	130	144	1	231	2.6	5
SMBG130A	SMBJ130A	PK	130	144	1	209	2.9	5
SMBG150	SMBJ150	PL	150	167	1	268	2.2	5
SMBG150A	SMBJ150A	PM	150	167	1	243	2.5	5
SMBG160	SMBJ160	PN	160	178	1	287	2.1	5
SMBG160A	SMBJ160A	PP	160	178	1	259	2.3	5
SMBG170	SMBJ170	PQ	170	189	1	304	2.0	5
SMBG170A	SMBJ170A	PR	170	189	1	275	2.2	5

TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

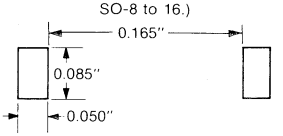
SURFACE MOUNT
TRANSZORB®
SMB SERIES
5.0 THRU 170.0 VOLTS
600 WATTS
UNIDIRECTIONAL

RECOMMENDED PAD SIZES

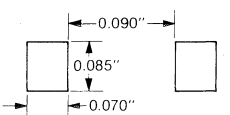
The pad dimensions should be 0.010" longer than the contact size, in the lead axis. This allows a solder fillet to form, see figure below.

Contact factory for soldering methods.

GULL-WING
(Pad distances equal layout for SO-8 to 16.)



MODIFIED J-BEND



ABBREVIATIONS & SYMBOLS

V_R	Stand Off Voltage: Applied Reverse Voltage to assure a non-conductive condition. (See Note 1)
BV (min)	This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25 C
V_C	Maximum Clamping Voltage The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
I_{PP}	Peak Pulse Current - See Figure 2
P_P	Peak Pulse Power
I_R	Reverse Leakage

NOTES

Note 1:
A TransZorb TVS is normally selected according to the reverse "Stand Off Voltage" (VR) which should be equal to or greater than the DC or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

NEW

SURFACE MOUNT
TRANSZORB® TVS
SMB SERIES
6.5 THRU 43 VOLTS
600 WATTS
BIDIRECTIONAL

FEATURES

- **600 watts peak power**
- **Low Inductance**
- **Voltage range: 6.5 to 43 volts**
- **JEDEC Registered Package Outline**

MECHANICAL CHARACTERISTICS

- Epoxy Molded Surface Mountable Case
- Gull-wing or Modified J-bend leads (C-bend)
- Terminals: Tin/Lead Plated
- Body marked with type code (see table) and Logo
- Standard Packaging: **12mm tape** (see EIA Std. RS-481)

DESCRIPTION

This series of TransZorb® transient voltage suppressors, available in small outline surface mountable packages, is designed to optimize board space. Packaged for use with surface mount technology automated assembly equipment, these parts can be placed on printed circuit boards and ceramic substrates to protect sensitive components from transient voltage damage.

APPLICATIONS

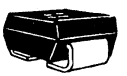
General Semiconductor Industries' surface mountable packages are desigend specifically for transient voltage suppression. The wide leads assure a large surface contact for good heat dissipation, and a low resistance path for surge current flow to ground. These high speed transient voltage suppressors can be used to effectively protect sensitive components such as integrated circuits and MOS devices.

A 600W (SMB) device is normally selected when the threat of transients is from lightning-induced transients conducted via external leads or I/O lines. It is also used to protect against switching transients induced by large coils or industrial motors. System impedance at component level in a system is usually high enough to limit the current to within the peak pulse current (Ipp) rating of this series. In an overstress condition, the failure mode is a short circuit.

MAXIMUM RATINGS

- 600 watts of Peak Power dissipation (10/1000μs)
- $t_{clamping}$ (0 volts to BV min): less than 1×10^{-12} seconds (theoretical)
- Operating and Storage Temperature: -55° to +150°C

CASES



Modified J-Bend Leads (C-Bend) DO-214AA

Gull-Wing Leads DO-215AA

Schematic Symbol

FIGURE 1—Peak Pulse Power vs Pulse Time

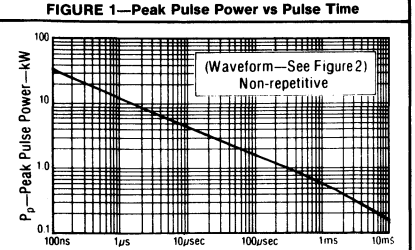


FIGURE 2—Pulse Waveform

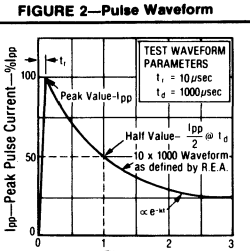
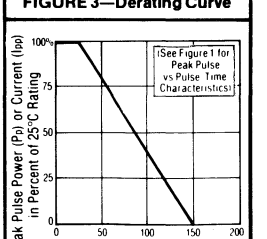


FIGURE 3—Derating Curve



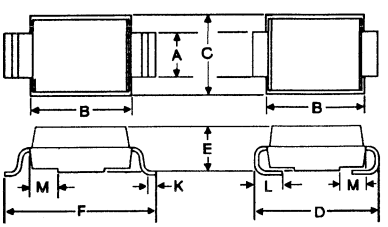
ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER		DEVICE MARKING CODE	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R VOLTS	BREAKDOWN VOLTAGE B_V @ I_T VOLTS		MAXIMUM CLAMPING VOLTAGE @ Ipp VOLTS	PEAK PULSE CURRENT (See Fig. 2) Ipp AMPS	MAXIMUM REVERSE LEAKAGE @ V_R I_R µA
GULL-WING LEAD	MODIFIED J-BEND			MIN.	I_T mA			
SMBG6.5C	SMBJ6.5C	AH	6.5	7.22	10	12.3	48.7	1000
SMBG6.5CA	SMBJ6.5CA	AK	6.5	7.22	10	11.2	53.6	1000
SMBG7.5C	SMBJ7.5C	AN	7.5	8.33	1	14.3	42.0	200
SMBG7.5CA	SMBJ7.5CA	AP	7.5	8.33	1	12.9	46.5	200
SMBG8.0C	SMBJ8.0C	AQ	8.0	8.89	1	15.0	40.0	100
SMBG8.0CA	SMBJ8.0CA	AR	8.0	8.89	1	13.6	44.1	100
SMBG8.5C	SMBJ8.5C	AS	8.5	9.44	1	15.9	37.7	20
SMBG8.5CA	SMBJ8.5CA	AT	8.5	9.44	1	14.4	41.7	20
SMBG9.0C	SMBJ9.0C	AU	9.0	10.0	1	16.9	35.5	10
SMBG9.0CA	SMBJ9.0CA	AV	9.0	10.0	1	15.4	39.0	10
SMBG10C	SMBJ10C	AW	10	11.1	1	18.8	31.9	10
SMBG10CA	SMBJ10CA	AX	10	11.1	1	17.0	35.3	10
SMBG12C	SMBJ12C	BD	12	13.3	1	22.0	27.3	5
SMBG12CA	SMBJ12CA	BE	12	13.3	1	19.9	30.2	5
SMBG14C	SMBJ14C	BH	14	15.6	1	25.8	23.3	5
SMBG14CA	SMBJ14CA	BK	14	15.6	1	23.2	25.8	5
SMBG15C	SMBJ15C	BL	15	16.7	1	26.9	22.3	5
SMBG15CA	SMBJ15CA	BM	15	16.7	1	24.4	24.0	5
SMBG18C	SMBJ18C	BS	18	20.0	1	32.2	18.6	5
SMBG18CA	SMBJ18CA	BT	18	20.0	1	29.2	20.5	5
SMBG22C	SMBJ22C	BW	22	24.4	1	39.4	15.2	5
SMBG22CA	SMBJ22CA	BX	22	24.4	1	35.5	16.9	5
SMBG24C	SMBJ24C	BY	24	26.7	1	43.0	14.0	5
SMBG24CA	SMBJ24CA	BZ	24	26.7	1	38.9	15.4	5
SMBG26C	SMBJ26C	CD	26	28.9	1	46.6	12.4	5
SMBG26CA	SMBJ26CA	CE	26	28.9	1	42.1	14.2	5
SMBG30C	SMBJ30C	CH	30	33.3	1	53.5	11.2	5
SMBG30CA	SMBJ30CA	CK	30	33.3	1	48.4	12.4	5
SMBG33C	SMBJ33C	CL	33	36.7	1	59.0	10.2	5
SMBG33CA	SMBJ33CA	CM	33	36.7	1	53.3	11.3	5
SMBG36C	SMBJ36C	CN	36	40.0	1	64.3	9.3	5
SMBG36CA	SMBJ36CA	CP	36	40.0	1	58.1	10.3	5
SMBG40C	SMBJ40C	CQ	40	44.4	1	71.4	8.4	5
SMBG40CA	SMBJ40CA	CR	40	44.4	1	64.5	9.3	5
SMBG43C	SMBJ43C	CS	43	47.8	1	76.7	7.8	5
SMBG43CA	SMBJ43CA	CT	43	47.8	1	69.4	8.6	5

CASE OUTLINES

DO-215AA
"GULL-WING"

DO-214AA
"C" BEND (MODIFIED J-BEND)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.077	.160	.130	.205	.075	.235	.015	.030	.038
MAX	.083	.180	.155	.220	.095	.255	.030	.060	.058
DIMENSIONS IN MILLIMETERS									
MIN	1.96	4.06	3.30	5.21	1.91	5.97	0.38	0.76	0.97
MAX	2.10	4.57	3.81	5.59	2.41	6.48	0.76	1.52	1.47

Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

Components Packaging: Standard 12mm tape.

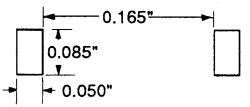
SURFACE MOUNT
TRANSZORB® TVS
SMB SERIES
6.5 THRU 43 VOLTS
600 WATTS
BIDIRECTIONAL

RECOMMENDED PAD SIZES

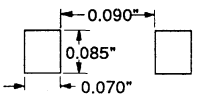
The pad dimensions should be 0.010" longer than the contact size in the lead axis. This allows a solder fillet to form, see figure below.

Contact factory for soldering methods.

GULL-WING
(Pad distances equal layout for SO-8 to 16.)



MODIFIED J-BEND



ABBREVIATIONS & SYMBOLS

V_R Stand Off Voltage: Applied Reverse Voltage to assure a non-conductive condition. (See Note 1)

$BV_{(min)}$ This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb® TVS when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} Peak Pulse Current - See Figure 2.

P_{pp} Peak Pulse Power

I_R Reverse Leakage

NOTES

Note 1:
A TransZorb TVS is normally selected according to the reverse "Stand Off Voltage" (VR) which should be equal to or greater than the dc or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

SURFACE MOUNT
TRANSZORB®
SMC SERIES
5.0 THRU 170.0 VOLTS
1500 WATTS
UNIDIRECTIONAL

FEATURES

- **1500 Watts Peak Power**
- **Voltage Range: 5.0-170 Volts**
- **Low Inductance**
- **JEDEC Registered Low Profile Package for Surface Mounting**

MAXIMUM RATINGS

- 1500 watts of Peak Power dissipation (10/1000μs)
- $t_{clamping}$ (0 volts to BV min): less than 1 x 10^{-12} seconds (theoretical)
- Forward surge rating: 100 Amps, 1/120 sec @ 25°C
- Operating and Storage Temp.: -55° to +150°C

DESCRIPTION

This series of TransZorb® transient voltage suppressors, available in small outline mountable packages, is designed to optimize board space. Packaged for use with surface mount technology automated assembly equipment, these parts can be placed on printed circuit boards and ceramic substrates to protect sensitive components from transient voltage damage.

APPLICATION

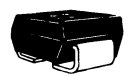
This device is designed specifically for transient voltage suppression. The wide leads assure a large surface contact for good heat dissipation, and a low resistance path for surge current flow to ground.

A 1500W (SMC) device is normally selected when the threat of transients is from lightning induced transients, conducted via external leads or I/O lines. It is also used to protect against switching transients induced by large coils or industrial motors. Source impedance at component level in a system is usually high enough to limit the current within the peak pulse current (Ipp) rating of this series.

MECHANICAL CHARACTERISTICS

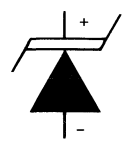
- Molded Surface Mountable Case
- Gull-wing or Modified J-bend leads
- Terminals: Tin/Lead Plated
- Positive end indicated by polarity band
- Body marked with type code (see part list) and Logo
- Standard Packaging: **16 mm tape** (see EIA Std. RS-481)

CASES



Modified J-Bend
Leads (C-Bend)
DO-214AB

Gull-Wing Leads
DO-215AB

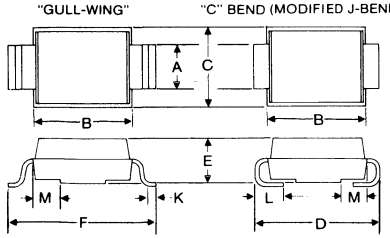


Schematic Symbol

SURFACE MOUNT CASE OUTLINES

DO-215 AB
"GULL-WING"

DO-214 AB
"C" BEND (MODIFIED J-BEND)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.115	.260	.225	.305	.075	.380	.025	.030	.038
MAX	.121	.280	.245	.320	.095	.400	.040	.060	.053
DIMENSIONS IN MILLIMETERS									
MIN	2.92	6.60	5.72	7.75	1.91	9.65	0.64	0.76	0.97
MAX	3.07	7.11	6.22	8.13	2.41	10.16	1.02	1.52	1.35

Typical Standoff Height: 0.004"-0.008" (0.1mm-0.2mm)

FIGURE 3—Derating Curve

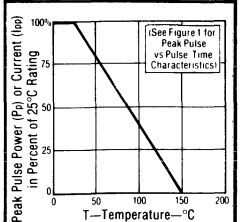


FIGURE 1—Peak Pulse Power vs Pulse Time

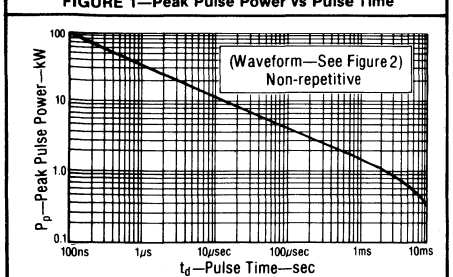


FIGURE 2—Pulse Waveform

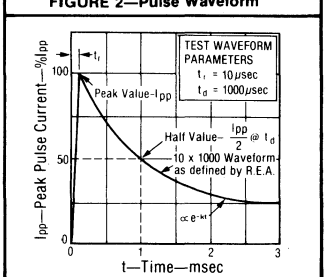
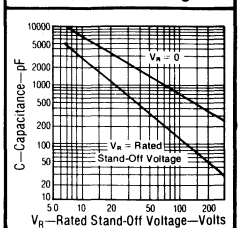


FIGURE 4
Typical Capacitance vs Stand-Off Voltage



SURFACE MOUNT
TRANSZORB®
SMC SERIES
5.0 THRU 170.0 VOLTS
1500 WATTS
UNIDIRECTIONAL

ELECTRICAL CHARACTERISTICS @ 25°C

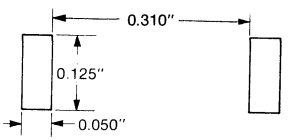
GENERAL SEMICONDUCTOR PART NUMBER		DEVICE MARKING CODE	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R	BREAKDOWN VOLTAGE BV @ IT VOLTS		MAXIMUM CLAMPING VOLTAGE @ Ipp	PEAK PULSE CURRENT (See Fig. 2)	MAXIMUM REVERSE LEAKAGE @ V_R
GULL-WING LEAD	MODIFIED "J" BEND LEAD		VOLTS	MIN.	@ IT mA	VOLTS	Ipp AMPS	IR uA
SMCG5.0	SMCJ5.0	GDD	5.0	6.40	10	9.6	156.2	1000
SMCG5.0A	SMCJ5.0A	GDE	5.0	6.40	10	9.2	163.0	1000
SMCG6.0	SMCJ6.0	GDF	6.0	6.67	10	11.4	131.6	1000
SMCG6.0A	SMCJ6.0A	GDG	6.0	6.67	10	10.3	145.6	1000
SMCG6.5	SMCJ6.5	GDH	6.5	7.22	10	12.3	122.0	500
SMCG6.5A	SMCJ6.5A	GDK	6.5	7.22	10	11.2	133.9	500
SMCG7.0	SMCJ7.0	GDL	7.0	7.78	10	13.3	112.8	200
SMCG7.0A	SMCJ7.0A	GDM	7.0	7.78	10	12.0	125.0	200
SMCG7.5	SMCJ7.5	GDN	7.5	8.33	1	14.3	104.9	100
SMCG7.5A	SMCJ7.5A	GDP	7.5	8.33	1	12.9	116.3	100
SMCG8.0	SMCJ8.0	GDQ	8.0	8.89	1	15.0	100.0	50
SMCG8.0A	SMCJ8.0A	GDR	8.0	8.89	1	13.6	110.3	50
SMCG8.5	SMCJ8.5	GDS	8.5	9.44	1	15.9	94.3	25
SMCG8.5A	SMCJ8.5A	GDT	8.5	9.44	1	14.4	104.2	20
SMCG9.0	SMCJ9.0	GDU	9.0	10.0	1	16.9	88.7	10
SMCG9.0A	SMCJ9.0A	GDV	9.0	10.0	1	15.4	97.4	10
SMCG10	SMCJ10	GDW	10	11.1	1	18.8	79.8	5
SMCG10A	SMCJ10A	GDX	10	11.1	1	17.0	88.2	5
SMCG11	SMCJ11	GDY	11	12.2	1	20.1	74.6	5
SMCG11A	SMCJ11A	GDZ	11	12.2	1	18.2	82.4	5
SMCG12	SMCJ12	GED	12	13.3	1	22.0	68.2	5
SMCG12A	SMCJ12A	GEE	12	13.3	1	19.9	75.3	5
SMCG13	SMCJ13	GEF	13	14.4	1	23.8	63.0	5
SMCG13A	SMCJ13A	GEG	13	14.4	1	21.5	69.7	5
SMCG14	SMCJ14	GEH	14	15.6	1	25.8	58.1	5
SMCG14A	SMCJ14A	GEK	14	15.6	1	23.2	64.7	5
SMCG15	SMCJ15	GEL	15	16.7	1	26.9	55.8	5
SMCG15A	SMCJ15A	GEM	15	16.7	1	24.4	61.5	5
SMCG16	SMCJ16	GEN	16	17.8	1	28.8	52.1	5
SMCG16A	SMCJ16A	GEP	16	17.8	1	26.0	57.7	5
SMCG17	SMCJ17	GEQ	17	18.9	1	30.5	49.2	5
SMCG17A	SMCJ17A	GER	17	18.9	1	27.6	53.3	5
SMCG18	SMCJ18	GES	18	20.0	1	32.2	46.6	5
SMCG18A	SMCJ18A	GET	18	20.0	1	29.2	51.4	5
SMCG20	SMCJ20	GEU	20	22.2	1	35.8	41.9	5
SMCG20A	SMCJ20A	GEV	20	22.2	1	32.4	46.3	5
SMCG22	SMCJ22	GEW	22	24.4	1	39.4	38.1	5
SMCG22A	SMCJ22A	GEX	22	24.4	1	35.5	42.2	5
SMCG24	SMCJ24	GEY	24	26.7	1	43.0	34.9	5
SMCG24A	SMCJ24A	GEZ	24	26.7	1	38.9	38.6	5
SMCG26	SMCJ26	GFD	26	28.9	1	46.6	32.2	5
SMCG26A	SMCJ26A	GFE	26	28.9	1	42.1	35.6	5
SMCG28	SMCJ28	GFF	28	31.1	1	50.0	30.0	5
SMCG28A	SMCJ28A	GFG	28	31.1	1	45.4	33.0	5
SMCG30	SMCJ30	GFH	30	33.3	1	53.5	28.0	5
SMCG30A	SMCJ30A	GFK	30	33.3	1	48.4	31.0	5
SMCG33	SMCJ33	GFL	33	36.7	1	59.0	25.2	5
SMCG33A	SMCJ33A	GFM	33	36.7	1	53.3	28.1	5
SMCG36	SMCJ36	GFN	36	40.0	1	64.3	23.3	5
SMCG36A	SMCJ36A	GFP	36	40.0	1	58.1	25.8	5
SMCG40	SMCJ40	GFQ	40	44.4	1	71.4	21.0	5
SMCG40A	SMCJ40A	GFR	40	44.4	1	64.5	32.2	5
SMCG43	SMCJ43	GFS	43	47.8	1	76.7	19.6	5
SMCG43A	SMCJ43A	GFT	43	47.8	1	69.4	21.6	5
SMCG45	SMCJ45	GFU	45	50.0	1	80.3	18.7	5
SMCG45A	SMCJ45A	GFV	45	50.0	1	72.7	20.6	5
SMCG48	SMCJ48	GFW	48	53.3	1	85.5	17.5	5
SMCG48A	SMCJ48A	GFX	48	53.3	1	77.4	19.4	5
SMCG51	SMCJ51	GFY	51	56.7	1	91.1	18.5	5
SMCG51A	SMCJ51A	GFZ	51	56.7	1	82.4	18.2	5
SMCG54	SMCJ54	GGD	54	60.0	1	96.3	15.6	5
SMCG54A	SMCJ54A	GGE	54	60.0	1	87.1	17.2	5
SMCG58	SMCJ58	GGF	58	64.4	1	103.0	14.6	5
SMCG58A	SMCJ58A	GGG	58	64.4	1	93.6	16.0	5
SMCG60	SMCJ60	GGH	60	66.7	1	107.0	14.0	5
SMCG60A	SMCJ60A	GGK	60	66.7	1	96.8	15.5	5
SMCG64	SMCJ64	GGL	64	71.1	1	114.0	13.2	5
SMCG64A	SMCJ64A	GGM	64	71.1	1	103.0	14.6	5
SMCG70	SMCJ70	GGN	70	77.8	1	125	12.0	5
SMCG70A	SMCJ70A	GGP	70	77.8	1	113	13.3	5
SMCG75	SMCJ75	GGQ	75	83.3	1	134	11.2	5
SMCG75A	SMCJ75A	GGR	75	83.3	1	121	12.4	5
SMCG78	SMCJ78	GGS	78	86.7	1	139	10.8	5
SMCG78A	SMCJ78A	GGT	78	86.7	1	126	11.4	5
SMCG85	SMCJ85	GGU	85	94.4	1	151	9.9	5
SMCG85A	SMCJ85A	GGV	85	94.4	1	137	10.4	5
SMCG90	SMCJ90	GGW	90	100	1	160	9.4	5
SMCG90A	SMCJ90A	GGX	90	100	1	146	10.3	5
SMCG100	SMCJ100	GGY	100	111	1	179	8.4	5
SMCG100A	SMCJ100A	GGZ	100	111	1	162	9.3	5
SMCG110	SMCJ110	GHD	110	122	1	196	7.7	5
SMCG110A	SMCJ110A	GHE	110	122	1	177	8.4	5
SMCG120	SMCJ120	GHF	120	133	1	214	7.0	5
SMCG120A	SMCJ120A	GHG	120	133	1	193	7.9	5
SMCG130	SMCJ130	GHH	130	144	1	231	6.5	5
SMCG130A	SMCJ130A	GHK	130	144	1	209	7.2	5
SMCG150	SMCJ150	GHL	150	167	1	268	5.6	5
SMCG150A	SMCJ150A	GHM	150	167	1	243	6.2	5
SMCG160	SMCJ160	GHN	160	178	1	287	5.2	5
SMCG160A	SMCJ160A	GHP	160	178	1	259	5.8	5
SMCG170	SMCJ170	GHQ	170	189	1	304	4.9	5
SMCG170A	SMCJ170A	GHR	170	189	1	275	5.5	5

RECOMMENDED PAD SIZES

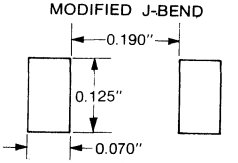
The pad dimensions should be 0.010" longer than the contact size, in the lead axis. This allows a solder fillet to form, see figure below.

Contact factory for soldering methods.

GULL-WING
(Pad distances equal layout for SO-28.)



MODIFIED J-BEND



ABBREVIATIONS & SYMBOLS

V_R	Stand Off Voltage: Applied Reverse Voltage to assure a non-conductive condition. (See Note 1)
BV (min)	This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.
V_C	Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.
I_{PP}	Peak Pulse Current - See Figure 2
P_P	Peak Pulse Power
I_R	Reverse Leakage

NOTES

Note 1:
A TransZorb TVS is normally selected according to the reverse "Stand Off Voltage" (VR) which should be equal to or greater than the DC or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

NEW

SURFACE MOUNT
TRANSZORB® TVS
SMC SERIES
6.5 THRU 43 VOLTS
1500 WATTS
BIDIRECTIONAL

FEATURES

- **1500 watts peak power**
- **Low Inductance**
- **Voltage range: 6.5 to 43 volts**
- **JEDEC Registered Package Outline**

MECHANICAL CHARACTERISTICS

- Epoxy Molded Surface Mountable Case
- Gull-wing or Modified J-bend leads (C-bend)
- Terminals: Tin/Lead Plated
- Body marked with type code (see table) and Logo
- Standard Packaging: **16mm tape** (see EIA Std. RS-481)

DESCRIPTION

This series of TransZorb® transient voltage suppressors, available in small outline surface mountable packages, is designed to optimize board space. Packaged for use with surface mount technology automated assembly equipment, these parts can be placed on printed circuit boards and ceramic substrates to protect sensitive components from transient voltage damage.

APPLICATIONS

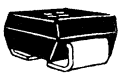
General Semiconductor Industries' surface mountable packages are desigend specifically for transient voltage suppression. The wide leads assure a large surface contact for good heat dissipation, and a low resistance path for surge current flow to ground. These high speed transient voltage suppressors can be used to effectively protect sensitive components such as integrated circuits and MOS devices.

A 1500W (SMC) device is normally selected when the threat of transients is from lightning-induced transients conducted via external leads or I/O lines. It is also used to protect against switching transients induced by large coils or industrial motors. System impedance at component level in a system is usually high enough to limit the current to within the peak pulse current (Ipp) rating of this series. In an overstress condition, the failure mode is a short circuit.

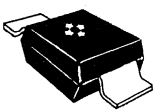
MAXIMUM RATINGS

- 1500 watts of Peak Power dissipation (10/1000µs)
- $t_{clamping}$ (0 volts to BV min): less than 1×10^{-12} seconds (theoretical)
- Operating and Storage Temperature: -55° to +150°C

CASES



Modified J-Bend
Leads (C-Bend)
DO-214AB



Gull-Wing Leads
DO-215AB

Schematic Symbol

FIGURE 1—Peak Pulse Power vs Pulse Time

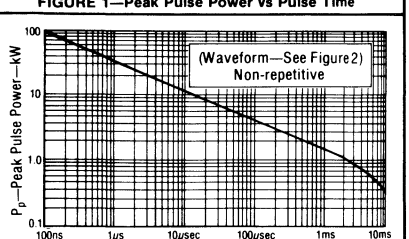


FIGURE 2—Pulse Waveform

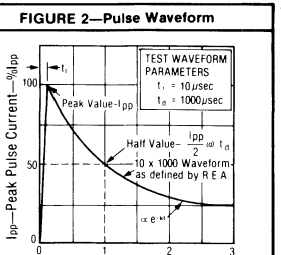
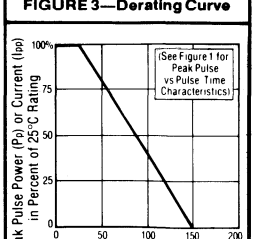


FIGURE 3—Derating Curve



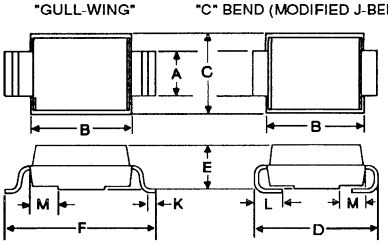
ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER		DEVICE MARKING CODE	REVERSE STAND-OFF VOLTAGE (NOTE 1) V_R	BREAKDOWN VOLTAGE B_v @ I_T		MAXIMUM CLAMPING VOLTAGE @ Ipp	PEAK PULSE CURRENT (See Fig. 2) Ipp	MAXIMUM REVERSE LEAKAGE @ V_R I_R
GULL-WING LEAD	MODIFIED J-BEND		VOLTS	MIN. VOLTS	I_T mA	VOLTS	AMPS	μA
SMCG6.5C	SMCJ6.5C	BDH	6.5	7.22	10	12.3	122.0	1000
SMCG6.5CA	SMCJ6.5CA	BDK	6.5	7.22	10	11.2	133.9	1000
SMCG7.5C	SMCJ7.5C	BDN	7.5	8.33	1	14.3	104.9	200
SMCG7.5CA	SMCJ7.5CA	BDP	7.5	8.33	1	12.9	116.3	200
SMCG8.0C	SMCJ8.0C	BDQ	8.0	8.89	1	15.0	100.0	100
SMCG8.0CA	SMCJ8.0CA	BDR	8.0	8.89	1	13.6	110.3	100
SMCG8.5C	SMCJ8.5C	BDS	8.5	9.44	1	15.9	94.3	50
SMCG8.5CA	SMCJ8.5CA	BDT	8.5	9.44	1	14.4	104.2	50
SMCG9.0C	SMCJ9.0C	BDU	9.0	10.0	1	16.9	88.7	20
SMCG9.0CA	SMCJ9.0CA	BDV	9.0	10.0	1	15.4	97.4	20
SMCG10C	SMCJ10C	BDW	10	11.1	1	18.8	79.8	10
SMCG10CA	SMCJ10CA	BDX	10	11.1	1	17.0	88.2	10
SMCG12C	SMCJ12C	BED	12	13.3	1	22.0	68.2	5
SMCG12CA	SMCJ12CA	BEE	12	13.3	1	19.9	75.3	5
SMCG14C	SMCJ14C	BEH	14	15.6	1	25.8	58.1	5
SMCG14CA	SMCJ14CA	BEK	14	15.6	1	23.2	64.7	5
SMCG15C	SMCJ15C	BEL	15	16.7	1	26.9	55.8	5
SMCG15CA	SMCJ15CA	BEM	15	16.7	1	24.4	61.5	5
SMCG18C	SMCJ18C	BES	18	20.0	1	32.2	46.6	5
SMCG18CA	SMCJ18CA	BET	18	20.0	1	29.2	51.4	5
SMCG22C	SMCJ22C	BEW	22	24.4	1	39.4	38.1	5
SMCG22CA	SMCJ22CA	BEX	22	24.4	1	35.5	42.2	5
SMCG24C	SMCJ24C	BEY	24	26.7	1	43.0	34.9	5
SMCG24CA	SMCJ24CA	BEZ	24	26.7	1	38.9	38.6	5
SMCG26C	SMCJ26C	BFD	26	28.9	1	46.6	32.2	5
SMCG26CA	SMCJ26CA	BFE	26	28.9	1	42.1	35.6	5
SMCG30C	SMCJ30C	BFH	30	33.3	1	53.5	28.0	5
SMCG30CA	SMCJ30CA	BFK	30	33.3	1	48.4	31.0	5
SMCG33C	SMCJ33C	BFL	33	36.7	1	59.0	25.2	5
SMCG33CA	SMCJ33CA	BFM	33	36.7	1	53.3	28.1	5
SMCG36C	SMCJ36C	BFN	36	40.0	1	64.3	23.3	5
SMCG36CA	SMCJ36CA	BFP	36	40.0	1	58.1	25.8	5
SMCG40C	SMCJ40C	BFQ	40	44.4	1	71.4	21.0	5
SMCG40CA	SMCJ40CA	BFR	40	44.4	1	64.5	23.2	5
SMCG43C	SMCJ43C	BFS	43	47.8	1	76.7	19.6	5
SMCG43CA	SMCJ43CA	BFT	43	47.8	1	69.4	21.6	5

CASE OUTLINES

DO-215AB "GULL-WING"

DO-214AB "C" BEND (MODIFIED J-BEND)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.115	.260	.225	.305	.075	.380	.025	.030	.038
MAX	.121	.280	.245	.320	.095	.255	.400	.060	.053
DIMENSIONS IN MILLIMETERS									
MIN	2.92	6.60	5.72	7.75	1.91	9.65	0.64	0.76	0.97
MAX	3.07	7.11	6.22	8.13	2.41	10.16	1.02	1.52	1.35

Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

Components Packaging: Standard 16mm tape.

SURFACE MOUNT TRANSZORB® TVS SMC SERIES

6.5 THRU 43 VOLTS 1500 WATTS BIDIRECTIONAL

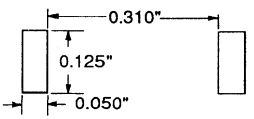
RECOMMENDED PAD SIZES

The pad dimensions should be 0.010" longer than the contact size in the lead axis. This allows a solder fillet to form, see figure below.

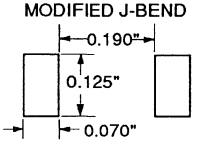
Contact factory for soldering methods.

GULL-WING

(Pad distances equal layout for SO-28.)



MODIFIED J-BEND



ABBREVIATIONS & SYMBOLS

V_R Stand Off Voltage: Applied Reverse Voltage to assure a non-conductive condition. (See Note 1)

$BV_{(min)}$ This is the minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C Maximum Clamping Voltage. The maximum peak voltage appearing across the TransZorb® TVS when subjected to the peak pulse current in a one millisecond time interval. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{PP} Peak Pulse Current - See Figure 2.

P_P Peak Pulse Power

I_R Reverse Leakage

NOTES

Note 1:
A TransZorb TVS is normally selected according to the reverse "Stand Off Voltage" (VR) which should be equal to or greater than the dc or continuous peak operating voltage level.

General Semiconductor Industries, Inc.

NEW

SURFACE MOUNT DIODE ARRAY TRANSZORB® TVS 8 PIN UNIDIRECTIONAL & BIDIRECTIONAL 5.0 THRU 24 VOLTS

FEATURES

- **300 watts peak pulse power**
- **Data and Bus Line Applications**
- **Unidirectional & Bidirectional**
- **Standard SO-8 package**

MAXIMUM RATINGS

- Peak Pulse Power (8/20μs): 300 watts
- Operating and Storage Temperature Range: -55°C to +150°C
- Repetition Rate (duty cycle): 01%

MECHANICAL CHARACTERISTICS

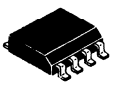
- Molded SO-8 Surface Mount
- Terminals: Solder dipped
- Body marked with device code and logo
- Pin No. 1 marked with dot on top of package
- Unidirectional cathode on bevelled side of device

DESCRIPTION

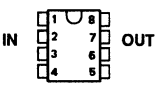
This family of TransZorb® TVS diode arrays are designed for surface mount applications such as smart cards, cameras and other electronic circuitry which require multiple protection with limited board space. These are available as unidirectional or bidirectional devices employing TransZorb TVS technology. They can provide board level protection for TTL and MOS logic circuits against every form of ESD threat.

These devices are best used at the board interface on all I/O ports and power input bus lines. For best results, separate units are required for data lines and power bus lines. If subjected to a transient current beyond their peak pulse capability, the units will either short or open circuit. The low profile package is designed to minimize lead inductance without sacrificing maximum transient current handling capability.

CASE



(TOP VIEW)



SO-8

ABBREVIATIONS & SYMBOLS

V_D **Stand Off Voltage:** Applied Reverse Voltage to assure a nonconductive condition. (See Note.)

V_C **Maximum Clamping Voltage:** The maximum peak voltage appearing across the TransZorb TVS when subjected to the peak pulse current waveform of 8 by 20μs. The peak pulse voltages are the combination of voltage rise due to both the series resistance and thermal rise.

I_{pp} **Peak Pulse Current**

P_p **Peak Pulse Power**

I_D **Reverse Leakage**

NOTE: A TransZorb TVS is normally selected according to the Reverse Stand Off Voltage (V_D) which should be equal to or greater than the dc or continuous peak operating voltage level.

FIGURE 1 -- Peak Pulse Power vs Pulse Time

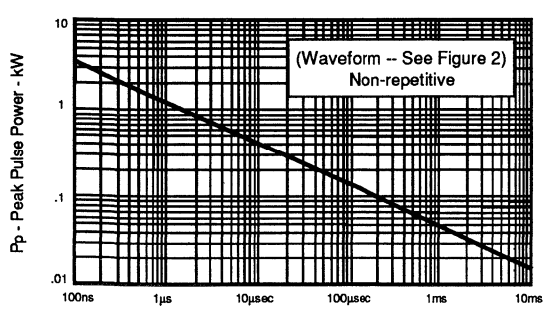
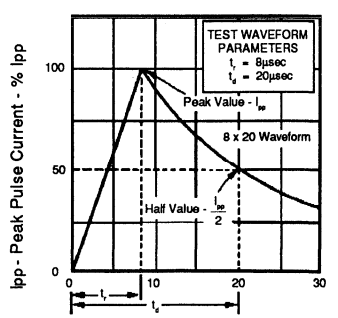


FIGURE 2 -- Pulse Waveform



SURFACE MOUNT DIODE ARRAY TRANSZORB® TVS 8 PIN UNIDIRECTIONAL & BIDIRECTIONAL 5.0 THRU 24 VOLTS

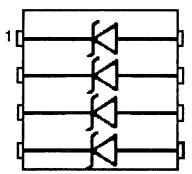
ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER	DEVICE MARKING CODE	REVERSE STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE @ 1mA	MAXIMUM CLAMPING VOLTAGE @ 1A (8/20μs)	MAXIMUM CLAMPING VOLTAGE @ 5A (8/20μs)	LEAKAGE CURRENT @ V_D	CAPACITANCE @ 0V, 1MHz
UNIDIRECTIONAL BIDIRECTIONAL		V_D Volts	$BV_{(min)}$ Volts	V_C Volts	V_C Volts	I_D μA	C pF
SMDA05	SDA	5.0	6.0	9.8	11	100	550
SMDA05C	**SDB**	5.0	6.0	9.8	11	100	400
SMDA12	SDC	12	13.3	19	24	1	185
SMDA12C	**SDD**	12	13.3	19	24	1	150
SMDA15	SDE	15	16.7	24	30	1	140
SMDA15C	**SDF**	15	16.7	24	30	1	100
SMDA24	SDG	24	26.7	43	55	1	88
SMDA24C	**SDH**	24	26.7	43	55	1	63

CIRCUIT DIAGRAM

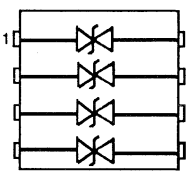
UNIDIRECTIONAL

SMDA05 SMDA12
SMDA15 SMDA24

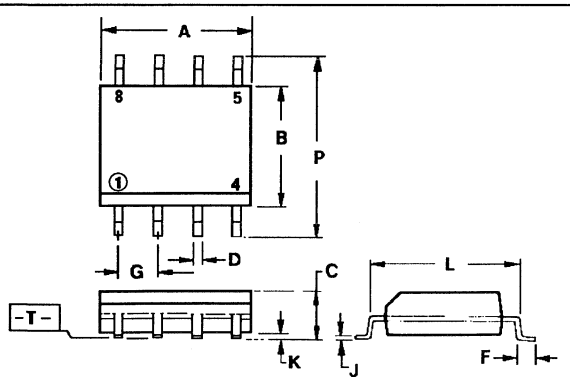


BIDIRECTIONAL

SMDA05C SMDA12C
SMDA15C SMDA24C



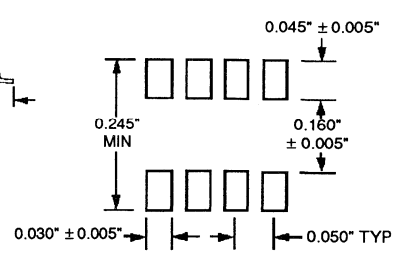
CASE OUTLINE AND SOLDER PAD GEOMETRY



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.206
P	5.79	6.20	0.228	0.244

NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION "A" IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖	0.25 (0.010) Ⓜ	A Ⓢ



General Semiconductor Industries, Inc.

NEW

ZENER DIODES
1.5 WATTS
10V THRU 68V
SURFACE MOUNT
SMZG & SMZJ
Series

FEATURES

- **Zener Voltages 10V - 68V**
- **JEDEC Registered Package Outline for Surface Mounting**
- **Maximum Limits Guaranteed on Four Parameters**

MECHANICAL CHARACTERISTICS

- Molded Surface Mountable Case
- Gull-Wing or Modified J-Bend Leads
- Cathode (Positive end) Marked with Polarity Band
- Body Marked with Type Code

DESCRIPTION

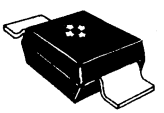
This series of surface mount zener diodes is fully specified for use in power regulator applications. These devices are useful in situations where large surge currents are expected.

MAXIMUM RATINGS

- DC Power Dissipation (P_D): 1.5 watts
- Derated above 75°C: 20 mW / °C
- Junction and Storage Temperature (T_J, T_{stg}): -55°C to +150°C

CASES

Modified J-Bend
Leads (C-Bend)
DO-214AA

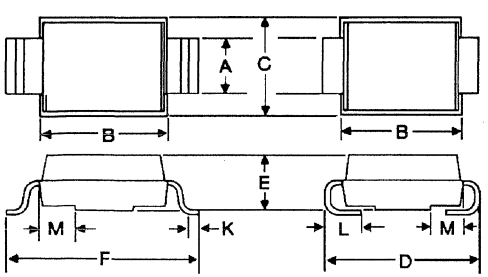


Gull-Wing Leads
DO-215AA

CASE OUTLINE

DO-215AA
"GULL-WING"

DO-214AA
"C" BEND (MODIFIED J-BEND)



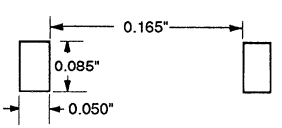
DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.077	.160	.130	.205	.075	.235	.015	.030	.038
MAX	.083	.180	.155	.220	.095	.255	.030	.060	.058
DIMENSIONS IN MILLIMETERS									
MIN	1.96	4.06	3.30	5.21	1.91	5.97	0.38	0.76	0.97
MAX	2.10	4.57	3.81	5.59	2.41	6.48	0.76	1.52	1.47

Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

Components Packaging: Standard 12mm tape.

RECOMMENDED PAD SIZE

GULL-WING
(Pad distances equal layout for SO-8 to 16.)



MODIFIED J-BEND

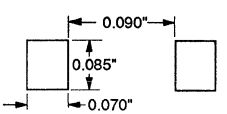
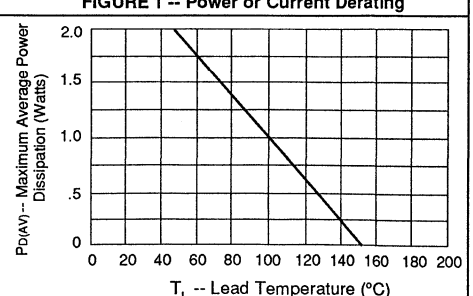


FIGURE 1 -- Power or Current Derating



ELECTRICAL CHARACTERISTICS @ 25°C

GSI PART NUMBER *		DEVICE MARKING CODE	NOMINAL ZENER VOLTAGE	TEST CURRENT	MAX. ZENER IMPEDANCE			MAX. REVERSE LEAKAGE CURRENT		MAX. ZENER CURRENT
GULL-WING	MODIFIED J-BEND		V_Z @ I_{ZT}	I_{ZT}	Z_{ZT} @ I_{ZT}	Z_{ZK} @	I_{ZK}	I_R @	V_R	I_{ZM}
			Volts	mA	Ohms	Ohms	mA	µA	Volts	mA dc
SMZG3789A,B	SMZJ3789A,B	789A,B	10	37.5	5	1000	0.25	50	7.6	125
SMZG3790A,B	SMZJ3790A,B	790A,B	11	34.1	6	650	0.25	10	8.4	115
SMZG3791A,B	SMZJ3791A,B	791A,B	12	31.2	7	550	0.25	5	9.1	105
SMZG3792A,B	SMZJ3792A,B	792A,B	13	28.8	7.5	550	0.25	5	9.9	98
SMZG3793A,B	SMZJ3793A,B	793A,B	15	25.0	9	600	0.25	5	11.4	85
SMZG3794A,B	SMZJ3794A,B	794A,B	16	23.4	10	600	0.25	5	12.2	80
SMZG3795A,B	SMZJ3795A,B	795A,B	18	20.8	12	650	0.25	5	13.7	70
SMZG3796A,B	SMZJ3796A,B	796A,B	20	18.7	14	650	0.25	5	15.2	62
SMZG3797A,B	SMZJ3797A,B	797A,B	22	17.0	17.5	650	0.25	5	16.7	56
SMZG3798A,B	SMZJ3798A,B	798A,B	24	15.6	19	700	0.25	5	18.2	51
SMZG3799A,B	SMZJ3799A,B	799A,B	27	13.9	23	700	0.25	5	20.6	46
SMZG3800A,B	SMZJ3800A,B	800A,B	30	12.5	26	750	0.25	5	22.8	41
SMZG3801A,B	SMZJ3801A,B	801A,B	33	11.4	33	800	0.25	5	25.1	38
SMZG3802A,B	SMZJ3802A,B	802A,B	36	10.4	38	850	0.25	5	27.4	35
SMZG3803A,B	SMZJ3803A,B	803A,B	39	9.6	45	900	0.25	5	29.7	31
SMZG3804A,B	SMZJ3804A,B	804A,B	43	8.7	53	950	0.25	5	32.7	28
SMZG3805A,B	SMZJ3805A,B	805A,B	47	8	67	1000	0.25	5	35.8	26
SMZG3806A,B	SMZJ3806A,B	806A,B	51	7.3	70	1100	0.25	5	38.8	24
SMZG3807A,B	SMZJ3807A,B	807A,B	56	6.7	86	1300	0.25	5	42.6	22
SMZG3808A,B	SMZJ3808A,B	808A,B	62	6	100	1500	0.25	5	47.1	20
SMZG3809A,B	SMZJ3809A,B	809A,B	68	5.5	120	1700	0.25	5	51.7	18

* "A" denotes 10% device tolerance, "B" denotes 5% tolerance.

General Semiconductor Industries, Inc.

NEW

ZENER DIODES 5 WATTS 10V THRU 75V SURFACE MOUNT SMZG & SMZJ Series

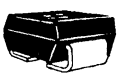
FEATURES

- **Zener Voltages 10V - 75V**
- **JEDEC Registered Package Outline for Surface Mounting**
- **Maximum Limits Guaranteed on Four Parameters**

DESCRIPTION

This series of surface mount zener diodes is fully specified for use in power regulator applications. These devices are useful in situations where large surge currents are expected.

CASES



Modified J-Bend Leads (C-Bend) DO-214AA

Gull-Wing Leads DO-215AA

MAXIMUM RATINGS

- DC Power Dissipation (P_D): 5 watts
- Derated above 75°C: 65 mW / °C
- Junction and Storage Temperature (T_J, T_{stg}): -55°C to +150°C

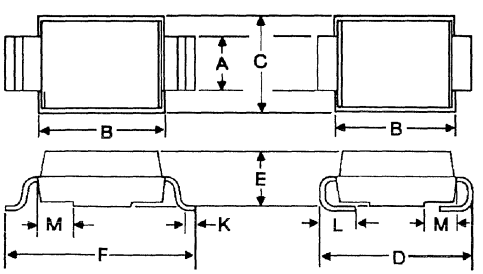
MECHANICAL CHARACTERISTICS

- Molded Surface Mountable Case
- Gull-Wing or Modified J-Bend Leads
- Cathode (Positive end) Marked with Polarity Band
- Body Marked with Type Code

CASE OUTLINE

DO-215AA "GULL-WING"

DO-214AA "C" BEND (MODIFIED J-BEND)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.077	.160	.130	.205	.075	.235	.015	.030	.038
MAX	.083	.180	.155	.220	.095	.255	.030	.060	.058
DIMENSIONS IN MILLIMETERS									
MIN	1.96	4.06	3.30	5.21	1.91	5.97	0.38	0.76	0.97
MAX	2.10	4.57	3.81	5.59	2.41	6.48	0.76	1.52	1.47

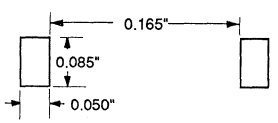
Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

Components Packaging: Standard 12mm tape.

RECOMMENDED PAD SIZE

GULL-WING

(Pad distances equal layout for SO-8 to 16.)



MODIFIED J-BEND

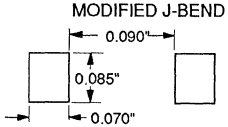
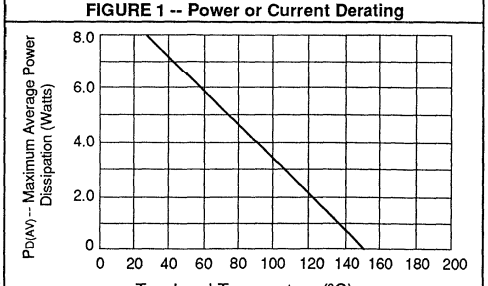


FIGURE 1 -- Power or Current Derating



ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR PART NUMBER *		DEVICE MARKING CODE	NOMINAL ZENER VOLTAGE V_Z @ I_{ZT}	TEST CURRENT I_{ZT}	MAX. ZENER IMPEDANCE		MAX. REVERSE LEAKAGE CURRENT			MAX. ZENER CURRENT I_{ZM}
					Z_{Zt} @ I_{Zt}	Z_{ZK} @ I_{ZK} = 1 mA	I_R µA	@ V_R Volts		
GULL-WING	MODIFIED J-BEND		Volts	mA	Ohms	Ohms		A-Suffix	B-Suffix	mA dc
SMZG5347A,B	SMZJ5347A,B	347A,B	10	125	2.5	600	100	7.2	7.6	475
SMZG5348A,B	SMZJ5348A,B	348A,B	11	125	3	400	10	8.0	8.4	430
SMZG5349A,B	SMZJ5349A,B	349A,B	12	100	3	300	5	8.6	9.1	395
SMZG5350A,B	SMZJ5350A,B	350A,B	13	100	3	200	5	9.4	9.9	365
SMZG5351A,B	SMZJ5351A,B	351A,B	14	100	3	100	5	10.1	10.6	340
SMZG5352A,B	SMZJ5352A,B	352A,B	15	75	3	100	5	10.8	11.5	315
SMZG5353A,B	SMZJ5353A,B	353A,B	16	75	3	100	5	11.5	12.2	295
SMZG5354A,B	SMZJ5354A,B	354A,B	17	70	3	100	5	12.2	12.9	280
SMZG5355A,B	SMZJ5355A,B	355A,B	18	65	3	100	5	13.0	13.7	265
SMZG5356A,B	SMZJ5356A,B	356A,B	19	65	3	100	5	13.7	14.4	250
SMZG5357A,B	SMZJ5357A,B	357A,B	20	65	3	100	5	14.4	15.2	237
SMZG5358A,B	SMZJ5358A,B	358A,B	22	50	3.5	100	5	15.8	16.7	216
SMZG5359A,B	SMZJ5359A,B	359A,B	24	50	3.5	100	5	17.3	18.2	198
SMZG5360A,B	SMZJ5360A,B	360A,B	25	50	4	110	5	18.0	19.0	190
SMZG5361A,B	SMZJ5361A,B	361A,B	27	50	5	120	5	19.4	20.6	176
SMZG5362A,B	SMZJ5362A,B	362A,B	28	50	6	130	5	20.1	21.2	170
SMZG5363A,B	SMZJ5363A,B	363A,B	30	40	8	140	5	21.6	22.8	158
SMZG5364A,B	SMZJ5364A,B	364A,B	33	40	10	150	5	23.8	25.1	144
SMZG5365A,B	SMZJ5365A,B	365A,B	36	30	11	160	5	25.9	27.4	132
SMZG5366A,B	SMZJ5366A,B	366A,B	39	30	14	170	5	28.1	29.7	122
SMZG5367A,B	SMZJ5367A,B	367A,B	43	30	20	190	5	31.0	32.7	110
SMZG5368A,B	SMZJ5368A,B	368A,B	47	25	25	210	5	33.8	35.8	100
SMZG5369A,B	SMZJ5369A,B	369A,B	51	25	27	230	5	36.7	38.8	93
SMZG5370A,B	SMZJ5370A,B	370A,B	56	20	35	280	5	40.3	42.6	86
SMZG5371A,B	SMZJ5371A,B	371A,B	60	20	40	350	5	43.0	45.5	79
SMZG5372A,B	SMZJ5372A,B	372A,B	62	20	42	400	5	44.6	47.1	76
SMZG5373A,B	SMZJ5373A,B	373A,B	68	20	44	500	5	49.0	51.7	70
SMZG5374A,B	SMZJ5374A,B	374A,B	75	20	45	620	5	54.0	56.0	63

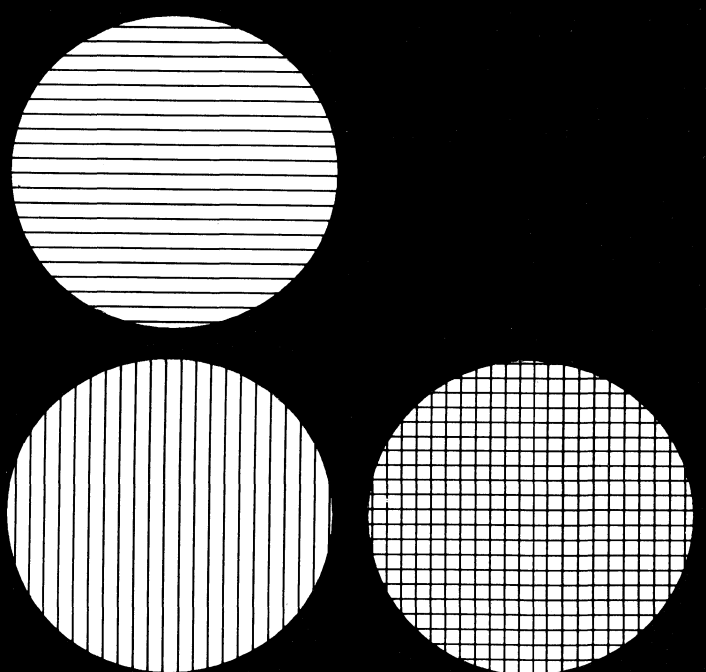
*"A" denotes 10% device tolerance, "B" denotes 5% tolerance.

General Semiconductor Industries, Inc.

SECTION 2

DISCRETE SEMICONDUCTOR CHIPS

- TransZorb® TVS Diode Chips
- NPN Silicon Transistor Chips



Dear Customer:

General Semiconductor Industries, Inc. (GSI) is pleased to introduce a standard product line offering of discrete semiconductor chips. GSI chips originate from our TransZorb® TVS diode and NPN silicon transistor product lines, and are manufactured at our world class wafer fabs in Tempe, Arizona, and Macroom, County Cork, Ireland.

This catalog has been developed to assist in the selection of chips for your hybrid, smart card, and connector designs. A broad selection will assure that the precise voltage and power rating for your application may be readily identified. Applications and/or sales assistance is available by contacting your local GSI sales representative office.

General Semiconductor Industries, Inc.
2001 West Tenth Place
Tempe, AZ 85281

General Semiconductor Ireland Ltd.
Macroom
County Cork
IRELAND

Part I

TRANSZORB®

TRANSIENT VOLTAGE SUPPRESSION

DIODE CHIPS

Introduction

General Semiconductor Industries, Inc. offers a complete line of TransZorb®* transient voltage suppressor semiconductor chips in die and cell construction, utilizing mesa and planar processing. Chips are available in unidirectional and bidirectional polarity, voltages ranging from 5V through 100V, and varying peak pulse power handling capabilities. Chips are tested to a specified and guaranteed set of parameters and subjected to the same rigid in-process controls as packaged devices.

Testing and Inspection

The breakdown voltage (B_V) and leakage current (I_R) of GSI's TVS chips are 100% tested. Visual inspection, to the criteria of MIL-STD-750, Method 2073, and surge testing are available at a nominal cost. Surge testing would be performed on a sample lot basis. The surge specification as noted per device series is the capability of the chip.

Metallized Surfaces

Mesa die is offered with top and backside metallization of nickel-nickel-gold. Planar die is offered with aluminum topside and chrome-silver-gold backside metallization or top and backside metallization of chrome-silver-gold. Mesa cell is a mesa die soldered between two silver clad aluminum disks.

Chip Bonding

GSI's TVS chips are compatible with solder bonding techniques. Connections to the device can be made by conventional wiring bonding, ribbon lead bonding, or solder bonding techniques.

Polarity Orientation

Mesa die is cathode up for all voltages offered. Planar die is offered with cathode (window up) for 5V and anode up for all other voltages.

Packaging

GSI supplies all semiconductor die in either industry multi-pak or glass vials. The number of die per multi-pak will be dependent upon the die size.

Each container will be packaged in an anti-static bag and labeled with the following information:

* GSI's device part number
* Wafer lot number
* Date code (testing date)
* Quantity
* Logo

Chip Size

According to power rating capabilities, die and cell size will be per the following matrix. All dimensions are in inches.

Power	Pulse Waveform	Mesa Die	Mesa Cell	Planar Die
300W	8/20μs	----	----	.025 sq.
500W	8/20μs	----	----	.037 sq.
500W	10/1000μs	.070 sq.	.100 dia.	----
600W	10/1000μs	.080 sq.	.113 dia.	----
1.5kW	10/1000μs	.114 sq.	.160 dia.	----

Chip Identification

The listed part numbers and applicable product notes designate GSI's standard product offering. All Mesa processed chips will carry the part number of a GSI encapsulated (packaged) counterpart.

Example:

MD	SA	15
Mesa Die	Packaged Device Series	15V V_R

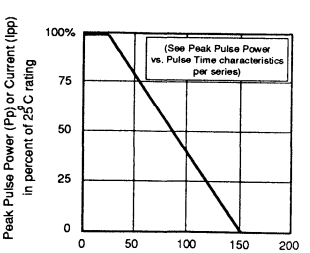
Planar die series carries the chip size.

Example:

PD	37S	05
Planar Die	.037" Die Size	5V V_R

Temperature Derating

Typical power derating curve for TVS chips above 25°C:



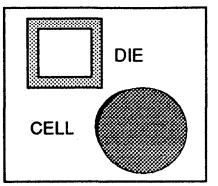
* TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

General Semiconductor Industries, Inc.

TRANSZORB® TVS CHIPS
MDSA & MCSA Series

DESCRIPTION

This TransZorb® TVS chip series is designed for hybrid, smart card and connector applications. High current handling capabilities and fast response time makes these TVS chips excellent for protection against damaging transient voltages caused by lightning, load switching, and electrostatic discharge. This series of silicon transient suppressor chips has a peak pulse rating of 500 watts for one millisecond.



FEATURES

- **Voltage Range: 5V - 100V**
- **500 watts Peak Pulse Power**
- **Mesa Construction Glass-Passivated**
- **Lot Traceability**

MAXIMUM RATINGS

• Power Dissipation @ T_A = 25°C (10/1000µs):	500 watts
• Forward Surge Rating @ 25°C Unidirectional only:	70 amps (1/20 sec half cycle)
• Operating and Storage Temperature:	-55°C to +150°C

PHYSICAL CHARACTERISTICS

	DIE	CELL
Size:	.070 inches sq.	.100 inches dia.
Thickness - Unidirectional:	.014 inches max.	---
Bidirectional:	.0155 inches max.	.045 inches max.
Bond Area:	.055 inches sq. max.	.100 inches
Metallized Surface:	Ni-Ni-Au	Silver Clad Alum. Disks
Polarity:	Unidirectional & Bidirectional	Bidirectional

NOTES

1. Unidirectional die are cathode topside orientation. To specify bidirectional die, add a "C" suffix. MDSA5.0 and MDSA6.0 are available in unidirectional only.

2. A TransZorb® TVS is normally selected according to the "Reverse Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or the Continuous Peak Operating Voltage.

3. The I_R limit is doubled for bidirectional devices with V_R equal to or less than 10V.

ABBREVIATIONS

V_R The Stand-Off Voltage: the applied reverse voltage to assure a nonconductive condition.

$B_{V(min)}$ The minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C The maximum peak voltage appearing across the device when subjected to the peak pulse current.

Ipp Peak Pulse Current - (see Fig 2).

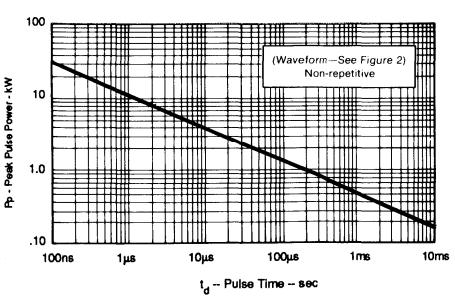


Figure 1 – Peak Pulse Power vs. Pulse Time

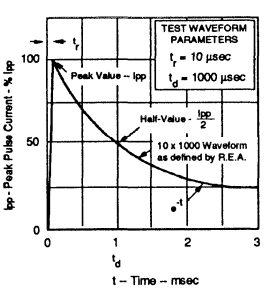


Figure 2 – Pulse Waveform

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR INDUSTRIES' DEVICE NUMBER		REVERSE STAND-OFF VOLTAGE (NOTE 2)	BREAKDOWN VOLTAGE V_{BR} VOLTS		MAXIMUM CLAMPING VOLTAGE @ Ipp (FIG 2)	MAXIMUM PEAK PULSE CURRENT (FIG 2)	MAXIMUM REVERSE LEAKAGE @V_R (NOTE 3)
DIE	CELL	V_R VOLTS	MIN	@ I_T mA	V_C VOLTS	Ipp A	I_R µA
MDSA5.0	---	5.0	6.40	10	9.2	54.0	600
MDSA6.0	---	6.0	6.67	10	10.3	48.5	600
MDSA6.5	MCSA6.5C	6.5	7.22	10	11.2	44.7	400
MDSA7.0	MCSA7.0C	7.0	7.78	10	12.0	41.7	150
MDSA7.5	MCSA7.5C	7.5	8.33	1	12.9	38.8	50
MDSA8.0	MCSA8.0C	8.0	8.89	1	13.6	36.7	25
MDSA8.5	MCSA8.5C	8.5	9.44	1	14.4	34.7	10
MDSA9.0	MCSA9.0C	9.0	10.0	1	15.4	32.5	5
MDSA10	MCSA10C	10	11.1	1	17.0	29.4	3
MDSA11	MCSA11C	11	12.2	1	18.2	27.4	3
MDSA12	MCSA12C	12	13.3	1	19.9	25.1	3
MDSA13	MCSA13C	13	14.4	1	21.5	23.2	3
MDSA14	MCSA14C	14	15.6	1	25.8	21.5	3
MDSA15	MCSA15C	15	16.7	1	24.4	20.6	3
MDSA16	MCSA16C	16	17.8	1	26.0	19.2	3
MDSA17	MCSA17C	17	18.9	1	27.6	18.1	3
MDSA18	MCSA18C	18	20.0	1	29.2	17.2	3
MDSA20	MCSA20C	20	22.2	1	32.4	15.4	3
MDSA22	MCSA22C	22	24.4	1	35.5	14.1	3
MDSA24	MCSA24C	24	26.7	1	38.9	12.8	3
MDSA26	MCSA26C	26	28.9	1	42.1	11.9	3
MDSA28	MCSA28C	28	31.1	1	45.4	11.0	3
MDSA30	MCSA30C	30	33.3	1	48.4	10.3	3
MDSA33	MCSA33C	33	36.7	1	53.3	9.4	3
MDSA36	MCSA36C	36	40.0	1	58.1	8.6	3
MDSA40	MCSA40C	40	44.4	1	64.5	7.8	3
MDSA43	MCSA43C	43	47.8	1	69.4	7.2	3
MDSA45	MCSA45C	45	50.0	1	72.7	6.9	3
MDSA48	MCSA48C	48	53.3	1	77.4	6.5	3
MDSA51	MCSA51C	51	56.7	1	82.4	6.1	3
MDSA54	MCSA54C	54	60.0	1	87.1	5.7	3
MDSA58	MCSA58C	58	64.4	1	93.6	5.3	3
MDSA60	MCSA60C	60	66.7	1	96.8	5.2	3
MDSA64	MCSA64C	64	71.1	1	103.0	4.9	3
MDSA70	MCSA70C	70	77.8	1	113.0	4.4	3
MDSA75	MCSA75C	75	83.3	1	121.0	4.1	3
MDSA78	MCSA78C	78	86.7	1	126.0	4.0	3
MDSA85	MCSA85C	85	94.4	1	137.0	3.6	3
MDSA90	MCSA90C	90	100.0	1	146.0	3.4	3

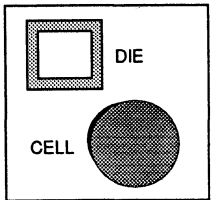
General Semiconductor Industries, Inc.

TRANSZORB® TVS CHIPS

MDP6K & MCP6K Series

DESCRIPTION

This TransZorb® TVS series is designed for hybrid, smart card and connector applications. High current handling capabilities and fast response time makes these TVS chip excellent for protection against damaging transient voltages caused by lightning, load switching and electrostatic discharge. This series of silicon transient suppressor chips has a peak pulse rating of 600 watts for one millisecond.



FEATURES

- **Voltage Range: 6.8V - 100V**
- **600 watts Peak Pulse Power**
- **Mesa Construction Glass-Passivated**
- **Lot Traceability**

MAXIMUM RATINGS

- Power Dissipation @ T_A = 25°C (10/1000µs): 600 watts
- Forward Surge Rating @ 25°C Unidirectional only: 100 amps (1/20 sec half cycle)
- Operating and Storage Temperature: -55°C to +150°C

PHYSICAL CHARACTERISTICS

	DIE	CELL
Size:	.080 inches sq.	.113 inches sq. dia.
Thickness - Unidirectional:	.014 inches max.	---
Bidirectional:	.0155 inches max.	.045 inches max.
Bond Area:	.065 inches sq. max.	.113 inches
Metallized Surface:	Ni-Ni-Au	Silver Clad Alum. Disks
Polarity:	Unidirectional & Bidirectional	Bidirectional

NOTES

1. Unidirectional die are cathode topside orientation. To specify bidirectional die, add a "C" suffix. MDP6K6.8 is available in unidirectional only.

2. A TransZorb® TVS is normally selected according to the "Reverse Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or the Continuous Peak Operating Voltage.

3. The I_R limit is doubled for bidirectional devices with V_R equal to or less than 10V.

ABBREVIATIONS

V_R The Stand-Off Voltage: the applied reverse voltage to assure a nonconductive condition.

$B_{V(min)}$ The minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C The maximum peak voltage appearing across the device when subjected to the peak pulse current.

Ipp Peak Pulse Current - (see Fig 2).

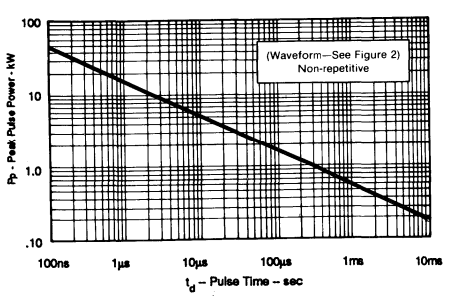


Figure 1 – Peak Pulse Power vs. Pulse Time

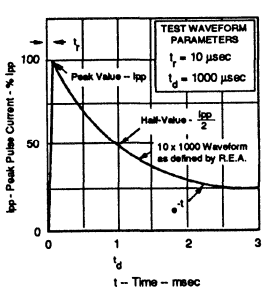


Figure 2 – Pulse Waveform

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR INDUSTRIES' DEVICE NUMBER		REVERSE STAND-OFF VOLTAGE (NOTE 2)	BREAKDOWN VOLTAGE V_{BR} VOLTS		MAXIMUM CLAMPING VOLTAGE @ Ipp (FIG 2)	MAXIMUM PEAK PULSE CURRENT (FIG 2)	MAXIMUM REVERSE LEAKAGE @V_R (NOTE 3)
DIE	CELL	V_R VOLTS	MIN	@ I_T mA	V_C VOLTS	Ipp A	I_R µA
MDP6K6.8	---	5.80	6.45	10	10.5	57	1000
MDP6K7.5	---	6.40	7.13	10	11.3	53	500
MDP6K8.2	MCP6K8.2C	7.02	7.79	10	12.1	50	200
MDP6K9.1	MCP6K9.1C	7.78	8.65	1	13.4	45	50
MDP6K10	MCP6K10C	8.55	9.50	1	14.5	41	10
MDP6K11	MCP6K11C	9.40	10.5	1	15.6	38	5
MDP6K12	MCP6K12C	10.2	11.4	1	16.7	36	5
MDP6K13	MCP6K13C	11.1	12.4	1	18.2	33	5
MDP6K15	MCP6K15C	12.8	14.3	1	21.2	28	5
MDP6K16	MCP6K16C	13.6	15.2	1	22.5	27	5
MDP6K18	MCP6K18C	15.3	17.1	1	25.2	24	5
MDP6K20	MCP6K20C	17.1	19.0	1	27.7	22	5
MDP6K22	MCP6K22C	18.8	20.9	1	30.6	20	5
MDP6K24	MCP6K24C	20.5	22.8	1	33.2	18	5
MDP6K27	MCP6K27C	23.1	25.7	1	37.5	16	5
MDP6K30	MCP6K30C	25.6	28.5	1	41.4	14.4	5
MDP6K33	MCP6K33C	28.2	31.4	1	45.7	13.2	5
MDP6K36	MCP6K36C	30.8	34.2	1	49.9	12.0	5
MDP6K39	MCP6K39C	33.3	37.1	1	53.9	11.2	5
MDP6K43	MCP6K43C	36.8	40.9	1	59.3	10.1	5
MDP6K47	MCP6K47C	40.2	44.7	1	64.8	9.3	5
MDP6K51	MCP6K51C	43.6	48.5	1	70.1	8.6	5
MDP6K56	MCP6K56C	47.8	53.2	1	77.0	7.8	5
MDP6K62	MCP6K62C	53.0	58.9	1	85.0	7.1	5
MDP6K68	MCP6K68C	58.1	64.6	1	92.0	6.5	5
MDP6K75	MCP6K75C	64.1	71.3	1	103.0	5.8	5
MDP6K82	MCP6K82C	70.1	77.9	1	113.0	5.3	5
MDP6K91	MCP6K91C	77.8	86.5	1	125.0	4.8	5
MDP6K100	MCP6K100C	85.5	95.0	1	137.0	4.4	5

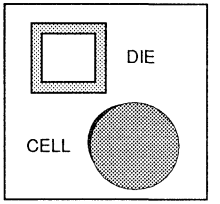
General Semiconductor Industries, Inc.

TRANSZORB® TVS CHIPS

MD1.5K & MC1.5K Series

DESCRIPTION

This TransZorb® TVS chip series is designed for hybrid, smart card and connector applications. High current handling capabilities and fast response time makes these TVS chips excellent for protection against damaging transient voltages caused by lightning, load switching and electrostatic discharge. This series of silicon transient suppressor chips has a peak pulse rating of 1500 watts for one millisecond.



FEATURES

- **Voltage Range: 6.8V - 100V**
- **1.5kW Peak Pulse Power**
- **Mesa Construction Glass-Passivated**
- **Lot Traceability**

MAXIMUM RATINGS

- Power Dissipation @ T_A = 25°C (10/1000µs): 1500 watts
- Forward Surge Rating @ 25°C Unidirectional only: 200 amps (1/20 sec half cycle)
- Operating and Storage Temperature: -55°C to +150°C

PHYSICAL CHARACTERISTICS

	DIE	CELL
Size:	.114 inches sq.	.160 inches dia.
Thickness - Unidirectional:	.014 inches max.	---
Bidirectional:	.0155 inches max.	.045 inches max.
Bond Area:	.099 inches sq. max.	.160 inches
Metallized Surface:	Ni-Ni-Au	Silver Clad Alum. Disks
Polarity:	Unidirectional & Bidirectional	Bidirectional

NOTES

1. Unidirectional die are cathode topside orientation. To specify bidirectional die, add a "C" suffix. MD1.5K6.8 is available in unidirectional only.

2. A TransZorb® TVS is normally selected according to the "Reverse Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or the Continuous Peak Operating Voltage.

3. The I_R limit is doubled for bidirectional devices with V_R equal to or less than 10V.

ABBREVIATIONS

V_R The Stand-Off Voltage: the applied reverse voltage to assure a nonconductive condition.

$B_{V(min)}$ The minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C The maximum peak voltage appearing across the device when subjected to the peak pulse current.

Ipp Peak Pulse Current - (see Fig 2).

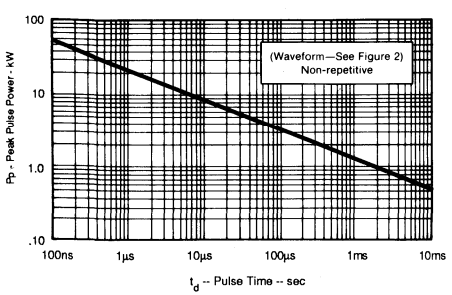


Figure 1 – Peak Pulse Power vs. Pulse Time

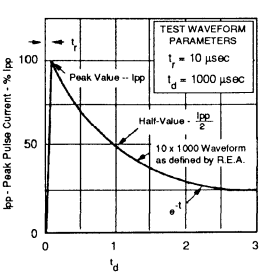


Figure 2 – Pulse Waveform

ELECTRICAL CHARACTERISTICS @ 25°C

GENERAL SEMICONDUCTOR INDUSTRIES' DEVICE NUMBER		REVERSE STAND-OFF VOLTAGE (NOTE 2)	BREAKDOWN VOLTAGE V_{BR} VOLTS		MAXIMUM CLAMPING VOLTAGE @ I_{PP} (FIG 2)	MAXIMUM PEAK PULSE CURRENT (FIG 2)	MAXIMUM REVERSE LEAKAGE @V_R (NOTE 3)
DIE	CELL	V_R VOLTS	MIN	@ IT mA	V_C VOLTS	I_{PP} A	I_R µA
MD1.5K6.8	---	5.80	6.45	10	10.5	143.0	1000
MD1.5K7.5	MC1.5K7.5C	6.40	7.13	10	11.3	132.0	500
MD1.5K8.2	MC1.5K8.2C	7.02	7.79	10	12.1	124.0	200
MD1.5K9.1	MC1.5K9.1C	7.78	8.65	1	13.4	112.0	50
MD1.5K10	MC1.5K10C	8.55	9.50	1	14.5	103.0	10
MD1.5K11	MC1.5K11C	9.40	10.5	1	15.6	96.0	5
MD1.5K12	MC1.5K12C	10.2	11.4	1	16.7	90.0	5
MD1.5K13	MC1.5K13C	11.1	12.4	1	18.2	82.0	5
MD1.5K15	MC1.5K15C	12.8	14.3	1	21.2	71.0	5
MD1.5K16	MC1.5K16C	13.6	15.2	1	22.5	67.0	5
MD1.5K18	MC1.5K18C	15.3	17.1	1	25.2	59.5	5
MD1.5K20	MC1.5K20C	17.1	19.0	1	27.7	54.0	5
MD1.5K22	MC1.5K22C	18.8	20.9	1	30.6	49.0	5
MD1.5K24	MC1.5K24C	20.5	22.8	1	33.2	45.0	5
MD1.5K27	MC1.5K27C	23.1	25.7	1	37.5	40.0	5
MD1.5K30	MC1.5K30C	25.6	28.5	1	41.4	36.0	5
MD1.5K33	MC1.5K33C	28.2	31.4	1	45.7	33.0	5
MD1.5K36	MC1.5K36C	30.8	34.2	1	49.9	30.0	5
MD1.5K39	MC1.5K39C	33.3	37.1	1	53.9	28.0	5
MD1.5K43	MC1.5K43C	36.8	40.9	1	59.3	25.3	5
MD1.5K47	MC1.5K47C	40.2	44.7	1	64.8	23.2	5
MD1.5K51	MC1.5K51C	43.6	48.5	1	70.1	21.4	5
MD1.5K56	MC1.5K56C	47.8	53.2	1	77.0	19.5	5
MD1.5K62	MC1.5K62C	53.0	58.9	1	85.0	17.7	5
MD1.5K68	MC1.5K68C	58.1	64.6	1	92.0	16.3	5
MD1.5K75	MC1.5K75C	64.1	71.3	1	103.0	14.6	5
MD1.5K82	MC1.5K82C	70.1	77.9	1	113.0	13.3	5
MD1.5K91	MC1.5K91C	77.8	86.5	1	125.0	12.0	5
MD1.5K100	MC1.5K100C	85.5	95.0	1	137.0	11.0	5

General Semiconductor Industries, Inc.

TRANSZORB® TVS CHIPS

PD25S Series

DESCRIPTION

This TransZorb® TVS chip series is designed for hybrid, smart card and connector applications. High current handling capabilities and fast response time makes these TVS chips excellent for protection against damaging transient voltages caused by electrostatic discharge. This series of silicon transient suppressor chips is designed for extremely low clamping voltage requirements and has a peak pulse rating of 300 watts for twenty microseconds.

FEATURES

- **Voltage Range: 5V, 12V, 15V and 24V**
- **300 watts Peak Pulse Power**
- **Planar Construction**
- **Lot Traceability**

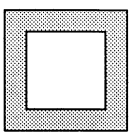
MAXIMUM RATINGS

• Power Dissipation @ T_A = 25°C (8/20µs):	300 watts
• Forward Surge Rating @ 25°C:	5 amps (1/20 sec half cycle)
• Operating and Storage Temperature:	-55°C to +150°C

PHYSICAL CHARACTERISTICS

Size:	.025 inches sq.
Thickness:	.010 inches max.
Bond Area:	.019 inches max.
Metallized Surface - Standard:	Al (top); Cr-Ag-Au (back)
Option (see Note 2):	Cr-Ag-Au (top & backside)
Polarity:	Unidirectional

DIE



NOTES

1. Part numbers shown are cathode topside for 5V product and anode topside for all other voltages.

2. Part numbers shown have aluminum topside and chrome/silver/goldbackside metallization. For chrome/silver/gold top and backside metallization, add a "B" suffix.

3. TransZorb® TVSs are normally selected according to the "Reverse Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or Continuous Peak Operating Voltage.

ABBREVIATIONS

V_R The Stand-Off Voltage: the applied reverse voltage to assure a nonconductive condition.

$B_{V(min)}$ The minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C The maximum peak voltage appearing across the device when subjected to the peak pulse current.

Ipp Peak Pulse Current - (see Fig 2).

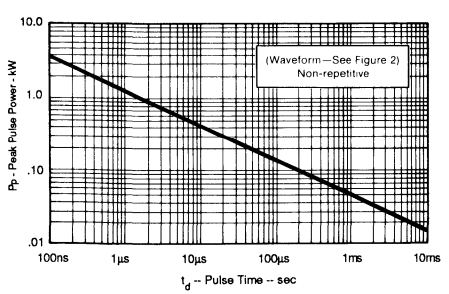


Figure 1 – Peak Pulse Power vs. Pulse Time

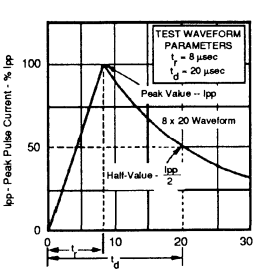


Figure 2 – Pulse Waveform

ELECTRICAL CHARACTERISTICS @ 25°C						
GENERAL SEMICONDUCTOR INDUSTRIES' DEVICE NUMBER SINGLE DIE	REVERSE STAND-OFF VOLTAGE (NOTE 3) V_R VOLTS	BREAKDOWN VOLTAGE V_{BR} VOLTS MIN	@ I_T mA	MAXIMUM CLAMPING VOLTAGE @ 1A V_{C1} VOLTS	MAXIMUM CLAMPING VOLTAGE @ 5A V_{C2} VOLTS	MAXIMUM LEAKAGE CURRENT @ V_R I_R µA
PD25S5.0	5.0	6.0	1	9.8	11.0	100
PD25S12	12.0	13.3	1	18.0	22.0	1
PD25S15	15.0	16.7	1	23.0	28.0	1
PD25S24	24.0	26.7	1	40.0	50.0	1

General Semiconductor Industries, Inc.

TRANSZORB® TVS CHIPS

PD37S Series

DESCRIPTION

The TransZorb® TVS chip series is designed for hybrid, smart card and connector applications. High current handling capabilities and fast response time makes these TVS chips excellent for protection against damaging transient voltages caused by electrostatic discharge. This series of silicon transient suppressor chips is designed for extremely low clamping voltage requirements and has a peak pulse rating of 500 watts for twenty microseconds.

FEATURES

- **Voltage Range: 5V, 12V, 15V, 24V and 30V**
- **500 watts Peak Pulse Power**
- **Planar Construction**
- **Lot Traceability**

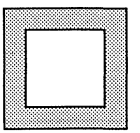
MAXIMUM RATINGS

• Power Dissipation @ T_A = 25°C (8/20µs):	500 watts
• Forward Surge Rating @ 25°C:	10 amps (1/20 sec half cycle)
• Operating and Storage Temperature:	-55°C to +150°C

PHYSICAL CHARACTERISTICS

Size:	.037 inches sq.
Thickness:	.010 inches max.
Bond Area:	.029 inches sq.
Metallized Surface - Standard:	Al (top); Cr-Ag-Au (back)
Option (see Note 2):	Cr-Ag-Au; (top & backside)
Polarity:	Unidirectional

DIE



NOTES

1. Part numbers shown are cathode topside for 5V product and anode topside for all other voltages.

2. Part numbers shown have aluminum topside and chrome/silver/goldbackside metallization. For chrome/silver/gold top and backside metalization, add a "B" suffix.

3. TransZorb® TVSs are normally selected according to the "Reverse Stand-Off Voltage" (V_R) which should be equal to or greater than the DC or Continuous Peak Operating Voltage.

ABBREVIATIONS

V_R The Stand-Off Voltage: the applied reverse voltage to assure a nonconductive condition.

$B_{V(min)}$ The minimum Breakdown Voltage the device will exhibit and is used to assure that conduction does not occur prior to this voltage level at 25°C.

V_C The maximum peak voltage appearing across the device when subjected to the peak pulse current.

Ipp Peak Pulse Current - (see Fig 2).

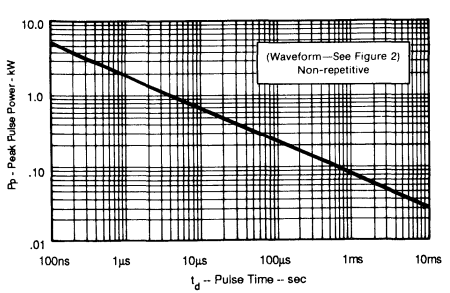


Figure 1 – Peak Pulse Power vs. Pulse Time

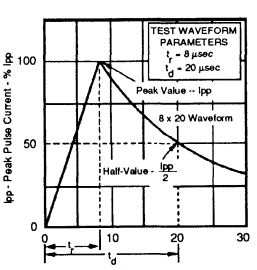


Figure 2 – Pulse Waveform

ELECTRICAL CHARACTERISTICS @ 25°C						
GENERAL SEMICONDUCTOR INDUSTRIES' DEVICE NUMBER SINGLE DIE	REVERSE STAND-OFF VOLTAGE (NOTE 3) V_R VOLTS	BREAKDOWN VOLTAGE V_{BR} VOLTS MIN	@ I_T mA	MAXIMUM CLAMPING VOLTAGE @ 1A V_{C1} VOLTS	MAXIMUM CLAMPING VOLTAGE @ 10A V_{C2} VOLTS	MAXIMUM LEAKAGE CURRENT @ V_R I_R µA
PD37S5.0	5.0	6.0	1	10.2	12.5	200
PD37S12	12.0	13.3	1	21.1	26.0	2
PD37S15	15.0	16.7	1	26.7	33.0	2
PD37S24	24.0	26.7	1	42.3	52.1	2
PD37S30	30.0	33.3	1	52.8	65.0	2

Part II

NPN SILICON

TRANSISTOR CHIPS

Basic Characteristics

All NPN silicon bipolar power switching transistors manufactured by General Semiconductor Industries, Inc. are available in die or wafer form.

General Semiconductor provides as a minimum for every chip order:

A. 100% electrical probe test to low current parameters (15A max.).

B. 100% visual inspection per MIL-STD-750, Method 2072.

C. Element evaluation of mounted samples per MIL-STD-883C, Method 5008, Class B (See Appendix A). Recorded data and element evaluation samples are shipped to the customer with the chip order. Original data is also kept on file at GSI.

D. Chips packaged in industry standard anti-static "waffle pack" chip carriers. Each carrier is labeled with:

- GSI part number
- Customer part number
- Lot acceptance date code
- Wafer lot number
- Purchase order number
- GSI order acknowledgement number
- Quantity

E. Certificate of conformance to all electrical and mechanical specifications.

Die back metallization options include alloyed gold for Au/Si eutectic die attach, or chrome-silver-gold for soft solder die attach. Chips can also be supplied premounted on BeO or Molybdenum substrate. Top metallization is aluminum for ultrasonic aluminum wire bonding.

Technical assistance is available from the factory for achieving optimum results in die attachment, wire bonding, and the like, as well as assistance in selecting the appropriate chip for your application.

Chip Selection

Chip numbers shown in Table I reference JEDEC standard packaged transistor part numbers and GSI in-house standard part numbers which are typically assembled from that chip. A proprietary part number will be assigned to your selected chip by GSI. Please contact your GSI Sales Representative for information and assistance.

TABLE I

Chip Number	I_c max	Typical Device Types
01	3A	2N3506, 2N3507
05	5A	2N2891
11	10A	2N3418 - 2N3421, 2N4150
21	20-50A	2N6653 - 2N6655, GSDS50020
25	10-20A	GSTU6040, GSTU15020
31	20A	2N6922 - 2N6923, GSRU15040- GSRU20040
35	15A	2N6920 - 2N6921
37	35A	2N6924 - 2N6925
39	15-50A	2N6274 - 2N6277, 2N6678
41	10-25-30A	2N6338 - 2N6341 2N6584, GSTU30020

Mechanical Characteristics

Transistor chips are supplied with length and width dimensions as shown on the individual data sheets. The standard die thickness is .011 inches plus or minus .001 inches.

Two backside metallization systems are available. Our Cr-Ag-Au system is suitable for Au-Sn eutectic (80/20) mount or Pb-Sn-Ag soft solder mount. The thickness of the Cr-Ag-Au metallization is approximately 10,000 Angstroms. Chips are also available with alloyed Au back metallization (2,000 Angstroms deposited Au, then alloyed) for Au-Si eutectic die mount. A preform (Au/Si, 98/2) may be required for adequate flow to some substrates.

GSI can supply transistor chips premounted on substrates of beryllium oxide or molybdenum. Contact your GSI Sales Representative for information regarding standard sizes and availability.

Front-side aluminum thickness is 50,000 Angstroms minimum to accomodate ultrasonic aluminum bonding of lead wires. All chips are processed with a thermally-grown oxide over all exposed junctions to assure low leakage currents. As added protection for the junction and front aluminum, many devices are available with a glassivation coating. The glassivation completely covers the die front except at the wire bond pad areas. Glassivation thickness is 6,000 Angstroms minimum.

Electrical Test

All wafers are 100% probe tested to low current parameters: I_C to 15 amps, BV_{CBO} to 600 volts. Electrical testing of packaged element evaluation samples is performed to the requirements of MIL-STD-883C, Method 5008, para. 3.2.2, Class B (see Appendix A).

Product Assembly

A. Chrome-silver-gold backed chips:

The recommended soft solder preform for mounting of Cr-Ag-Au backed chips is lead/tin/silver (95/2.5/2.5). Die bonding in either a belt furnace or temperature-controlled mounting station should be performed in a forming gas atmosphere (Nitrogen/Hydrogen, 95/5) at a maximum temperature of 350°C. If a belt furnace is used, individual die should be weighted to assure adequate pressure to create a good mechanical bond. Mechanical scrubbing may be used with die mounting stations. Au-Sn (80/20) eutectic bonding may also be used with Cr-Ag-Au backed chips. Belt furnace reflow at 310°C in forming gas is recommended.

B. Gold backed chips:

Eutectic bonding is generally performed in a forming gas atmosphere (Nitrogen/Hydrogen 95/5) to prevent oxidation. The recommended temperature is 425°C; maximum recommended temperature is 450°C. Mechanical scrubbing is required. A gold/silicon preform (98/2) may be used to facilitate void-free bonding.

Wire Bonding

Ultrasonic aluminum wire bonding is recommended. Clamping of the die assembly is necessary for high quality ultrasonic bonds. Gold ball bonding is not recommended on power devices.

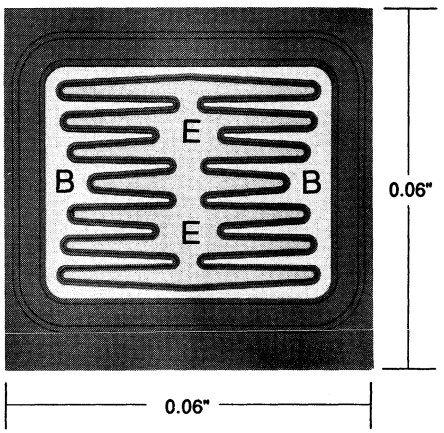
Technical Assistance

GSI manufacturing and engineering personnel possess many years of experience in the processing, mounting, wire bonding, and testing of transistor chips. Answers to your questions are only a phone call away!

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "01"

Typical Device Types: 2N3506, 2N3507



Bonding Pad Areas

Base
(2) 5 x 4 mils

Emitter
(2) 6.5 x 4.5 mils

Front Metallization:

Aluminum

Back Metallization:

Gold

3 AMP
Fast Switching

Typical Switching
(TO-5 Package)

- t_d = 15nsec
- t_r = 25nsec
- t_s = 45nsec
- t_f = 25nsec

Conditions:
V_{CC} = 30V, I_C = 1.5A,
$I_{B1} = I_{B2}$ = 150mA

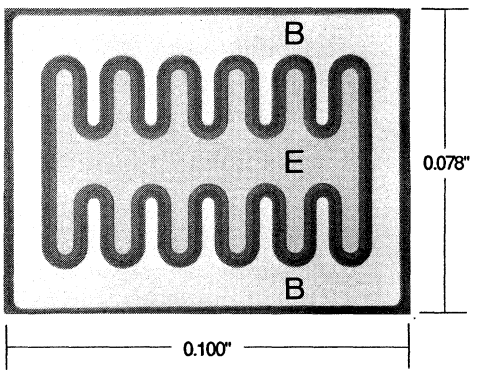
ELECTRICAL CHARACTERISTICS @ T_A = 25°C				
SYMBOL	**CONDITIONS**	**Min**	**Max**	**Unit**
BV_{CBO}	I_{CB} = 100μA	80		Volts
BV_{CEO}	I_{CE} = 10mA	50		Volts
BV_{EBO}	I_{EB} = 10μA	6.0		Volts
I_{CBO}	V_{CB} = 40V		1.0	μA
I_{EBO}	V_{EB} = 5.0V		10	μA
H_{FE}	I_C = 500mA, V_{CE} = 1.0V	35	250	
H_{FE}	I_C = 3.0A, V_{CE} = 5.0V	20		
$V_{CE(SAT)}$*	I_C = 1.5A, I_B = 0.15A		1.0*	Volts

* When assembled in a TO-5 package

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "05"

Typical Device Types: 2N2891



Bonding Pad Areas

Base
(2) 88 x 9 mils

Emitter
(2) 69 x 10 mils

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

5 AMP

Fast Switching

Typical Switching (TO-111 Package)

- t_r = 60nsec
- t_s = 1000nsec
- t_f = 100nsec

Conditions:
V_{CC} = 40V, I_C = 2.0A,
$I_{B1} = I_{B2}$ = 0.2A

ELECTRICAL CHARACTERISTICS @ T_A = 25°C				
SYMBOL	**CONDITIONS**	**Min**	**Max**	**Unit**
BV_{CBO}	I_{CB} = 1.0mA	200		Volts
BV_{CEO}	I_{CE} = 50mA	120		Volts
BV_{EBO}	I_{EB} = 10μA	8.0		Volts
I_{CBO}	V_{CB} = 120V		0.5	μA
I_{EBO}	V_{EB} = 8.0V		10	μA
H_{FE}	I_C = 100mA, V_{CE} = 2.0V	40	120	
H_{FE}	I_C = 3.0A, V_{CE} = 5.0V	40		
$V_{CE(SAT)}$*	I_C = 3.0A, I_B = 0.3A		0.6*	Volts

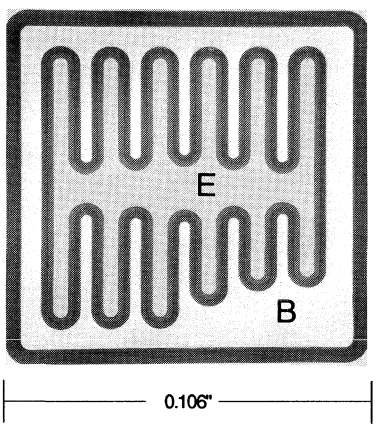
* When assembled in a TO-5 package

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "11"

Typical Device Types: 2N3418 - 2N3421, 2N4150

10 AMP
Fast Switching



Bonding Pad Areas

Base
(1) 31 x 13.5 mils

Emitter
(1) 19 x 10 mils

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

SYMBOL	CONDITIONS	11C-1 Min	11C-1 Max	11C-2 Min	11C-2 Max	Unit
BV_{CBO}	I_{CB} = 1.0mA	200		200		Volts
BV_{CEO}	I_{CE} = 50mA	120		110		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		8.0		Volts
I_{CBO}	V_{CB} =120V		5.0		----	µA
I_{CBO}	V_{CB} = 90V		----		0.5	µA
I_{EBO}	V_{EB} = 8.0V		0.5		0.5	µA
H_{FE}	I_C = 100mA, V_{CE} = 2.0V	40		80		
H_{FE}	I_C = 5.0A, V_{CE} = 5.0V	40		----		
H_{FE}	I_C = 10A, V_{CE} = 5.0V			20		
$V_{CE(SAT)}$*	I_C = 2.0A, I_B = 200mA		0.3*		----	Volts
$V_{CE(SAT)}$*	I_C = 10A, I_B = 1.0A		----		1.2*	Volts

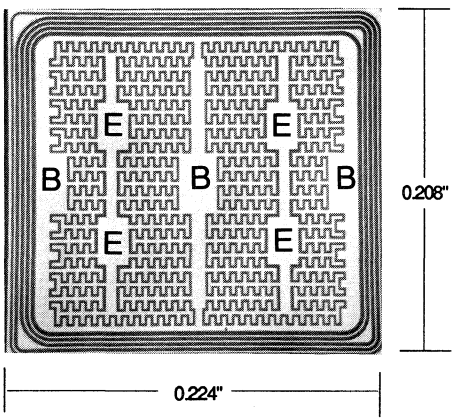
* When assembled in a TO-5 package

TYPICAL SWITCHING @ CONDITIONS							
SYMBOL	11C-1 Ref. 2N3421	11C-2 Ref. 2N4150	Units	SYMBOL	11C-1 Ref. 2N3421	11C-2 Ref. 2N4150	Units
t_d	45	25	nsec	V_{CC}	20	20	V
t_r	65	400	nsec	I_C	1	5	A
t_s	950	600	nsec	I_{B1}	100	500	mA
t_f	70	200	nsec	I_{B2}	100	500	mA

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "21"

Typical Device Types: 2N6653, 2N6654, 2N6655, GSDS50020



Bonding Pad Areas

Base
(3) 34 x 16 mils

Emitter
(4) 26 x 16 mils

• $C^2R^®$ For High Voltage Surface Stabilization

20 - 50 AMP Fast Switching

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

SYMBOL	CONDITIONS	21J Min	21J Max	21M Min	21M Max	Unit
BV_{CBO}	I_{CB} = 1.0mA	380		500		Volts
BV_{CEO}	I_{CE} = 50mA	200		400		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		8.0		Volts
I_{CBO}	V_{CB} =160V, 320V		0.5		0.5	µA
I_{EBO}	V_{EB} = 5.0V		0.5		0.5	µA
H_{FE}	I_C = 15A, V_{CE} = 5.0V			10		
H_{FE} *	I_C = 50A, V_{CE} = 5.0V	8.0*				
$V_{CE(SAT)}$*	I_C = 50/15A, I_B = 10/3A		0.6*		0.6*	Volts
$I_{C(MAX)}$*			60*		25*	Amps

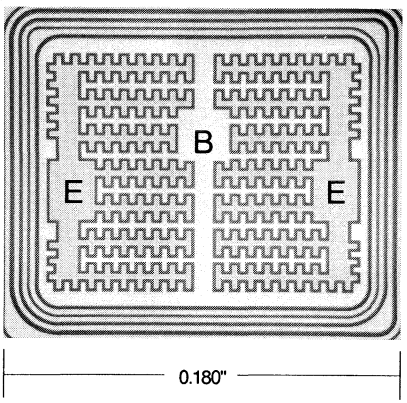
* When assembled in a TO-3 package

TYPICAL SWITCHING (TO-3 Package)				@ CONDITIONS			
SYMBOL	21J	21M	Units	SYMBOL	21J	21M	Units
t_d	20	20	nsec	V_{CC}	90	200	V
t_r	180	180	nsec	I_C	50	15	A
t_s	600	1400	nsec	I_{B1}	10	3.0	A
t_f	150	320	nsec	I_{B2}	10	3.0	A

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "25"

Typical Device Types: GSTU6040, GSTU15020



Bonding Pad Areas

Base
(1) 20 x 20 mils

Emitter
(2) 22 x 16 mils

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

• $C^2R^{®}$ For High Voltage Surface Stabilization

10 - 20 AMP Fast Switching

Typical Switching (TO-3 Package)

- t_d = 20nsec
- t_r = 180nsec
- t_s = 1250nsec
- t_f = 250nsec

Conditions:
V_{CC} = 150V, I_C = 6.0A,
$I_{B1} = I_{B2}$ = 1.2A

Rugged Construction
Excellent Safe Operating Areas

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

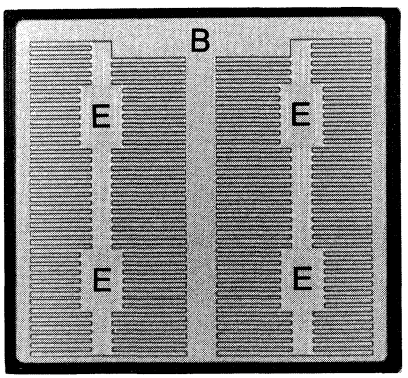
SYMBOL	CONDITIONS	25M Ref. GSTU6040 Min	25M Ref. GSTU6040 Max	25N Ref. GSTU15020 Min	25N Ref. GSTU15020 Max	Unit
BV_{CBO}	I_{CB} = 1.0mA	500		300		Volts
BV_{CEO}	I_{CE} = 50mA	400		200		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		8.0		Volts
I_{CBO}	V_{CB} = 320V, 240V		0.5		0.5	µA
I_{EBO}	V_{EB} = 5.0V		0.5		0.5	µA
H_{FE}	I_C = 100mA, V_{CE} = 5.0V	20		20		
H_{FE}	I_C = 6.0A, V_{CE} = 5.0V	10				
H_{FE}	I_C = 15A, V_{CE} = 5.0V			10		
$V_{CE(SAT)}$*	I_C = 6.0A, I_B = 1.2A		0.5*			Volts
$V_{CE(SAT)}$*	I_C = 15A, I_B = 3.0A				0.8*	Volts

* When assembled in a TO-3 package

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "31"

Typical Device Types: GSRU15040, GSRU20040, 2N6922, 2N6923



Bonding Pad Areas

Base
(1) 106 x 20 mils

Emitter
(4) 37.5 x 23 mils

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

• $C^2R^®$ For High Voltage Surface Stabilization

20 AMP
Ultra Fast Switching

Typical Switching
(TO-3 Package)

- t_d = 20nsec
- t_r = 40nsec
- t_s = 1000nsec
- t_f = 40nsec

Conditions:
V_{CC} = 450V, I_C = 15A,
I_{B1} = 3.0A, I_{B2} = 6.0A

ELECTRICAL CHARACTERISTICS @ T_A = 25°C				
SYMBOL	**CONDITIONS**	**Min**	**Max**	**Unit**
BV_{CBO}**	I_{CB} = 1.0mA	550**		Volts
BV_{CEO}	I_{CE} = 50mA	450		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		Volts
I_{CBO}	V_{CB} = 440V		0.5	µA
I_{EBO}	V_{EB} = 8.0V		0.5	µA
H_{FE}	I_C = 15A, V_{CE} = 5.0V	12		
H_{FE}*	I_C = 20A, V_{CE} = 5.0V	8.0*		
$V_{CE(SAT)}$*	I_C = 15A, I_B = 3.0A		1.0*	Volts

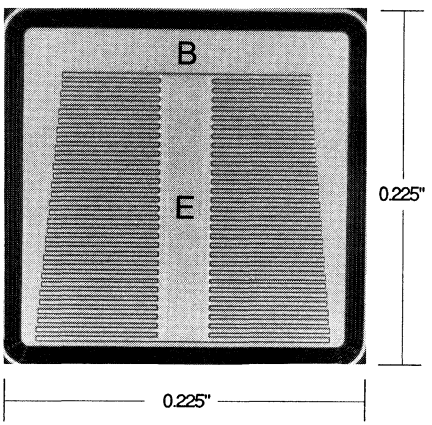
* When assembled in a TO-3 package

** Available with V_{CBO} = 550, 750, 850V

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "35"

Typical Device Types: 2N6920, 2N6921



Bonding Pad Areas

Base
(1) 172 x 23.7 mils

Emitter
(1) 157.5 x 26 mils

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

• $C^2R^®$ For High Voltage Surface Stabilization

Rugged Construction Excellent Safe Operating Areas

15 AMP

Ultra Fast Switching

Typical Switching
(TO-3 Package)

- t_d = 20nsec
- t_r = 90nsec
- t_s = 800nsec
- t_f = 50nsec

Conditions:
V_{CC} = 400V, I_C = 10A,
I_{B1} = 2.0A, I_{B2} = 4.0A

ELECTRICAL CHARACTERISTICS @ T_A = 25°C				
SYMBOL	**CONDITIONS**	**Min**	**Max**	**Unit**
BV_{CBO}**	I_{CB} = 1.0mA	550**		Volts
BV_{CEO}	I_{CE} = 50mA	450		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		Volts
I_{CBO}	V_{CB} = 440V		0.5	µA
I_{EBO}	V_{EB} = 8.0V		0.5	µA
H_{FE}	I_C = 10A, V_{CE} = 5.0V	10		
$V_{CE(SAT)}$*	I_C = 10A, I_B = 2.0A		1.0*	Volts

* When assembled in a TO-3 package

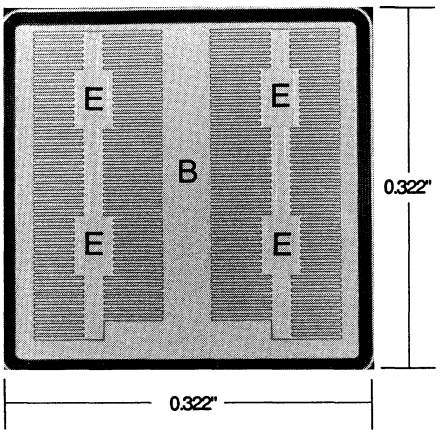
** Available with V_{CBO} = 550, 750, 850V

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "37"

Typical Device Types: 2N6924, 2N6925

35 AMP
Fast Switching



Bonding Pad Areas

Base
(1) 135 x 28 mils

Emitter
(1) 49 x 30 mils

Front Metallization:
Aluminum

Back Metallization:
Gold
or
Chrome-Silver-Gold

Typical Switching
(TO-3 Package)

- t_d = 20nsec
- t_r = 90nsec
- t_s = 1300nsec
- t_f = 150nsec

Conditions:
V_{CC} = 250V, I_C = 25A,
I_{B1} = 5.0A, I_{B2} = 10A

- $C^2R^®$ For High Voltage Surface Stabilization

Rugged Construction
Excellent Safe Operating Areas

ELECTRICAL CHARACTERISTICS @ T_A = 25°C				
SYMBOL	**CONDITIONS**	**Min**	**Max**	**Unit**
BV_{CBO}**	I_{CB} = 1.0mA	550**		Volts
BV_{CEO}	I_{CE} = 50mA	450		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		Volts
I_{CBO}	V_{CB} = 440V		0.5	µA
I_{EBO}	V_{EB} = 8.0V		0.5	µA
H_{FE}*	I_C = 30A, V_{CE} = 5.0V	9.0*		
$V_{CE(SAT)}$*	I_C = 30A, I_B = 6.0A		1.3*	Volts

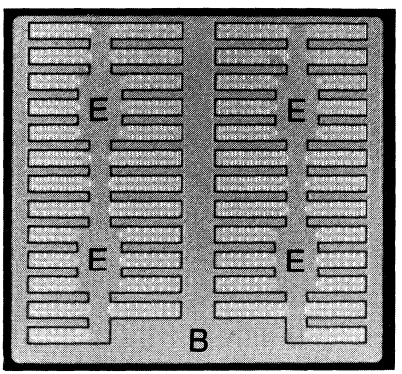
* When assembled in a TO-3 package

** Available with V_{CBO} = 550, 750, 850V

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "39"

Typical Device Types: 2N6274 - 2N6277, 2N6678



Bonding Pad Areas

Base
(1) 109 x 24.5 mils

Emitter
(4) 38 x 23 mils

• $C^2R^®$ For High Voltage Surface Stabilization

Rugged Construction Excellent Safe Operating Areas

20 - 50 AMP Fast Switching

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

SYMBOL	CONDITIONS	39M Min	39M Max	39O Min	39O Max	Unit
BV_{CBO}	I_{CB} = 1.0mA	500		350		Volts
BV_{CEO}	I_{CE} = 50mA	400		170		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		8.0		Volts
I_{CBO}	V_{CB} =480V, 120V		0.5		0.5	µA
I_{EBO}	V_{EB} = 7.0V, 6.0V		0.5		0.5	µA
H_{FE}*	I_C = 15A, V_{CE} = 5.0V	10*				
H_{FE}*	I_C = 50A, V_{CE} = 4.0V			10*		
$V_{CE(SAT)}$*	I_C = 15A, I_B = 3.0A		0.6*			Volts
$V_{CE(SAT)}$*	I_C = 50A, I_B = 10A				1.3*	Volts

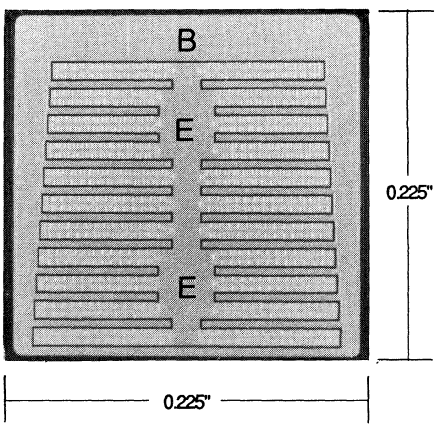
* When assembled in a TO-3 package

TYPICAL SWITCHING (TO-3 Package)				@ CONDITIONS			
SYMBOL	39M	39O	Units	SYMBOL	39M	39O	Units
t_d	30	30	nsec	V_{CC}	200	80	V
t_r	350	300	nsec	I_C	15	20	A
t_s	1900	800	nsec	I_{B1}	3.0	2.0	A
t_f	350	250	nsec	I_{B2}	3.0	2.0	A

General Semiconductor Industries, Inc.

NPN TRANSISTOR CHIP "41"

Typical Device Types: 2N6338 - 2N6341, 2N6584, GSTU30020



Bonding Pad Areas

Base
(1) 65 x 22.5 mils

Emitter
(2) 38 x 23 mils

• $C^2R^®$ For High Voltage Surface Stabilization

Rugged Construction Excellent Safe Operating Areas

10 - 25 - 30 AMP

Fast Switching

Front Metallization: Aluminum

Back Metallization: Gold or Chrome-Silver-Gold

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

SYMBOL	CONDITIONS	41M Min	41M Max	41N Min	41N Max	41O Min	41O Max	Unit
BV_{CBO}	I_{CB} = 1.0mA	500		350		350		Volts
BV_{CEO}	I_{CE} = 50mA	400		200		180		Volts
BV_{EBO}	I_{EB} = 1.0mA	8.0		8.0		8.0		Volts
I_{CBO}	V_{CB} =400V		0.5		----		----	µA
I_{CBO}	V_{CB} =250V		----		0.5		0.5	µA
I_{EBO}	V_{EB} = 8.0V		0.5		0.5		0.5	µA
H_{FE}*	I_C = 10A, V_{CE} = 5.0V	10*		----		----		
H_{FE}*	I_C = 30A, V_{CE} = 5.0V	----		10*		----		
H_{FE}*	I_C = 25A, V_{CE} = 2.0V	----		----		12*		
$V_{CE(SAT)}$*	I_C = 10A, I_B = 2.0A		1.0*		----		----	Volts
$V_{CE(SAT)}$*	I_C = 30A, I_B = 6.0A		----		1.0*		----	Volts
$V_{CE(SAT)}$*	I_C = 25A, I_B = 2.50A		----		----		1.5*	Volts

TYPICAL SWITCHING (TO-3 Package*)					@ CONDITIONS				
SYMBOL	41M	41N	41O	Units	SYMBOL	41M	41N	41O	Units
t_d	25	30	25	nsec	V_{CC}	200	125	80	V
t_r	250	200	100	nsec	I_C	10	30	10	A
t_s	1800	1100	1000	nsec	I_{B1}	2.0	6.0	1.0	A
t_f	300	150	200	nsec	I_{B2}	2.0	6.0	1.0	A

* When assembled in a TO-3 package

Appendix A

Element Evaluation Test Flow

Ref. MIL-STD-883C, Method 5008, para. 3.2.2, Class B.

In addition to 100% visual inspection and electrical probe tests, GSI performs element evaluation of mounted die samples for every transistor chip order, in accordance with the requirements of MIL-STD-883C, Method 5008, para. 3.2.2, Class B (Class S evaluation is available per customer requirements; contact factory).

Evaluation flow:

1. Internal visual inspection (ref. para. 3.2.2.3)

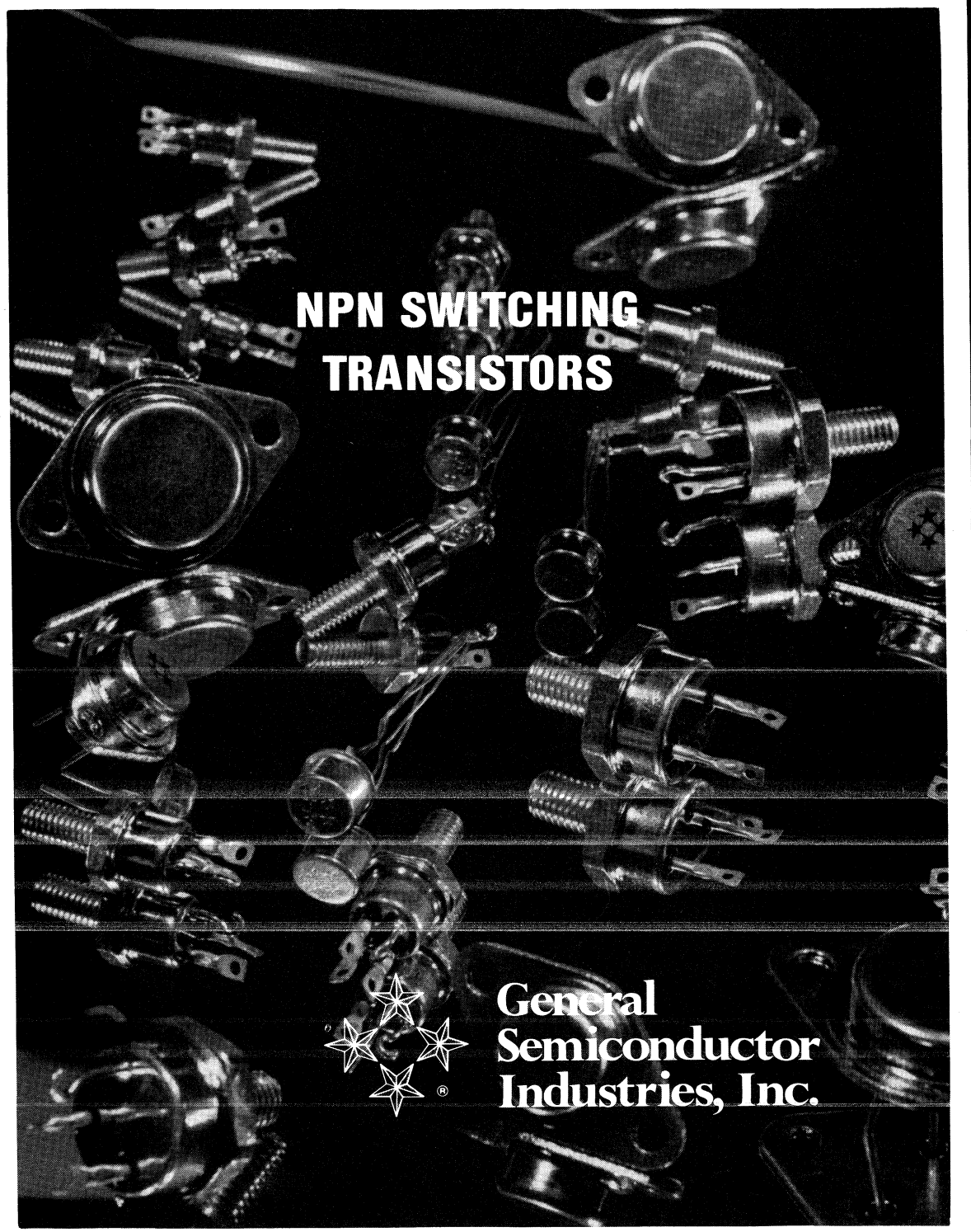
   - per MIL-STD-750, Method 2072
   - Sample Quantity: 10

2. Final electrical tests (ref. para. 3.2.2.1)

   - per the procuring specification

3. Wire bond evaluation (ref. para. 3.2.2.6.2)

   - per MIL-STD-883C, Method 2011
   - Sample quantity: 10 wires


NPN SWITCHING
TRANSISTORS
General
Semiconductor
Industries, Inc.

SWITCHING TRANSISTOR FUNDAMENTALS

The advances in the technology of bipolar switching power transistors have resulted in devices which combine high-voltage capability, speed, and ruggedness previously thought impossible to obtain in a single transistor. As an example, General Semiconductor Industries' 850 volt 2N6925A can switch a 25 ampere inductive load in just 35 nanoseconds (typical crossover time) and yet is rugged enough to switch a 50 ampere clamped inductive load to 550 volts, (RBSOA) without sacrificing the low saturation voltage that makes the bipolar transistor so attractive in switching circuits.

Switching Transistor Key Characteristics

The selection of the proper transistor to optimize reliable and efficient operation in switching circuits is largely dependent upon certain key characteristics. A brief review follows:

I. Blocking Voltage

A. **BV_{CEO}**: BV_{CEO} is the transistor breakdown voltage from collector to emitter with the base lead open. It is the lowest voltage of the collector-emitter breakdown voltages and, dependent upon base drive conditions and safe-operating area, it is often the limit for maximum steady-state voltage in a working circuit.

B. **BV_{CEV}**: BV_{CEV} is the collector-emitter breakdown voltage when the base-emitter junction is reverse-biased. It is the practical upper limit for voltage in any circuit, when operated within the limits of the reverse-bias safe operating area. A snubber circuit may be required to keep the turn-off load line within the limits of the RBSOA when operation is to the limit of the BV_{CEV} rating.

II. On-State Characteristics

A. CURRENT: The key current rating is the **DESIGN CENTER CURRENT** which can be recognized as the current at which most of the switching characteristics are measured. The **CONTINUOUS CURRENT RATING (I_C)** is based on the size of the transistor die, and thermal characteristics and is not usually intended to be the actual operating point of the transistor in a conservative design. The **PEAK CURRENT RATING (I_{CM})** is intended to state an overload condition which the transistor will survive. It is also not intended as an operating point for the transistor.

B. **$V_{CE(sat)}$**: This is the voltage across the transistor when it is fully on. Conditions which must be specified include the collector current, and the base current drive. The maximum $V_{CE(sat)}$ is of prime inportance in determining power loss when the transistor switch is in the on state.

III. Transition State Characteristics

A. Switching Times: Most practical power switching circuits are inductive. During turn-on, the voltage will drop very rapidly while the current rises slowly, as dictated by the circuit inductance. This phase shift minimizes the effect of turn-on times on efficiency with the exception of **DYNAMIC SATURATION TIME (t_{sd})** (See Dynamic Saturation—Its cause and Measurement in Section 5).
During turn-off the phase shift causes the voltage to rise prior to the start of the current fall. This creates a high instantaneous power dissipation in the switch. The significant switching times during turn-off are:

1. Crossover time (t_c); Crossover time is the time from a 10% rise in the voltage waveform until the current has fallen to 10% of the "on" current. Power during turn-off is proportional to t_c.

2. Voltage Rise Time (t_{rv}); This is the time it takes the voltage waveform to rise from 10% to 90% of V_{clamp}.

3. Current Fall Time (t_{fi}); This is the time it takes the collector current to fall from 90% to 10% of the I_C peak.

4. Voltage Storage Time (t_{sv}); This is the time interval between the removal or reversal of base drive and the rise of collector voltage to 10% of V_{clamp}.

B. Safe Operating Area

1. Reverse Biased Safe Operating Area (RBSOA): The RBSOA graph gives a more complete picture of the switching capabilities of a transistor than either the voltage or current specifications by themselves. The RBSOA is the critical characteristic in determining the reliability of a transistor in the inductive switching environment characteristic of switchmode power supplies.

2. Forward Biased Safe Operating Area: For a transitor switch the FBSOA is a less important characteristic than the RBSOA since it will spend most of its time either on or off and will switch through the area of the FBSOA graph only during turn-on. Also, for a switch, the DC FBSOA is of no importance at all. A pulsed FBSOA (10μs or less) is applicable for switches, but is usually not specified on the data sheet since most transistors can handle the peak rated current at peak rated V_{CEO} limit for at least 10μs.

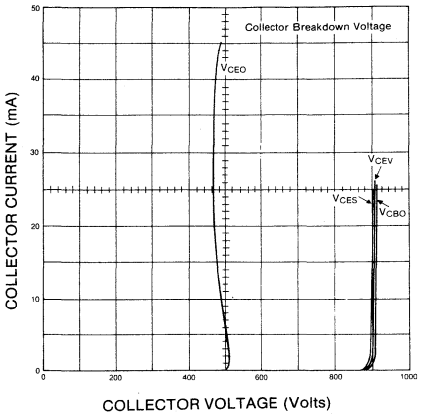


Figure 1—Avalanche Characteristics

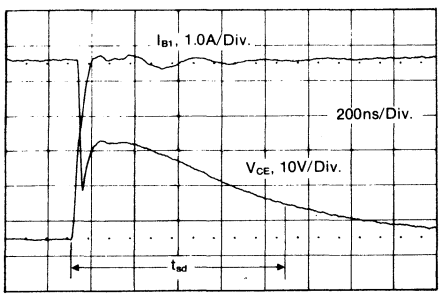


Figure 2—Dynamic Saturation Waveforms

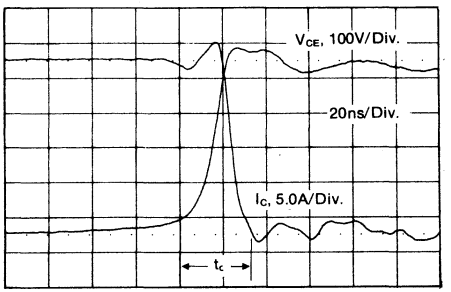


Figure 3—Crossover Waveforms

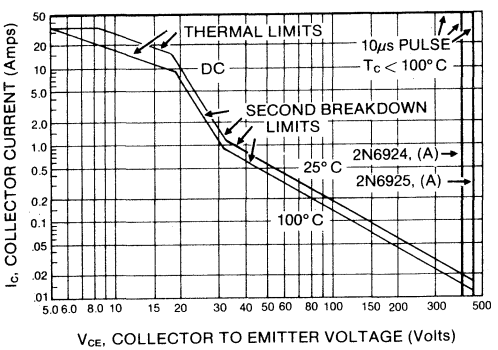


Figure 4—Forward Biased Safe Operating Area

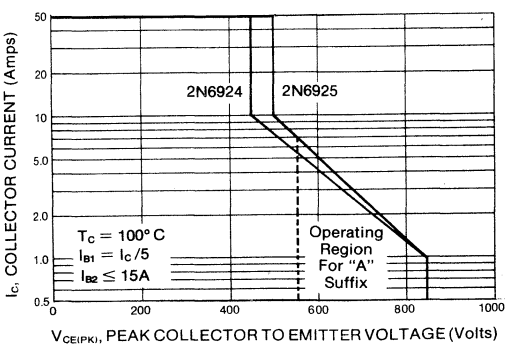


Figure 5—Reverse Bias Safe Operating Area

Ic = 2.0 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N4300	TO-5	80	100	8.0	15.0	30	120	1.0	2.0	0.3	1.0	0.1	30	10.0	90	
2N4863	TO-5	120	140	8.0	4.0	50	150	0.5	5.0	1.5	2.0	0.2	50	0.1	60	3-18
2N4864	TO-66	120	140	8.0	16.0	50	150	0.5	5.0	1.5	2.0	0.2	50	0.1	60	3-18
2N5148	TO-39	80	100	6.0	40.0	30	90	1.0	5.0	0.46	1.0	0.1	50	1.0	60	3-31
2N5150	TO-39	80	100	6.0	4.0	70	200	1.0	5.0	0.46	1.0	0.1	60	0.1	60	3-19

Ic = 3.0 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N3418	TO-5	60	85	8.0	15.0	20	60	1.0	2.0	0.25	1.0	0.1	40.0	0.5	80	3-8
2N3419	TO-5	80	125	8.0	15.0	20	60	1.0	2.0	0.25	1.0	0.1	40.0	0.5	120	3-8
2N3420	TO-5	60	85	8.0	15.0	40	120	1.0	2.0	0.25	1.0	0.1	40.0	0.5	80	3-8
2N3421	TO-5	80	125	8.0	15.0	40	120	1.0	2.0	0.25	1.0	0.1	40.0	0.5	120	3-8
2N3506	TO-39	40	60	5.0	2.6	40	200	1.5	2.0	1.0	1.5	0.15	60.0			3-10
2N3507	TO-39	50	80	5.0	2.6	30	150	1.5	2.0	1.0	1.5	0.15	60.0			3-10
2N4877	TO-5	60	70	5.0	5.7	20	100	2.0	1.0	1.0	0.4	0.4	30.0	100	70	
2N5334	TO-39	60	60	8.0	3.4	30	150	1.0	2.0	0.7	2.0	0.2	40.0	5.0	60	
2N5335	TO-39	80	80	8.0	3.4	15		2.0	2.0	0.7	2.0	0.2	40.0	5.0	80	
XGS7001	TO-39	30	50	5.0	2.9	20		2.0	2.0	1.0	1.0	0.1	120.0	10	30	3-87
XGS7002	TO-39	60	70	5.0	2.9	15		2.0	2.0	1.0	1.0	0.1	120.0	10	40	3-87

Ic = 5.0 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N2657	TO-5	60	80	7.0	4.0	40	120	1.0	2.0	0.5	1.0	0.1	20	0.1	60	
2N2658	TO-5	80	100	7.0	4.0	40	120	1.0	2.0	0.5	1.0	0.1	20	0.1	60	
2N2890	TO-5	80	100	5.0	3.0	30	90	1.0	2.0	0.5	1.0	0.1	30	0.1	60	
2N2891	TO-5	80	100	5.0	3.0	50	150	1.0	2.0	0.5	1.0	0.1	30	0.1	60	
2N3996	TO-111/Iso	80	100	8.0	30.0	40	120	1.0	2.0	0.25	1.0	0.1	40	5.0	90	3-12
2N3997	TO-111/Iso	80	100	8.0	30.0	80	240	1.0	2.0	0.25	1.0	0.1	40	5.0	90	3-12
2N3998	TO-111	80	100	8.0	30.0	40	120	1.0	2.0	0.25	1.0	0.1	40	5.0	90	3-12
2N3999	TO-111	80	100	8.0	30.0	80	240	1.0	2.0	0.25	1.0	0.1	40	5.0	90	3-12
2N4150	TO-5	80	100	5.0	5.0	40	120	5.0	5.0	0.6	5.0	0.5	15	0.1	60	3-16
2N5152	TO-39	80	100	6.0	6.0	30	90	2.5	5.0	1.5	5.0	0.5	60	1.0	60	
2N5154	TO-39	80	100	6.0	6.0	70	200	2.5	5.0	1.5	5.0	0.5	70	1.0	60	
2N5336	TO-39	80	80	6.0	3.4	30	120	2.0	2.0	0.7	2.0	0.2	30	10	80	
2N5337	TO-39	80	80	6.0	3.4	60	240	2.0	2.0	0.7	2.0	0.2	30	10	80	
2N5338	TO-39	100	100	6.0	3.4	30	120	2.0	2.0	0.7	2.0	0.2	30	10	100	
2N5339	TO-39	100	100	6.0	3.4	60	240	2.0	2.0	0.7	2.0	0.2	30	10		
2N5487	TO-5/S	80	120	8.0	15.0	100	300	1.0	2.0	0.25	1.0	0.1	40			
2N5487-1	TO-5	80	120	8.0	15.0	100	300	1.0	2.0	0.25	1.0	0.1	40			
2N5488	TO-5/S	100	150	8.0	15.0	40	120	1.0	2.0	0.25	1.0	0.1	40			
2N5488-1	TO-5	100	150	8.0	15.0	40	120	1.0	2.0	0.25	1.0	0.1	40			
GSTU4030	TO-3	300	350	7.0	62.5	10		4.0	5.0	0.8	4.0	0.8	25	1000	280	3-75
GSTU4035	TO-3	350	400	7.0	62.5	10		4.0	5.0	0.8	4.0	0.8	25	1000	320	3-75
GSTU4040	TO-3	400	450	7.0	62.5	10		4.0	5.0	0.8	4.0	0.8	25	1000	360	3-75

Available in JAN and JANTX(V)

Ic = 7.0 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6579	TO-204	350	450	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.0	50			3-27
2N6580	TO-204	400	500	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.0	50			3-27
2N6581	TO-204	450	550	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.0	50			3-27
2N6585	TO-61/Iso	350	450	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.4	50			
2N6586	TO-61/Iso	500	500	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.4	50			
2N6587	TO-61/Iso	450	550	9.0	71.4	7 -	35	5.0	3.0	1.5	5.0	1.4	50			3-39
2N6671	TO-204	300	450	8.0	8.5	10 -	40	5.0	3.0	1.0	5.0	1.4	60			3-39
2N6672	TO-204	350	550	8.0	85.0	10 -	40	5.0	3.0	1.0	5.0	1.0	60			3-39
2N6673	TO-204	400	650	8.0	85.0	10 -	40	5.0	3.0							
GSTU6030	TO-3	300	350	7.0	62.5	10		6.0	5.0	0.8	6.0	1.2	25	500	280	3-81
GSTU6035	TO-3	350	400	7.0	62.5	10		6.0	5.0	0.8	6.0	1.2	25	500	320	3-81
GSTU6040	TO-3	400	450	7.0	62.5	10		6.0	5.0	0.8	6.0	1.2	25	500	360	3-81

Ic = 7.5 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6582	TO-204	350	450	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			3-29
2N6583	TO-204	400	500	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			3-29
2N6584	TO-204	450	550	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			3-29
2N6588	TO-61/Iso	350	450	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			
2N6589	TO-61/Iso	400	500	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			
2N6590	TO-61/Iso	450	550	9.0	71.4	7 -	35	7.0	3.0	1.5	7.0	1.4	50			

Ic = 10 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6232	TO-5	100	140	7.0	15.0	25 -	100	5.0	2.0	1.4	10.0	1.0	30	0.2	140	3-21
2N6674	TO-3	300	450	7.0	100.0	8 -	20	10.0	2.0	1.0	10.0	2.0	15	100	450	
2N6675	TO-3	400	450	7.0	100.0	8 -	20	10.0	2.0	1.0	10.0	2.0	15	100	650	
2N6689	TO-61/Iso	300	450	7.0	100.0	8 -	20	10.0	2.0	1.0	10.0	2.0	15	100	450	
2N6690	TO-61/Iso	400	650	7.0	100.0	8 -	20	10.0	2.0	1.0	10.0	2.0	15	100	650	
GSTU8035	TO-3	350	400	7.0	94.0	10		8.0	5.0	0.8	8.0	1.6	25	320	500	3-79
GSTU8040	TO-3	400	450	7.0	94.0	10		8.0	5.0	0.8	8.0	1.6	25	360	500	3-79
GSTU8045	TO-3	450	500	7.0	94.0	10		8.0	5.0	0.8	8.0	1.6	25	400	500	3-79

Ic = 15 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6546	TO-3	300	650	9.0	100	6 -	30	10	2.0	1.5	10	2.0	6	1000	650	
2N6547	TO-3	300	850	9.0	100	6 -	30	10	2.0	1.5	10	2.0	6	1000	850	
2N6676	TO-204	300	450	8.0	175	8		15	3.0	1.0	15	3.0	15	100	450	3-41
2N6677	TO-204	350	550	8.0	175	8		15	3.0	1.0	15	3.0	15	100	550	3-41
2N6678	TO-204	400	650	8.0	175	8		15	3.0	1.0	15	3.0	15	100	650	3-41
2N6691	TO-61/Iso	300	450	8.0	100	8		15	3.0	1.5	15	3.0	15	100	450	3-41
2N6692	TO-61/Iso	350	550	8.0	100	8		15	3.0	1.5	15	3.0	15	100	550	3-41
2N6693	TO-61/Iso	400	650	8.0	100	8		15	3.0	1.5	15	3.0	15	100	650	3-41
2N6920	TO-3	400	550	8.0	100	8		10	2.0	1.0	10	2.0	20	1000	550	3-43
2N6920A	TO-3	450	850	8.0	100	8		10	2.0	1.0	10	2.0	20	1000	850	3-43
2N6921	TO-3	400	550	8.0	100	8		10	2.0	1.0	10	2.0	20	1000	550	3-43
2N6921A	TO-3	450	850	8.0	100	8		10	2.0	1.0	10	2.0	20	1000	850	3-63
GSRU10030	TO-204	300	400	8.0	100	10		10	5.0	1.0	10	2.0	20	500	320	3-63
GSRU10035	TO-204	350	450	8.0	100	10		10	5.0	1.0	10	2.0	20	500	360	3-63
GSRU10040	TO-204	400	500	8.0	100	10		10	5.0	1.0	10	2.0	20	500	400	3-65
GSTU10030	TO-204	300	400	8.0	100	8		10	5.0	1.0	10	2.0	25	100	320	3-81
GSTU10035	TO-204	350	450	8.0	100	8		10	5.0	1.0	10	2.0	25	100	360	3-81
GSTU10040	TO-204	400	500	8.0	100	8		10	5.0	1.0	10	2.0	25	100	400	3-81
XGSR10030	TO-3	300	350	7.0	100	10		10	5.0	0.8	10	2.0	25	500	280	3-88
XGSR10030-I	TO-3/Iso	300	350	7.0	100	10		10	5.0	0.8	10	2.0	25	500	280	3-88
XGSR10035	TO-3	350	400	7.0	100	10		10	5.0	0.8	10	2.0	25	500	320	3-88
XGSR10035-I	TO-3/Iso	350	400	7.0	100	10		10	5.0	0.8	10	2.0	25	500	320	3-88
XGSR10040	TO-3	400	450	7.0	100	10		10	5.0	0.8	10	2.0	25	500	360	3-88
XGSR10040-I	TO-3/Iso	400	450	7.0	100	10		10	5.0	0.8	10	2.0	25	500	360	3-88

Ic = 20 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6653	TO-3	300	350	7.0	75	10		15	2.0	0.6	15	3.0	25	100	280	3-31
2N6654	TO-3	350	400	7.0	75	10		15	2.0	0.6	15	3.0	25	100	320	3-31
2N6655	TO-3	400	450	7.0	75	10		15	2.0	0.8	15	3.0	25	100	360	3-31
2N6922	TO-3	400	550	8.0	125	8		15	2.0	1.0	15	3.0	15	1000	550	3-47
2N6922A	TO-3	400	850	8.0	125	8		15	2.0	1.0	15	3.0	15	1000	850	3-47
2N6923	TO-3	450	550	8.0	125	8		15	2.0	1.0	15	3.0	15	1000	550	3-47
2N6923A	TO-3	450	850	8.0	125	8		15	2.0	1.0	15	3.0	15	1000	850	3-47
GSRU14040	TO-3	400	500	8.0	175	10		14	5.0	1.0	14	3.0	15	10	400	3-64
GSRU15030	TO-3	300	400	8.0	100	10		15	5.0	1.0	15	3.0	25	100	320	3-69
GSRU15035	TO-3	350	450	8.0	100	10		15	5.0	1.0	15	3.0	25	100	360	3-69
GSRU15040	TO-3	400	500	8.0	100	10		15	5.0	1.0	15	3.0	25	100	400	3-69
GSTU15018	TO-3	180	250	7.0	80	10		15	5.0	0.8	15	3.0	25	500	200	3-83
GSTU15020	TO-3	200	300	7.0	80	10		15	5.0	0.8	15	3.0	25	500	180	3-83
GSTU15030	TO-3	300	400	8.0	100	10		15	5.0	1.0	15	3.0	25	100		
GSTU15035	TO-3	350	450	8.0	100	10		15	5.0	1.0	15	3.0	25	100		
GSTU15040	TO-3	400	500	8.0	100	10		15	5.0	1.0	15	3.0	25	100		
XGSR15030	TO-3	300	350	7.0	75	10		15	5.0	0.6	15	3.0	25	500	280	3-31
XGSR15030-I	TO-3/Iso	300	350	7.0	75	10		15	5.0	0.6	15	3.0	25	500	280	3-31
XGSR15035	TO-3	350	400	7.0	75	10		15	5.0	0.6	15	3.0	25	500	320	3-31
XGSR15035-I	TO-3/Iso	350	400	7.0	75	10		15	5.0	0.6	15	3.0	25	500	320	3-31
XGSR15040	TO-3	400	450	7.0	75	10		15	5.0	0.8	15	3.0	25	500	360	3-31
XGSR15040-I	TO-3/Iso	400	450	7.0	75	10		15	5.0	0.8	15	3.0	25	500	360	3-31

Ic = 25 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6338	TO-3	100	120	6.0	114	30	120	10	2.0	1.8	25	2.5	40	10	100	3-23
2N6339	TO-3	120	140	6.0	114	30	120	10	2.0	1.8	25	2.5	40	10	120	3-23
2N6340	TO-3	140	160	6.0	114	30	120	10	2.0	1.8	25	2.5	40	10	140	3-23
2N6341	TO-3	150	180	6.0	114	30	120	10	2.0	1.8	25	2.5	40	10	150	3-23
GSRU20030	TO-204	300	400	8.0	114	8		20	5.0	1.5	20	4.0	20	100	320	3-73
GSRU20035	TO-204	350	450	8.0	114	8		20	5.0	1.5	20	4.0	20	100	360	3-73
GSRU20040	TO-204	400	500	8.0	114	8		20	5.0	1.5	20	4.0	20	100	400	3-73

Ic = 30 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N4002	TO-63	80	80	8.0	100	20	80	30.0	4.0	1.2	30	15	15	1.0mA	90	3-14
2N4003	TO-63	100	100	8.0	100	20	80	4.0	4.0	1.2	30	15	15	1.0mA	110	3-14

Ic=35AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@V_{CE} VOLTS	DATA SHEET PG. NO.
2N6924	TO-3	400	550	8.0	172	8		25	2.0	1.0	25	5.0	15	1000	550	3-53
2N6924A	TO-3	400	850	8.0	172	8		25	2.0	1.0	25	5.0	15	1000	850	3-53
2N6925	TO-3	450	550	8.0	172	8		25	2.0	1.0	25	5.0	15	1000	550	3-53
2N6925A	TO-3	450	850	8.0	172	8		25	2.0	1.0	25	5.0	15	1000	850	3-53

Ic = 40 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
GSTU30018	TO-3	180	250	7.0	100	10		30	5.0	1.0	30	6.0	25	500	144	3-85
GSTU30020	TO-3	200	300	7.0	100	10		30	5.0	1.0	30	6.0	25	500	160	3-85

Ic = 50 AMPS

DEVICE TYPE	PACKAGE	BV_{CEO} VOLTS	BV_{CBO}/ BV_{CEV} VOLTS	BV_{EBO} VOLTS	P_D @ 100°C WATTS	h_{FE} @ Min.	Max.	I_C AMPS	V_{CE} VOLTS	$V_{CE(sat)}$ VOLTS	@ I_C AMPS	I_B AMPS	f_T MHz	I_{CBO}/ I_{CEV} uAMP	@ V_{CB} VOLTS	DATA SHEET PG. NO.
2N6274	TO-3 (Mod)	100	120	6.0	143	30	120	20	4.0	1.0	20	2.0	30	10	120	3-22
2N6277	TO-3 (Mod)	150	180	6.0	143	30	120	20	4.0	1.0	20	2.0	30	10	180	3-22
GSDS50018	TO-3 (Mod)	180	180	7.0	100	8		50	4.0	1.0	50	10.0	30	10	200	3-57
GSDS50020	TO-3 (Mod)	200	200	7.0	100	8		50	4.0	1.0	50	10.0	30	10	200	3-57

Available in JAN and JANTX(V)

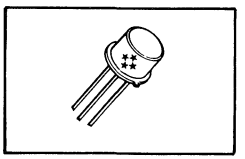
General Semiconductor Industries, Inc.

2N3418
2N3419
2N3420
2N3421

NPN SILICON POWER TRANSISTORS

DIFFUSED SILICON EPITAXIAL PASSIVATED TRANSISTOR

These NPN devices are designed for use in high speed switching and medium power amplifier applications. JAN, JANTX, and JANTXV devices to MIL-S-19500/393 are available. The latest technologies are used to offer the highest degree of reliability.

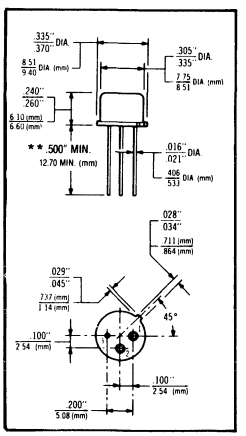


FEATURES

- **Fast Switching**
- **High Power Dissipation**
- **Low Leakage Current**
- **Low Saturation Voltage**

APPLICATIONS

- **Switching Regulators**
- **High Frequency Inverters**
- **Converters**
- **DC-RF Amplifiers**



**Also available in 1.5" lead length.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures		
Storage Temperature	−65°C to +200°C	
Operating Junction Temperature	+200°C	
Lead Temperature (Soldering, 60 second time limit)	+300°C	
Maximum Power Dissipation		
Total Dissipation at 100°C Case Temperature	15 Watts	
Linear Derating Factor	0.15 W/°C	
	2N3418 2N3420	**2N3419 2N3421**
Maximum Voltages and Current		
V_{CEO} Collector to Emitter Voltage	60 Volts	80 Volts
V_{CBO} Collector to Base Voltage	85 Volts	125 Volts
V_{EBO} Emitter to Base Voltage	8 Volts	8 Volts
I_C Collector Current	3 Amps	3 Amps

MECHANICAL CHARACTERISTICS

Case: TO-5 Package
Weight: 1.8 grams (maximum)
Leads: Gold Plated Kovar
1. Emitter 2. Base 3. Collector
Body marked with Logo and type number

*ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N3418 2N3420 MIN.	2N3418 2N3420 MAX.	2N3419 2N3421 MIN.	2N3419 2N3421 MAX.	UNITS
†Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	I_C = 50mA, I_E = 0	60		80		Volts
Collector Cutoff Current	I_{CEX}	V_{CE} = 80V, V_{BE} = -0.5V		0.5			μ Amps
		V_{CE} = 120V, V_{BE} = -0.5V				0.5	μ Amps
Emitter Cutoff Current	I_{EBO}	V_{EB} = 6V, I_C = 0		0.5		0.5	μ Amps
		V_{EB} = 8V, I_C = 0		10		10	μ Amps
†Collector Saturation Voltage	$V_{CE(sat)}$	I_C = 1A, I_B = 100mA		0.25		0.25	Volts
		I_C = 2A, I_B = 200mA		0.5		0.5	Volts
†Base Saturation Voltage	$V_{BE(sat)}$	I_C = 1A, I_B = 100mA	0.6	1.2	0.6	1.2	Volts
		I_C = 2A, I_B = 200mA	0.7	1.4	0.7	1.4	Volts
†DC Current Gain (2N3418/19)	h_{FE}	I_C = 1A, V_{CE} = 2V	20 MIN.	60 MAX.			
†DC Current Gain (2N3420/21)	h_{FE}	I_C = 1A, V_{CE} = 2V	40 MIN.	120 MAX.			

*JEDEC registered data. † Pulse Conditions: Width = 10μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

*DYNAMIC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N3418 2N3420 MIN.	2N3418 2N3420 MAX.	2N3419 2N3421 MIN.	2N3419 2N3421 MAX.	UNITS
Turn-On Time	t_{on}	See Figure 2		0.3		0.3	μSec
Turn-Off Time	t_{off}	See Figure 2		1.2		1.2	μSec
Collector Base Capacitance	C_{ob}	V_{CE}=10V, f=1MHz		150		150	pF
Collector Gain-Bandwidth Product	f_T	I_C=.1A, V_{CE}=10V, f=20MHz	40		40		MHz

*JEDEC registered data.

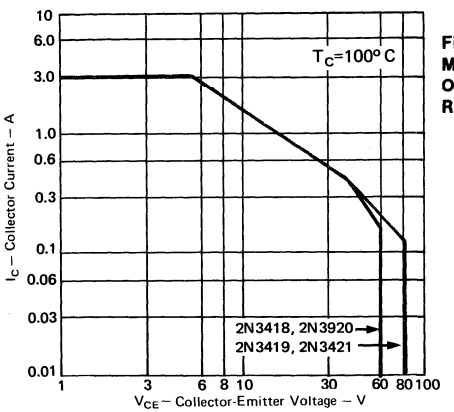


Figure 1
MAXIMUM SAFE OPERATING REGION

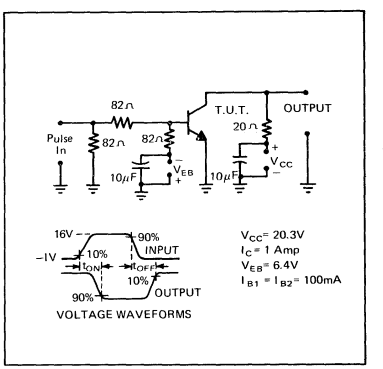


Figure 2
SWITCHING CIRCUIT

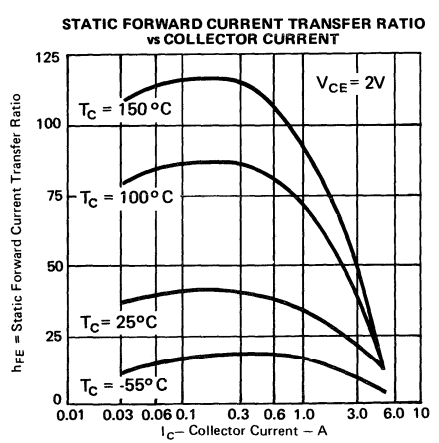


Figure 3
TYPICAL DC CURRENT GAIN (2N3418 - 2N3419)

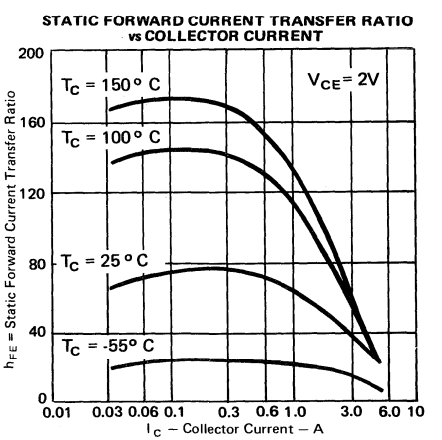


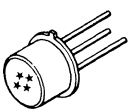
Figure 4
TYPICAL DC CURRENT GAIN (2N3420 - 2N3421)

General Semiconductor Industries, Inc.

2N3506
2N3507
NPN SILICON SWITCHING TRANSISTORS

DIFFUSED SILICON EPITAXIAL PASSIVATED TRANSISTOR

These devices are designed for use in high-current, high-speed, saturated switching and core driver applications. The latest technologies are used to offer the highest degree of reliability. JAN, JANTX, & JANTXV to MIL-S-19500/349 are available.



TO-39

FEATURES

- **Fast Switching**
- **Low Saturation Voltage**
- **Minimum f_T of 60 MHz**
- **Low Leakage Current**

APPLICATIONS

- **High speed Switching Regulated Power Supplies**
- **Converters**
- **Inverters**
- **Core Drivers**

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −65°C to +200°C
Operating Junction Temperature ..... +200°C
Lead Temperature (soldering, 60 second time limit) ..... +300°C

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature ..... .5 Watts
Linear Derating Factor ..... 28.6 mW/°C

Maximum Voltages and Current		2N3506	2N3507
V_{CEO}	Collector to Emitter Voltage	40 Volts	50 Volts
V_{CBO}	Collector to Base Voltage	60 Volts	80 Volts
V_{EBO}	Emitter to Base Voltage	5 Volts	5 Volts
I_C	Collector Current	3 Amps	3 Amps

MECHANICAL CHARACTERISTICS

TO-39 Package

Weight: 1.8 grams (approximate)
Lead material: Kovar with Gold Plating
Pin 1. Emitter 2. Base 3. Collector
Body marked with Logo ⁘ and part number

*ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N3506 MIN.	2N3506 MAX.	2N3507 MIN.	2N3507 MAX.	UNITS
Collector to Base Breakdown Voltage	BV_{CBO}	I_C =100μA, I_E =0	60		80		Volts
†Collector to Emitter Breakdown Voltage	BV_{CEO}	I_C =10mA, I_B =0	40		50		Volts
Emitter to Base Breakdown Voltage	BV_{EBO}	I_E =10μA, I_C =0	5		5		Volts
†DC Current Gain	h_{FE}	I_C=500mA, V_{CE}=1V	50		35		
†DC Current Gain	h_{FE}	I_C=1.5A, V_{CE}=2V	40	200	30	150	
†DC Current Gain	h_{FE}	I_C=2.5A, V_{CE}=3V	30		25		
†DC Current Gain	h_{FE}	I_C=3A, V_{CE}=5V	25		20		
†Collector Saturation Voltage	$V_{CE\ (SAT)}$	I_C=1.5A, I_B=150mA		1.0		1.0	Volts
		I_C=2.5A, I_B=250mA		1.5		1.5	Volts
†Base Saturation Voltage	$V_{BE\ (SAT)}$	I_C=1.5A, I_B=150mA	0.9	1.4	0.9	1.4	Volts
		I_C=2.5A, I_B=250mA		2.0		2.0	Volts
Collector Cutoff Current	I_{CEX}	V_{CE}= 40V, V_{EB} = 4V		1.0			μ Amps
		V_{CE}= 60V, V_{EB} = 4V				1.0	μ Amps
Base Cutoff Current	I_{BL}	V_{CE}= 40V, V_{EB} = 4V		1.0			μ Amps
		V_{CE}= 60V, V_{EB} = 4V				1.0	μ Amps

*JEDEC registered data. † Pulse Conditions: Width = 10μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

*DYNAMIC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNITS
Delay Time	t_d	See Figure 2		15	nSec
Rise Time	t_r	See Figure 2		30	nSec
Storage Time	t_s	See Figure 2		55	nSec
Fall Time	t_f	See Figure 2		35	nSec
Collector Base Capacitance (f=1.0MHz)	C_{OB}	V_{CE}=10V, I_E=0		40	pF
Current Gain - Bandwidth Product (f=20MHz	f_T	I_C=100mA, V_{CE}=5V	60		MHz

*JEDEC registered data.

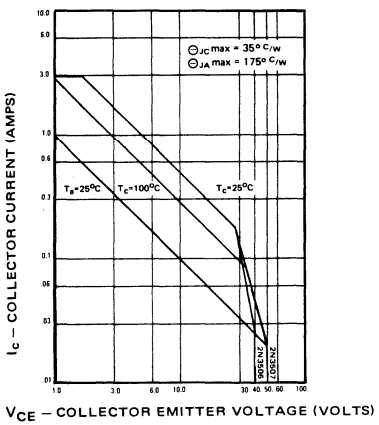


Figure 1 MAXIMUM SAFE OPERATION REGION

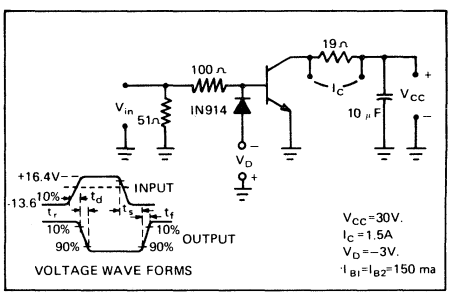


Figure 2 SWITCHING CIRCUIT

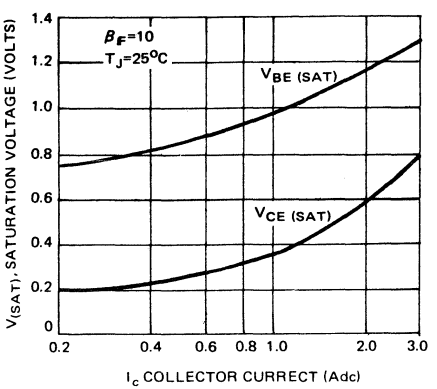


Figure 3 SATURATION VOLTAGES

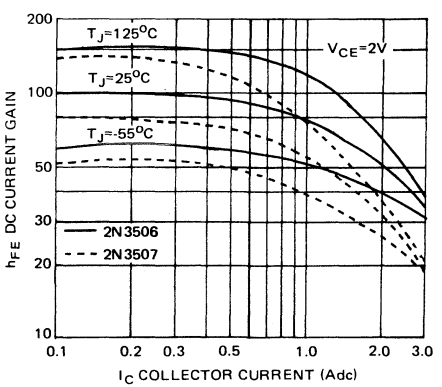


Figure 4 DC CURRENT GAIN

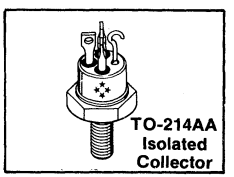
General Semiconductor Industries, Inc.

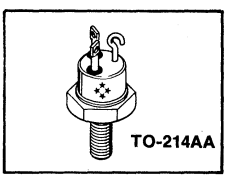
2N3996
2N3997
2N3998
2N3999

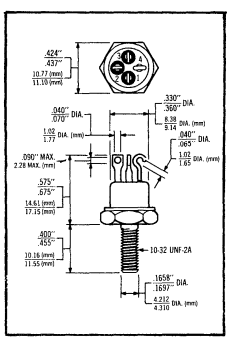
NPN SILICON HIGH POWER TRANSISTORS

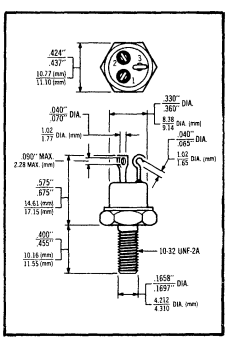
DIFFUSED SILICON EPITAXIAL PASSIVATED TRANSISTOR

These devices are designed for use in power amplifiers and high speed switching applications. The latest technologies are used to offer the highest degree of reliability.









FEATURES

- **Low Saturation Voltage**
- **Minimum f_T of 40 MHz**
- **Fast Switching**
- **Low Leakage Current**
- **Isolated Collector** (2N3996, 2N3997)

APPLICATIONS

- **High Frequency Inverters**
- **Converters**
- **Linear Amplifiers**
- **High Speed Switching Regulated Power Supplies**
- **RF Power Amplifiers**

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter Voltage	V_{CEO}	80 Volts
Collector to Base Voltage	V_{CBO}	100 Volts
Emitter to Base Voltage	V_{EBO}	8 Volts
Collector Current – Continuous	I_C	5 Amps
– Peak	$I_{C\ (Peak)}$	10 Amps
Base Current – Continuous	I_B	1 Amp
Total Device Dissipation, @ $T_C = 100°C$	P_D	30 Watts
Linear Derating Factor		.3W/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−65°C to +200°C
Thermal Resistance – Junction to Case	θ_{JC}	3.33°C/W
– Junction to Ambient	θ_{JA}	87.5°C/W

MECHANICAL CHARACTERISTICS

Case: TO-111/I (2N3996/7); TO-111 (2N3998/9)
1. Emitter 2. Base 3. Collector 4. Case
Body marked with Logo and type number
Weight: 5.3 grams (Approx.)

*ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N3996 2N3998 MIN	2N3996 2N3998 MAX	2N3997 2N3999 MIN	2N3997 2N3999 MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CEO}	†I_C = 50mA, I_B = 0	80		80		Volts
Collector Cutoff Current	I_{CEO}	V_{CE} = 60V, I_B = 0		10		10	μAmp
	I_{CES}	V_{CE} = 90V, V_{BE} = 0V		5.0		5.0	μAmp
		V_{CE} = 90V, V_{BE} = 0V @ T_C 150°C		50		50	μAmp
Emitter Cutoff Current	I_{EBO}	V_{EB} = 5V, I_C = 0		0.5		0.5	μAmp
		V_{EB} = 8V, I_C = 0		10		10	μAmp
DC Current Gain	h_{FE}	I_C = 50mA, V_{CE} = 2V	30		60		
		†I_C = 1A, V_{CE} = 2V	40	120	80	240	
		†I_C = 5A, V_{CE} = 5V	15		20		
		†I_C = 1A, V_{CE} = 2V @ T_C −55°C	10		20		
Collector Saturation Voltage	$V_{CE\ (sat)}$	†I_C = 1A, I_B = 0.1A		0.25		0.25	Volts
		†I_C = 5A, I_B = 0.5A		2.0		2.0	Volts
Base Emitter Saturation Voltage	$V_{BE\ (sat)}$	†I_C = 1A, I_B = 0.1A	0.6	1.2	0.6	1.2	Volts
		†I_C = 5A, I_B = 0.5A		1.6		1.6	Volts

* DYNAMIC CHARACTERISTICS

Turn-on Time	t_{on}	See Figure 1		0.3		0.3	μsec
Turn-off Time	t_{off}	See Figure 1		1.5		2.0	μsec
Collector Base Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz		150		150	pF
High Frequency Current Gain	$\|h_{fe}\|$	V_{CE} = 5V, I_C = 1.0A, f = 10MHz	4		4		

*JEDEC registered data. † Pulse Conditions: Width = 10μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

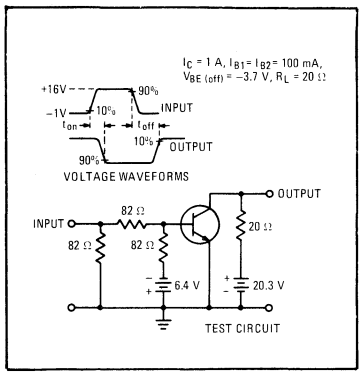


Figure 1
SWITCHING CIRCUIT

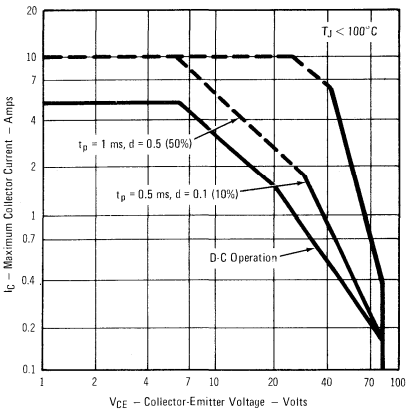


Figure 2
MAXIMUM SAFE OPERATING REGION

TYPICAL CHARACTERISTICS

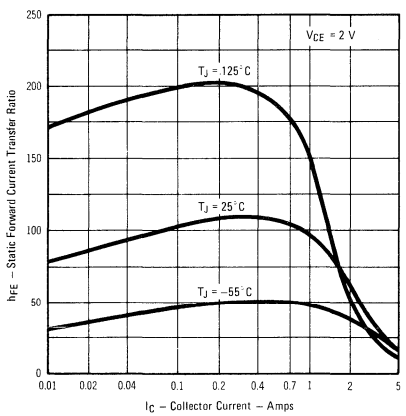


Figure 3
STATIC FORWARD CURRENT TRANSFER RATIO (2N3996, 2N3998)

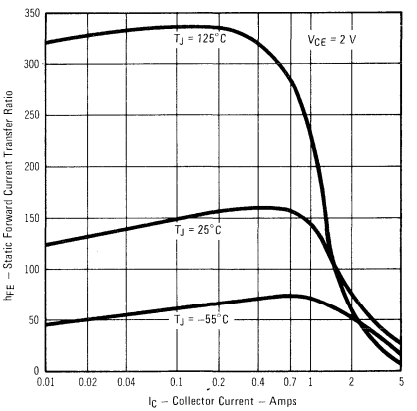


Figure 4
STATIC FORWARD CURRENT TRANSFER RATIO (2N3997, 2N3999)

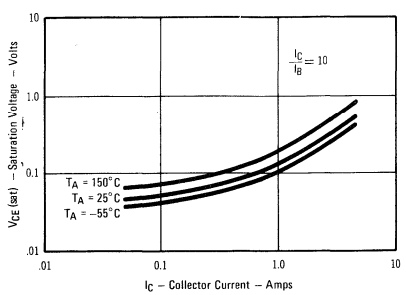


Figure 5
COLLECTOR TO EMITTER VOLTAGE

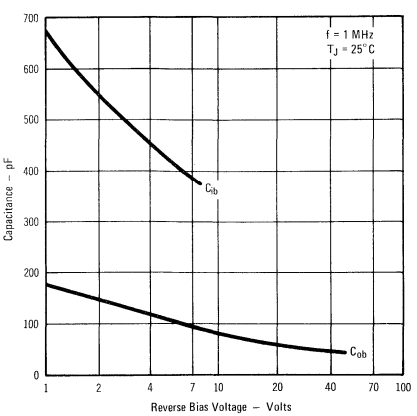


Figure 6
CAPACITANCE versus VOLTAGE

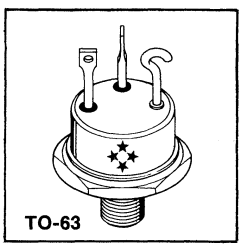
General Semiconductor Industries, Inc.

2N4002
2N4003

NPN SILICON POWER TRANSISTORS

DIFFUSED SILICON EPITAXIAL PASSIVATED TRANSISTORS

These NPN devices are designed for use in high power switching and untuned amplifier applications. The latest technologies are used to offer the highest degree of reliability.



FEATURES

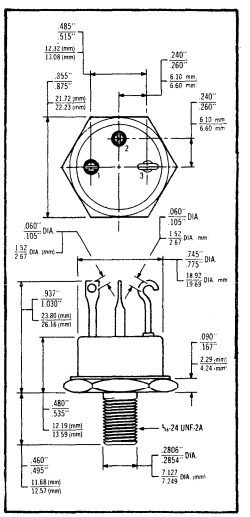
- **Fast Switching**
- **High Power Dissipation**
- **Low Leakage Current**
- **Low Saturation Voltage**

APPLICATIONS

- **Switching Regulators**
- **Inverters**
- **Converters**
- **Power Amplifiers**

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Storage Temperature		−65°C to +200°C	
Operating Junction Temperature		+200°C	
Lead Temperature (1/16 inch from case for 10 seconds)		+230°C	
Maximum Power Dissipation			
Total Dissipation at 100°C Case Temperature		100 Watts	
Linear Derating Factor		1.0 W/°C	
Maximum Voltages and Current		**2N4002**	**2N4003**
V_{CEO}	Collector to Emitter Voltage	80 Volts	100 Volts
V_{CBO}	Collector to Base Voltage	100 Volts	120 Volts
V_{EBO}	Emitter to Base Voltage	8 Volts	8 Volts
I_C	Continuous Collector Current	30 Amps	30 Amps



MECHANICAL CHARACTERISTICS

Case: TO-63 Package
Weight: 24 grams (Approximate)
1. Emitter 2. Base 3. Collector
Body marked with Logo and type number

*ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N4002 MIN	2N4002 MAX	2N4003 MIN	2N4003 MAX	UNITS
†Collector to Emitter Breakdown Voltage	BV_{CEO}	I_C = 30mA, I_B = 0	80		100		Volts
Collector Cutoff Current	I_{CEO}	V_{CE} = 40V, I_B = 0		2			mAmps
		V_{CE} = 50V, I_B = 0				2	mAmps
Emitter Cutoff Current	I_{EBO}	V_{EB} = 5V, I_C = 0		100		100	μAmps
		V_{EB} = 8V, I_C = 0		50		50	mAmps
†DC Current Gain	h_{FE}	V_{CE} = 4V, I_C = 30A	10		10		
		V_{CE} = 4V, I_C = 15A	20	80	20	80	
† Collector Saturation Voltage	$V_{CE(sat)}$	I_B = 4A, I_C = 30A		1.2		1.2	Volts
† Base-Emitter Voltage	$V_{BE(on)}$	V_{CE} = 4V, I_C = 30A		1.8		1.8	Volts

*JEDEC registered data. † Pulse Conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

*DYNAMIC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Turn-on Time	t_{on}	See Figure 2		1.0	μ sec
Turn-off Time	t_{off}	See Figure 2		3.0	μ sec
High Frequency Small Signal Common Emitter Small Signal	$\lvert h_{fe} \rvert$	V_{CE} = 10V, I_C = 1A, f = 10 MHz	3		
	h_{fe}	V_{CE} = 4V, I_C = 1A, f = 1 KHz	30		

*JEDEC registered data.

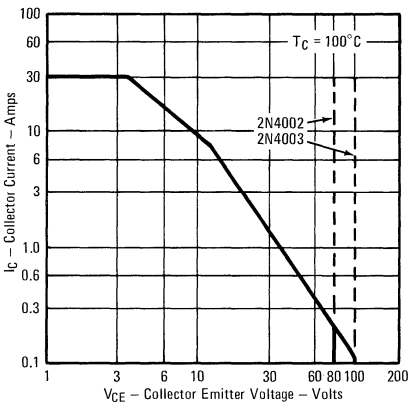


Figure 1 – MAXIMUM SAFE OPERATING REGION

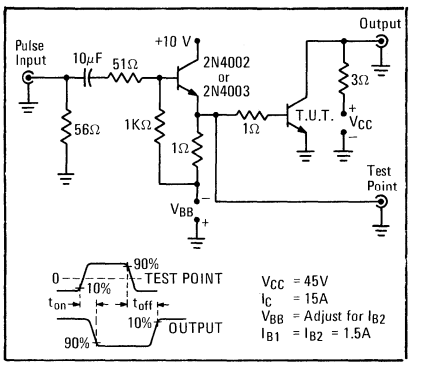


Figure 2 – SWITCHING CIRCUIT

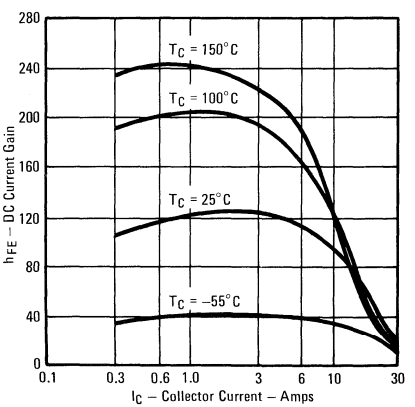


Figure 3 – TYPICAL DC CURRENT GAIN

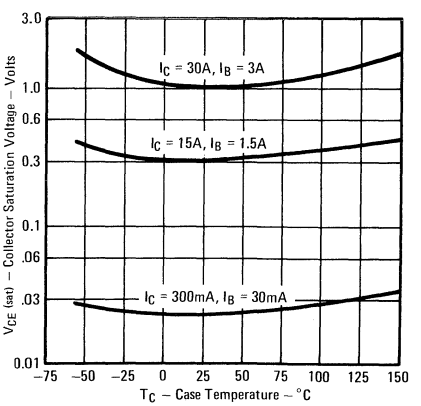


Figure 4 – SATURATION VOLTAGE VS. TEMPERATURE

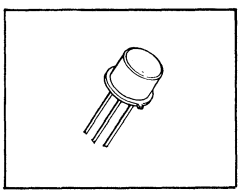
General Semiconductor Industries, Inc.

2N4150

NPN SILICON HIGH POWER TRANSISTORS

DIFFUSED SILICON PLANAR PASSIVATED TRANSISTORS

These devices are designed for use in high current switching applications. The latest technologies are used to offer the highest degree of reliability. JAN/JAN TX 2N4150 transistors to MIL-S-19500/394 are also available.

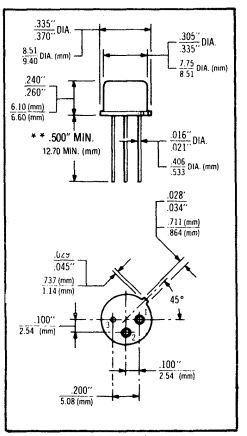


FEATURES

- **Low Saturation Voltage**
- **Fast Switching**
- **Collector Current: 10 Amps Peak**
- **Low Leakage Current**
- **Low Drive Requirement**

APPLICATIONS

- **High Speed Switching Regulated Power Supplies**
- **Converters**
- **Inverters**
- **Wide Band Amplifiers**



**Also available in 1.5" lead length.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	—65°C to 200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 60 second time limit)	+300°C
Maximum Power Dissipation	
Total Dissipation at 100°C Case Temperature (1) See Safe Operating Curves for derating	5 Watts
Linear derating factor	50 mW/°C

Maximum Voltages and Current	2N4150	JAN 2N4150
V_{CEO} Collector to Emitter Voltage	80 Volts	70 Volts
V_{CBO} Collector to Base Voltage	100 Volts	100 Volts
V_{EBO} Emitter to Base Voltage	5 Volts	7 Volts
I_C Continuous Collector Current	10 Amps	10 Amps

MECHANICAL CHARACTERISTICS

Case: TO-5 Package
Weight: 1.8 grams (maximum)
Leads: Gold Plated Kovar
1. Emitter 2. Base 3. Collector
Body marked with Logo ⁘ and type number

*ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N4150 MIN	2N4150 MAX	JAN2N4150 MIN	JAN2N4150 MAX	UNITS
Collector Cutoff Current	I_{CEO}	V_{CE}=60V, I_B = 0		10		10	μAmp
Collector Cutoff Current	I_{CEX}	V_{CE}=100V, V_{EB} = 0.5V		10		10	μAmp
Collector Cutoff Curent	I_{CBO}	V_{CB}=60V, V_{BE} = 0V		0.1		0.1	μAmp
Emitter Cutoff Current	I_{EBO}	V_{BE}=5V, V_{CE}= 0V		10		0.1	μAmp
†DC Current Gain	h_{FE}	I_C = 5A, V_{CE} = 5V	40	120	40	120	
	h_{FE}	I_C = 10A, V_{CE} = 5V	10		10		
	h_{FE}	I_C = 1A, V_{CE} = 5V	50		50		
Collector to Base Breakdown Voltage	BV_{CBO}	I_C = 10μA, I_E= 0	100		100		Volts
Collector to Emitter Breakdown Voltage	BV_{CEO}	I_C = 0.1A, I_B= 0	70		70		Volts
Emitter to Base Breakdown Voltage	BV_{EBO}	I_E = 10μA, I_C= 0	7		7		Volts
†Collector Saturation Voltage	$V_{CE(sat)}$	I_C = 5A, I_B = 0.5A		0.6		0.6	Volts
		I_C = 10A, I_B = 1A		2.5		2.5	Volts
†Base Saturation Voltage	$V_{BE(sat)}$	I_C = 5A, I_B = 0.5A		1.5		1.5	Volts
		I_C = 10A, I_B = 1A		2.5		2.5	Volts

*JEDEC registered data. † Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

General Semiconductor Industries, Inc. • 2001 W. Tenth Place, Tempe, AZ 85281 • (602)968-3101 • FAX: (602)966-6396

DYNAMIC CHARACTERISTICS*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N4150 MIN	2N4150 MAX	JAN 2N4150 MIN	JAN 2N4150 MAX	UNITS
Pulse Delay Time	t_d	See Circuit #1		–		50	nSec
Pulse Rise Time	t_r	See Circuit #1		200		500	nSec
Pulse Storage Time	t_s	See Circuit #1		2.0		1.5	μSec
Pulse Fall Time	t_f	See Circuit #1		200		500	nSec
Collector Base Capacitance	C_{obo}	V_{CB} = 10V, I_E = 0, f = 1 MHz		350		350	pF
High Frequency Small Signal	$\|h_{fe}\|$	I_C = 200mA, V_{CE} = 10V, f = 10MHz	1.5		1.5	7.5	

*JEDEC registered data.

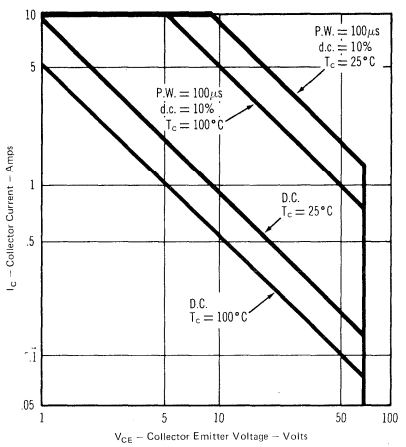


Figure 1—Maximum Safe Operation Region

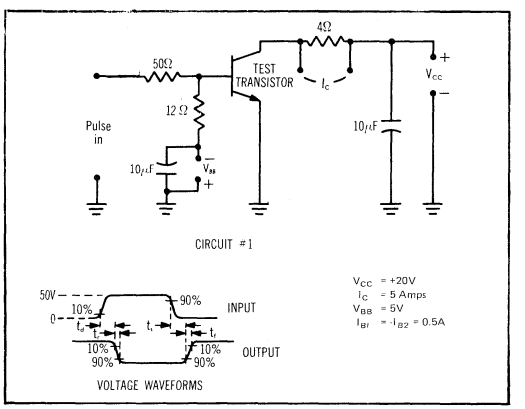


Figure 2—Pulse Response Measurement Circuit

TYPICAL CHARACTERISTICS

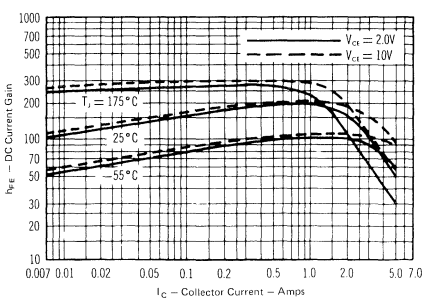


Figure 3—Static Forward Current Transfer Ratio

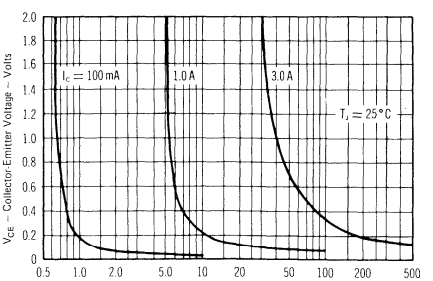


Figure 4—Collector Saturation Region

General Semiconductor Industries, Inc.

2N4863
2N4864

SILICON NPN TRANSISTORS

These double diffused, epitaxial collector devices are oxide passivated. They are designed for use in switching and many amplifier applications. The latest technologies are used to provide optimum performance and the highest degree of reliability.

NPN
120V
2.0 AMP SWITCHING

2N4863, Case TO-5; 2N4864, Case TO-66.

TO-5 & TO-66

***MAXIMUM RATINGS** (T_C = 25° C unless otherwise noted)

RATING	SYMBOL		2N4863	2N4864	UNIT
Collector-Base Voltage	V_{CBO}		140	140	Volts
Collector—Emitter Voltage	V_{CEO}		120	120	Volts
Emitter-Base Voltage	V_{EBO}		8.0	8.0	Volts
Collector Current—Continuous	I_C		2.0	2.0	Amps
Base Current—Continuous	I_B		0.5	0.5	Amps
Total Power Dissipation @ T_C = 100° C	P_D		4.0	16	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$		25	6.25	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}		-65 to +200	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25° C unless otherwise noted)

SYMBOL	CONDITIONS	2N4863 Min	2N4863 Max	2N4864 Min	2N4864 Max	Unit
$V_{CEO(sus)}$	I_C = 10mA	120	—	120	—	Volts
I_{CEX}	V_{CE} = 60V, V_{BE} = -0.5V, T_C = 150° C	—	10	—	10	μA
I_{CEX}	V_{CE} = 140V, V_{BE} = -0.5V	—	10	—	10	μA
I_{CBO}	V_{CB} = 60V	—	0.1	—	0.1	μA
I_{EBO}	V_{EB} = 8V	—	10	—	10	μA
I_{CEO}	V_{CE} = 60V	—	10	—	10	μA
h_{FE} †	V_{CE} = 5.0V, I_C = 2.0A	15	—	15	—	
h_{FE} †	V_{CE} = 5.0V, I_C = 0.5A	50	150	50	150	
$V_{CE(sat)}$ †	I_C = 2.0A, I_B = 0.2A	—	1.5	—	1.5	Volts
$V_{CE(sat)}$ †	I_C = 0.5A, I_B = 50mA	—	0.2	—	0.2	Volts
$V_{BE(on)}$ †	I_C = 0.5A, V_{CE} = 5.0V	—	1.2	—	1.2	Volts
$\|h_{FE}\|$	V_{CE} = 10V, I_C = 0.1A, f = 10MHz	5.0	—	5.0	—	
C_{ob}	V_{CB} = 10V, f = 1.0MHz	—	50	—	50	pF

* JEDEC registered data. † Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

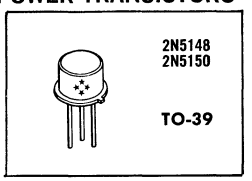
General Semiconductor Industries, Inc.

2N5148
2N5150

NPN SILICON HIGH POWER TRANSISTORS

DIFFUSED SILICON EPITAXIAL PASSIVATED TRANSISTOR

These devices are designed for use in power amplifiers and high speed switching applications. The latest technologies are used to offer the highest degree of reliability.



FEATURES

- Low Saturation Voltage
- Fast Switching
- Low Leakage Current
- Isolated Collector
  2N4998, 2N5000

APPLICATIONS

- High Frequency Inverters
- Converters
- Linear Amplifiers
- High Speed Switching Regulated Power Supplies
- RF Power Amplifiers

ABSOLUTE MAXIMUM RATINGS

		2N5148	2N5150
Collector to Emitter Voltage	V_{CEO}	80 Volts	
Collector to Base Voltage	V_{CBO}	100 Volts	
Emitter to Base Voltage	V_{EBO}	6 Volts	
Collector Current — Continuous	I_C	2 Amps	
— Peak	$I_{C\ (Peak)}$	5 Amps	
Base Current — Continuous	I_B	1 Amp	
Total Device Dissipation, @ $T_C = 50°C$	P_D	30 Watts	6 Watts
Linear Derating Factor		.2W/°C	.04W/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−65°C to +200°C	

MECHANICAL CHARACTERISTICS

Case: 2N5148, 2N5150 – TO-39
1. Emitter 2. Base 3. Collector
Body marked with Logo and type number

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	2N5148 MIN	2N5148 MAX	2N5150 MIN	2N5150 MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CEO}	†I_C = 100 mA, I_B = 0	80		80		Volts
Collector Cutoff Current	I_{CEO}	V_{CE} = 40V, I_B = 0		50		50	μAmp
	I_{CES}	V_{CE} = 60V, V_{BE} = 0V		1.0		1.0	μAmp
		V_{CE} = 100V, V_{BE} = 0V		1.0		1.0	mA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 5V, I_C = 0		1.0		1.0	μAmp
		V_{EB} = 6V, I_C = 0		1.0		1.0	mA
DC Current Gain	h_{FE}	†I_C = 50mA, V_{CE} = 5V	20		50		
		†I_C = 1A, V_{CE} = 5V	30	90	70	200	
		†I_C = 2A, V_{CE} = 5V	15		30		
		†I_C = 1A, V_{CE} = 5V @ T_C −55°C	15		35		
Collector Saturation Voltage	$V_{CE\ (sat)}$	†I_C = 1A, I_B = 0.1A		0.46		0.46	Volts
		†I_C = 3A, I_B = 0.6A		5.0		5.0	Volts
Base Emitter Saturation Voltage	$V_{BE\ (sat)}$	†I_C = 1A, I_B = 0.1A		1.2		1.2	Volts
		†I_C = 2A, I_B = 0.2A		1.5		1.5	Volts
Turn-on Time	t_{on}	See Figure 1		0.1		0.1	μsec.
Turn-off Time	t_{off}	See Figure 1		0.8		1.2	μsec.
Collector Base Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz		70		70	pF
High Frequency Current Gain	$\|h_{fe}\|$	V_{CE} = 5V, I_C = 0.2A, f = 20MHz	2.5		3		

*JEDEC registered data. † Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

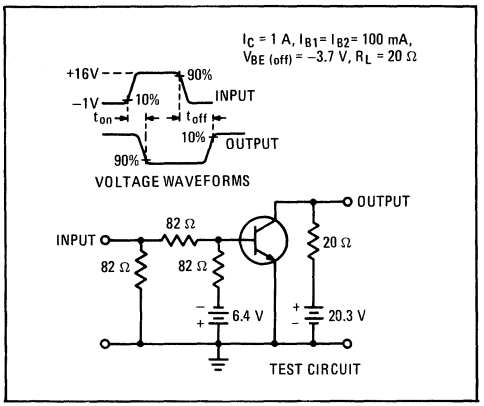


FIGURE 1 — Switching Circuit

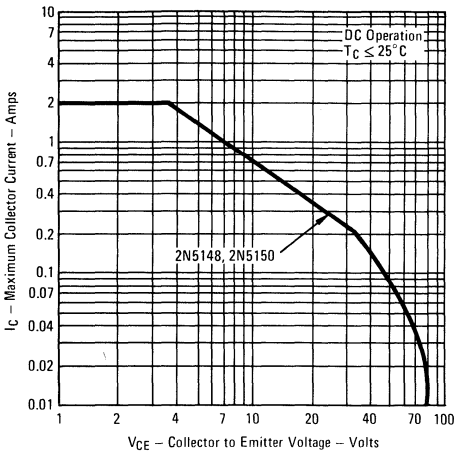


FIGURE 2 — Maximum Safe Operating Region

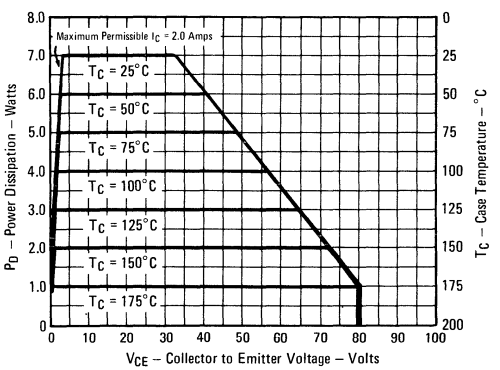


FIGURE 3 — Dissipation Derating Curve (2N5148, 2N5150)

TYPICAL CHARACTERISTICS

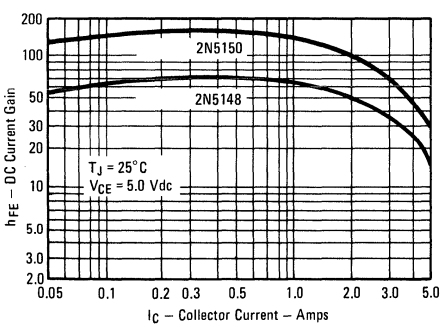


FIGURE 4 — DC Current Gain

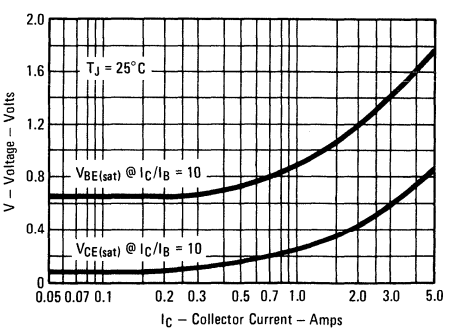


FIGURE 5 — "On" Voltages

General Semiconductor Industries, Inc.

2N6232

SILICON NPN TRANSISTORS

These double diffused, epitaxial collector devices are oxide passivated. They are designed for use in switching and many amplifier applications. The latest technologies are used to provide optimum performance and the highest degree of reliability.

NPN
100V
5.0 AMP SWITCHING

TO-5

3

NPN SWITCHING TRANSISTORS

***MAXIMUM RATINGS** (T_C = 25° C unless otherwise noted)

RATING	SYMBOL	2N6232	UNIT
Collector-Base Voltage	V_{CBO}	140	Volts
Collector—Emitter Voltage	V_{CEO}	100	Volts
Emitter-Base Voltage	V_{EBO}	7.0	Volts
Collector Current—Continuous	I_C	10	Amps
Base Current—Continuous	I_B	2.0	Amps
Total Power Dissipation @T_C = 100 °C	P_D	15	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	6.67	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25° C unless otherwise noted)

SYMBOL	CONDITIONS	2N6232 Min	2N6232 Max	Unit
V_{CBO}	I_C = 1.0mA	140	—	Volts
V_{CEO}	I_C = 100mA	100	—	Volts
V_{EBO}	I_E = 10μA	7.0	—	Volts
V_{CER}	I_C = 10mA, R_{BE} = 10Ω	140	—	Volts
I_{CBO}	V_{CB} = 140V	—	0.2	μA
I_{CES}	V_{CE} = 140V	—	0.2	μA
h_{FE}†	V_{CE} = 2.0V, I_C = 0.5A	40	250	
h_{FE}†	V_{CE} = 2.0V, I_C = 5.0A	25	100	
h_{FE}†	V_{CE} = 5.0V, I_C = 10A	20	—	
$V_{CE(sat)}$†	I_C = 5.0A, I_B = 0.5A	—	0.7	Volts
$V_{CE(sat)}$†	I_C = 10A, I_B = 1.0A	—	1.4	Volts
$V_{BE(sat)}$†	I_C = 5.0A, I_B = 0.5A	—	1.4	Volts
$V_{BE(sat)}$†	I_C = 10A, I_B = 1.0A	—	1.8	Volts
$\|h_{FE}\|$	V_{CE} = 10V, I_C = 0.2A, f = 10MHz	3.0	—	
C_{OB}	V_{CB} = 10V, f = 1.0MHz	—	150	pF
SWITCHING				
t_{on}	**Resistive Load**	—	0.25	μs
t_{off}	V_{CC} = 30V I_C = 5.0A I_{B1} = I_{B2} = 0.5A t_P = 10μs	—	1.2	μs

*JEDEC registered data. † Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

General Semiconductor Industries, Inc.

2N6274
2N6277

HIGH POWER NPN *Switch Plus* TRANSISTORS

These double diffused, epitaxial collector devices are oxide passivated. They are designed for use in switching and many amplifier applications. The latest technologies are used to provide optimum performance and the highest degree of reliability. The 2N6274 and 2N6277 are available as JAN, JANTX, and JANTXV supplied to Mil-S-19500/514.

- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Switching Regulators**

TO-204AE

NPN
UP TO
150V
V_{CEO}

50A
I_C (MAX)

20 A
SWITCHING

AVAILABLE AS
JAN
JANTX
JANTXV

Switch Plus

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION		2N6274	2N6277	UNIT
V_{CBO}	Collector-Base Voltage		120	180	Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining		100	150	Volts
V_{EBO}	Emitter-Base Voltage		6.0		Volts
I_C	Collector Current—Continuous		50		Amps
I_B	Base Current—Continuous		20		Amps
P_D	Total Power Dissipation T_C = 25°C		250		Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range		-65 to +200		°C

***ELECTRICAL CHARACTERISTICS** (Applies to all types unless otherwise noted.)

			2N6274		2N6277		
SYMBOL	CONDITIONS	NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
$V_{CEO(sus)}$	I_C = 50mA		100		150		Volts
I_{CEX}	V_{CE} = Rated V_{CB}, V_{EB} = 1.5V			10		10	μA
I_{CE}	V_{CE} = Rated V_{CB}, V_{EB} = 1.5V, T_C = 150°			1.0		1.0	μA
I_{EBO}	V_{EB} = 6.0V			100		100	μA
ON-STATE							
h_{FE}	I_C = 1.0A, V_{CE} = 4.0V	Pulsed: Notes 1 & 2.	50		50		
h_{FE}	I_C = 20A, V_{CE} = 4.0V		30	120	30	120	
h_{FE}	I_C = 50A, V_{CE} = 4.0V		10		10		
$V_{CE(sat)}$	I_C = 20A, I_B = 2.0A			1.0		1.0	Volts
$V_{CE(sat)}$	I_C = 50A, I_B = 10A			3.0		3.0	Volts
V_{BE}	I_C = 20A, V_{CE} = 4.0V			1.8		1.8	Volts
$V_{BE(sat)}$	I_C = 20A, I_B = 2.0A			1.8		1.8	Volts
$V_{BE(sat)}$	I_C = 50A, I_B = 10A			3.5		3.5	Volts
DYNAMIC							
t_r	**Resistive Load** V_{CC} = 80V, I_C = 20A I_{B1} = I_{B2} = 2.0A t_P = 50μs			0.35		0.35	μs
t_s				0.80		0.80	μs
t_f				0.25		0.25	μs
THERMAL			**MAXIMUM**				
$R_{\theta JC}$	V_{CE} = 10V, I_C = 5.0A		0.7		0.7		°C/W

Notes: 1) Measured using Kelvin connections.
2) Pulse measurement conditions: Length = 300μs. Duty Cycle ≤ 2%

*JEDEC registered data.

General Semiconductor Industries, Inc.

2N6338 THRU 2N6341 INCLUDING JAN, TX, TXV

HIGH POWER NPN SWITCHING TRANSISTORS

These transistors are designed for use in high performance, high speed switching systems. A double diffused, multiepitaxial process is utilized for these devices which results in a rugged transistor with superior switching speed.

The 2N6338 and 2N6341 are available as JAN, JANTX and JANTXV, supplied to MIL-S-19500/509.

NPN
100, 150V
10 AMP SWITCHING

TO-204AA (TO-3)

MAXIMUM RATINGS* Data applies to all JEDEC & JAN Types, $T_C = 25°C$, unless otherwise noted.

RATING	SYMBOL	2N6338	2N6339	2N6340	2N6341	UNIT
Collector-Base Voltage	V_{CBO}	120	140	160	180	Volts
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Volts
Emitter-Base Voltage	V_{EBO}	6				Volts
Collector Current-Continuous Peak	I_C I_{CM}	25 50				Amps Amps
Base Current-Continuous	I_B	10				Amps
Total Power Dissipation @ $T_C = 25°C$ $T_C = 100°C$	P_D P_D	200 112 (1)				Watts Watts
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200				°C

ELECTRICAL CHARACTERISTICS* — Data applies to all JEDEC & JAN Types, $T_C = 25°C$, unless otherwise noted.

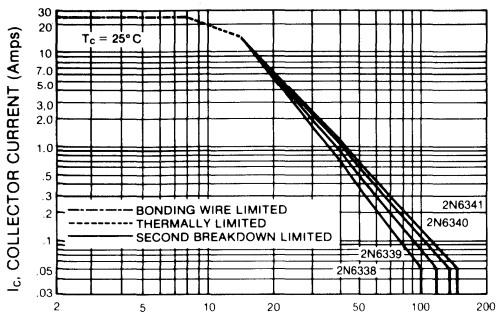
SYMBOL	CONDITIONS	PART NO.	Min	Max	Unit
$V_{CEO(sus)}$	$I_C = 50mA$ (3)	**2N6338**	100		Volts
		2N6339	120		Volts
		2N6340	140		Volts
		2N6341	150		Volts
I_{CEO}	V_{CE} = 1/2 Rated V_{CEO} (1)			50	μA
I_{CEX}	V_{CE} = Rated V_{CEO}, $V_{EB} = 1.5V$			10	μA
	V_{CE} = Rated V_{CEO}, $V_{EB} = 1.5V$, $T_C = 150°C$ (1)			1.0	mA
I_{CBO}	V_{CE} = Rated V_{CBO}			10	μA
I_{EBO}	$V_{EB} = 6V$			100	μA
h_{FE}	$V_{CE} = 2.0V$, $I_C = 0.5A$ (3)		50		
	$I_C = 10A$ (3)		30	120	
	$I_C = 10A$ (3), $T_C = -65°C$ (1)		10		
	$I_C = 25A$ (3)		12		
$V_{CE(sat)}$	$I_C = 10A$, $I_B = 1.0A$ (3)			1.0	Volts
	$I_C = 25A$, $I_B = 2.5A$ (3)			1.8	Volts
$V_{BE(sat)}$	$I_C = 10A$, $I_B = 1.0A$ (3)			1.8	Volts
	$I_C = 25A$, $I_B = 2.5A$ (2) (3)			2.5	Volts
f_t	$V_{CE} = 10V$, $I_C = 1A$, $f = 10MHz$		4.0		MHz
C_{obo}	$V_{CB} = 10V$, $0.1 \leq f \leq 1.0MHz$	JEDEC Only		300	pF
		JAN Types Only		450	
t_{on}	**Resistive Switching** $V_{CC} = 80V$, $I_C = 10A$ $I_{B1} = I_{B2} = 1.0A$	JAN Types Only		0.5	μs
t_r		JEDEC Only		0.3	μs
t_s				1.0	μs
t_f		JEDEC Only		0.25	μs
t_{off}		JAN Types Only		1.25	μs

THERMAL CHARACTERISTICS	SYMBOL		UNIT
Thermal Resistance	$R_{\theta JC}$	0.875	°C/W

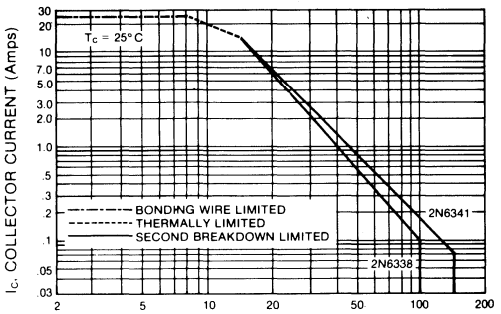
*JEDEC Registered Data, (1) Part of military specification only, (2) Part of JEDEC specification only, (3) Pulse Test: 300μs, Duty Cycle · 2%

SAFE OPERATING AREAS

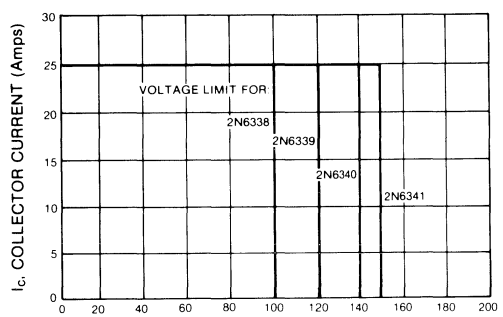
JEDEC REGISTERED dc ACTIVE REGION



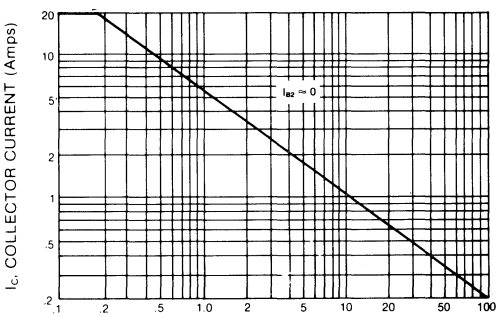
JAN SPECIFIED dc ACTIVE REGION



SWITCHING, CLAMPED OR SNUBBED INDUCTIVE LOAD

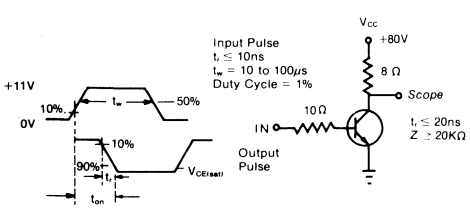


UNCLAMPED INDUCTIVED LOAD (JAN PARTS ONLY)

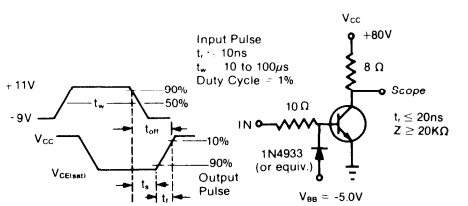


SWITCHING TIME TEST CIRCUITS

TURN-ON TIME

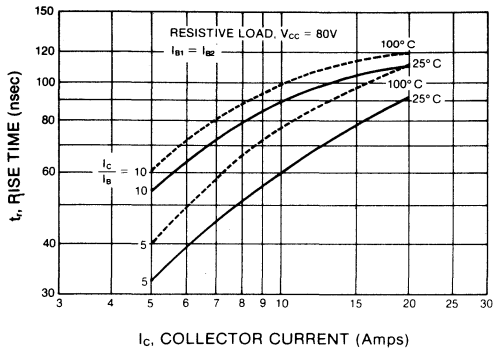


TURN-OFF TIME



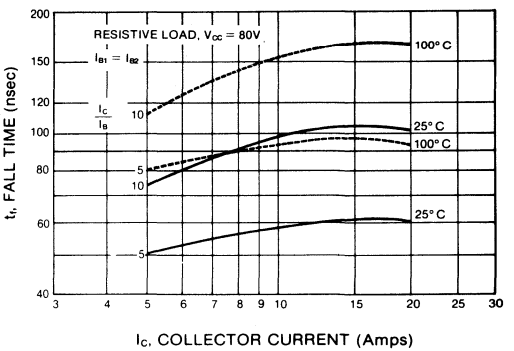
TYPICAL SWITCHING CHARACTERISTICS

RISE TIME



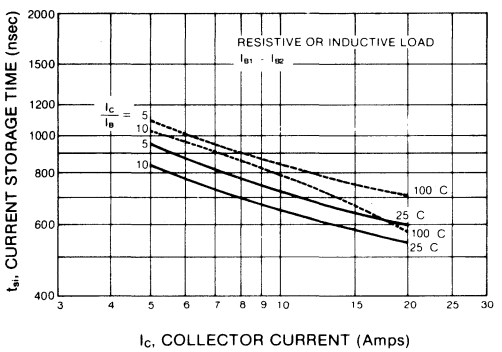
I_C, COLLECTOR CURRENT (Amps)

FALL TIME



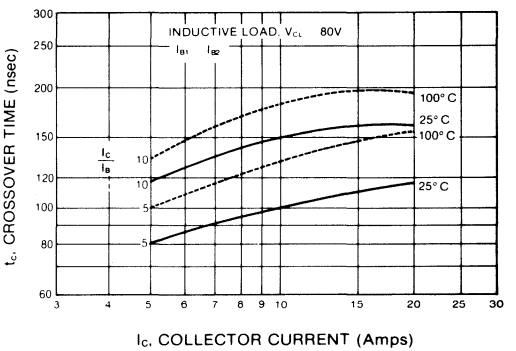
I_C, COLLECTOR CURRENT (Amps)

STORAGE TIME



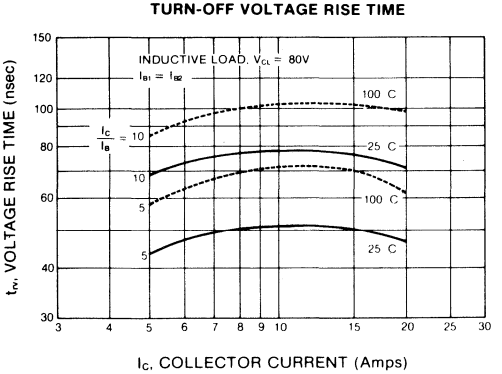
I_C, COLLECTOR CURRENT (Amps)

CROSSOVER TIME



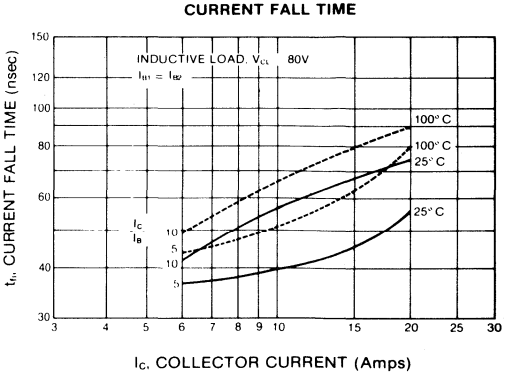
I_C, COLLECTOR CURRENT (Amps)

TURN-OFF VOLTAGE RISE TIME



I_C, COLLECTOR CURRENT (Amps)

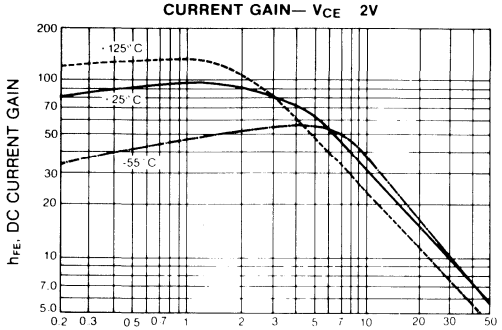
CURRENT FALL TIME



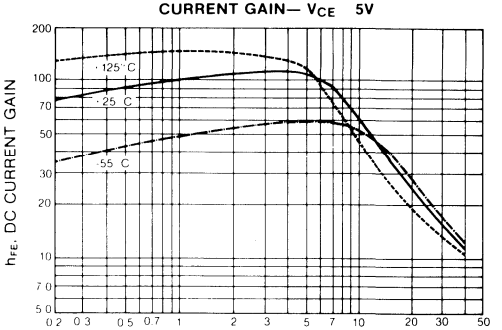
I_C, COLLECTOR CURRENT (Amps)

TYPICAL dc CHARACTERISTICS

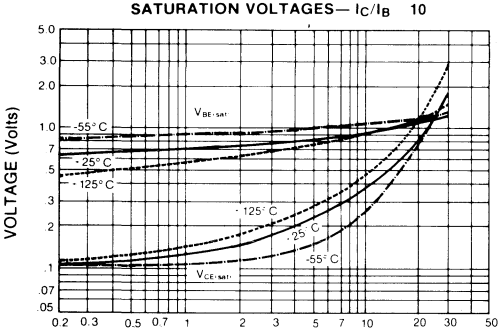
CURRENT GAIN— V_{CE} 2V



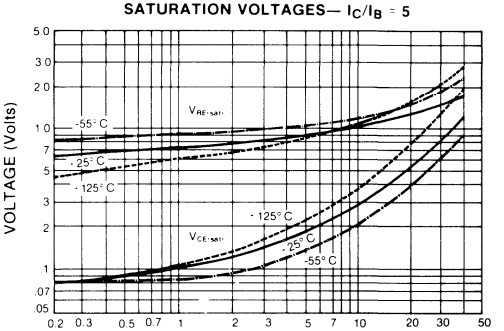
CURRENT GAIN— V_{CE} 5V



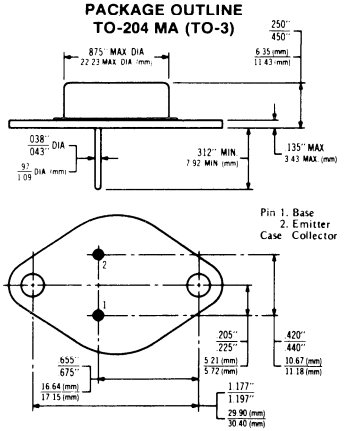
SATURATION VOLTAGES— I_C/I_B 10



SATURATION VOLTAGES— I_C/I_B = 5



PACKAGE OUTLINE
TO-204 MA (TO-3)



General Semiconductor Industries, Inc.

2N6579
2N6580
2N6581

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The 2N6581 series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

NPN
350, 400, 450V
10 AMP SWITCHING
t_f — 250ns TYPICAL

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted)

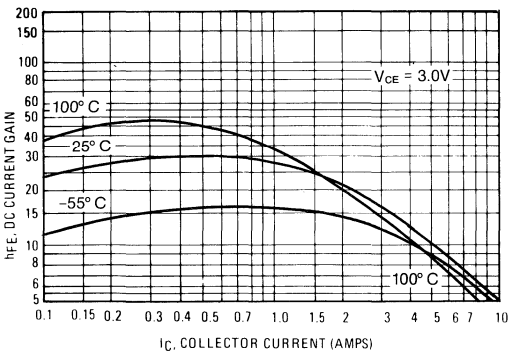
RATING	SYMBOL	2N6579	2N6580	2N6581	UNIT
Collector-Base Voltage	V_{CBO}	450	500	550	Volts
Collector-Emitter Voltage	V_{CEO}	350	400	450	Volts
Emitter-Base Voltage	V_{EBO}	9.0	9.0	9.0	Volts
Collector Current—Continuous Peak	I_C I_{CM}	10 16	10 16	10 16	Amps Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Total Power Dissipation @ T_C = 25° C	P_D	125	125	125	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	1.4	1.4	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

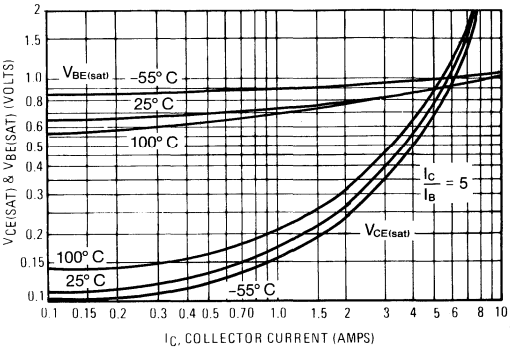
SYMBOL	CONDITIONS	2N6579 Min	2N6579 Max	2N6580 Min	2N6580 Max	2N6581 Min	2N6581 Max	Unit
$V_{CEO(sus)}$	I_C = 200mA	350	—	400	—	450	—	Volts
I_{CEV}	V_{CB} = rated V_{CBO}, V_{EB} = 1.5V	—	500	—	500	—	500	μA
I_{CEV} 100° C	V_{CB} = rated V_{CBO}, V_{EB} = 1.5V	—	2.0	—	2.0	—	2.0	mA
I_{EBO}	V_{EB} = 9.0V	—	100	—	100	—	100	μA
h_{FE}†	V_{CE} = 3.0V, I_C= 5.0A	7.0	35	7.0	35	7.0	35	—
$V_{CE(sat)}$†	I_C = 5.0A, I_B = 1.0A	—	1.5	—	1.5	—	1.5	Volts
$V_{CE(sat)}$†	I_C = 10A, I_B = 5.0A	—	3.0	—	3.0	—	3.0	Volts
$V_{BE(sat)}$†	I_C = 5.0A, I_B = 1.0A	—	1.5	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	12.5	50	12.5	50	12.5	50	MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz	75	250	75	250	75	250	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d**	**Resistive Load** V_{CC} = 150V I_C = 5.0A, R = 30Ω I_{B1} = I_{B2} = 1.0A t_p = 100 μsec	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r**		0.20	0.50	0.20	0.50	0.20	0.50	μs
t_s		1.70	2.00	1.70	2.00	1.70	2.00	μs
t_f		0.25	0.50	0.25	0.50	0.25	0.50	μs
t_s	**Inductive Load** V_{CLAMP} = 250V I_C = 5.0A, L = 100 μH I_{B1} = I_{B2} = 1.0A t_p = 50 μsec	1.70	2.00	1.70	2.00	1.70	2.00	μs
t_{rv}		0.22	0.30	0.22	0.30	0.22	0.30	μs
t_{fi}		0.15	0.25	0.15	0.25	0.15	0.25	μs
t_c		0.35	0.50	0.35	0.50	0.35	0.50	μs
t_s 100° C		2.50	3.00	2.50	3.00	2.50	3.00	μs
t_{rv} 100° C		0.30	0.50	0.30	0.50	0.30	0.50	μs
t_{fi} 100° C		0.20	0.30	0.20	0.30	0.20	0.30	μs
t_c 100° C		0.60	1.00	0.60	1.00	0.60	1.00	μs

*JEDEC registered data. † Pulse Conditions: Width = 10μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

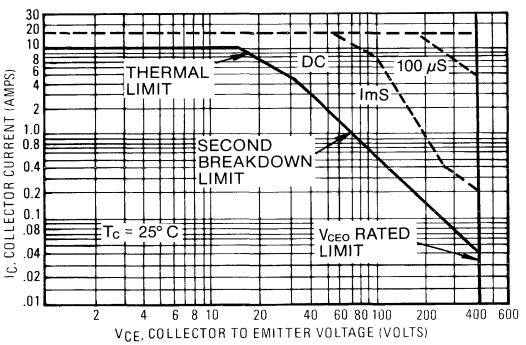
TYPICAL DC CURRENT GAIN



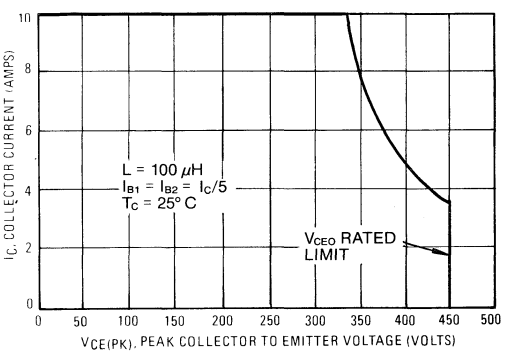
TYPICAL SATURATION VOLTAGE



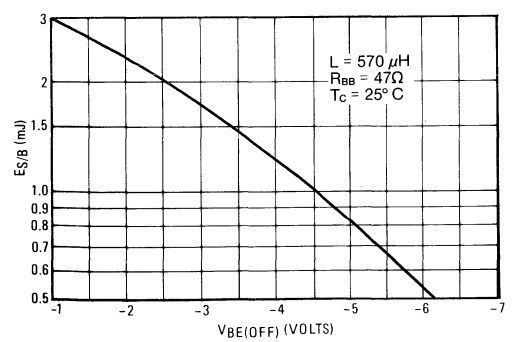
FORWARD BIASED SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA

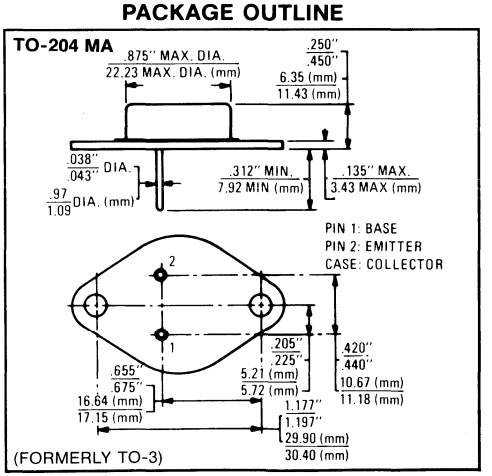


AVALANCHE ENERGY



PACKAGE OUTLINE

TO-204 MA



General Semiconductor Industries, Inc.

2N6582
2N6583
2N6584

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The 2N6584 series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

NPN
350, 400, 450V
10 AMP SWITCHING
t_f — 300ns TYPICAL

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted)

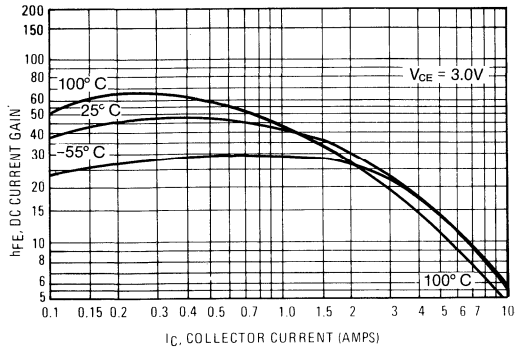
RATING	SYMBOL	2N6582	2N6583	2N6584	UNIT
Collector-Base Voltage	V_{CBO}	450	500	550	Volts
Collector-Emitter Voltage	V_{CEO}	350	400	450	Volts
Emitter-Base Voltage	V_{EBO}	9.0	9.0	9.0	Volts
Collector Current—Continuous Peak	I_C I_{CM}	10 16	10 16	10 16	Amps Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Total Power Dissipation @ T_C = 25° C	P_D	125	125	125	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	1.4	1.4	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

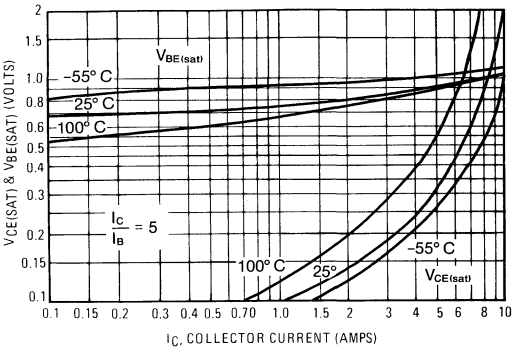
SYMBOL	CONDITIONS	2N6582 Min	2N6582 Max	2N6583 Min	2N6583 Max	2N6584 Min	2N6584 Max	Unit
V_{CBO}	I_C = 0.5mA	450	—	500	—	550	—	Volts
$V_{CEO(sus)}$	I_C = 200mA	350	—	400	—	450	—	Volts
I_{CEV}	V_{CB} = rated V_{CBO}, V_{EB} = 1.5V	—	500	—	500	—	500	μA
I_{CEV} 100° C	V_{CB} = rated V_{CBO}, V_{EB} = 1.5V	—	2.0	—	2.0	—	2.0	mA
I_{EBO}	V_{EB} = 9.0V	—	100	—	100	—	100	μA
h_{FE}†	V_{CE} = 3.0V, I_C= 7.0A	7.0	35	7.0	35	7.0	35	—
$V_{CE(sat)}$†	I_C = 7.0A, I_B = 1.4A	—	1.5	—	1.5	—	1.5	Volts
$V_{CE(sat)}$†	I_C = 10A, I_B = 5.0A	—	3.0	—	3.0	—	3.0	Volts
$V_{BE(sat)}$†	I_C = 7.0A, I_B = 1.4A	—	1.5	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	12.5	50	12.5	50	12.5	50	MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz	75	250	75	250	75	250	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load** V_{CC} = 150V I_C = 7.0A, R = 21Ω I_{B1} = I_{B2} = 1.4A t_p = 100 μsec	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r		0.35	0.50	0.35	0.50	0.35	0.50	μs
t_s		1.25	2.00	1.25	2.00	1.25	2.00	μs
t_f		0.30	0.50	0.30	0.50	0.30	0.50	μs
t_s	**Inductive Load** V_{CLAMP} = 250V I_C = 7.0A, L = 100 μH I_{B1} = I_{B2} = 1.4A t_p = 50 μsec	1.50	2.00	1.50	2.00	1.50	2.00	μs
t_{rv}		0.20	0.30	0.20	0.30	0.20	0.30	μs
t_{fi}		0.15	0.25	0.15	0.25	0.15	0.25	μs
t_c		0.30	0.50	0.30	0.50	0.30	0.50	μs
t_s 100° C		2.50	3.00	2.50	3.00	2.50	3.00	μs
t_{rv} 100° C		0.40	0.60	0.40	0.60	0.40	0.60	μs
t_{fi} 100° C		0.15	0.30	0.15	0.30	0.15	0.30	μs
t_c 100° C		0.65	1.00	0.65	1.00	0.65	1.00	μs

*JEDEC registered data. † Pulse Conditions: Width = 10μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

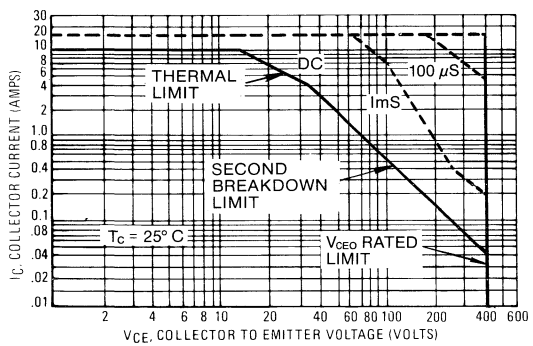
TYPICAL DC CURRENT GAIN



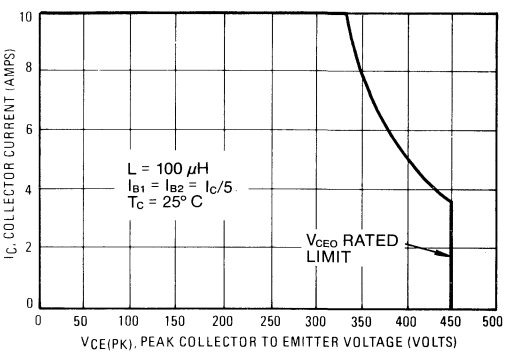
TYPICAL SATURATION VOLTAGE



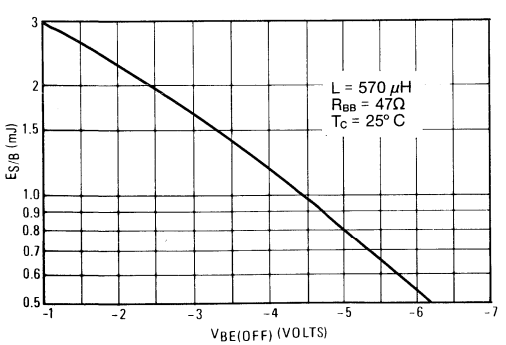
FORWARD BIASED SAFE OPERATING AREA



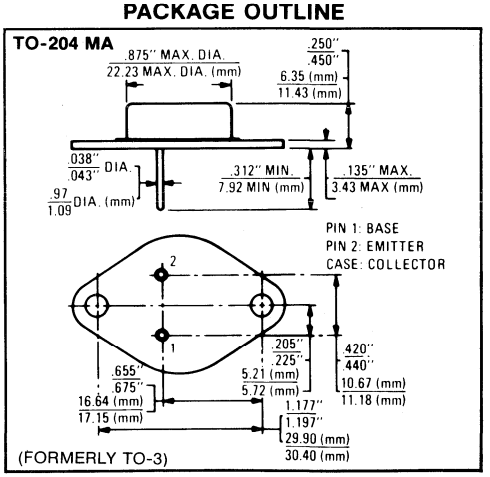
TURN-OFF SAFE OPERATING AREA



AVALANCHE ENERGY



PACKAGE OUTLINE



General Semiconductor Industries, Inc.

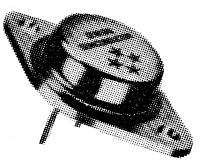
15 Amp NPN
300, 350, 400V
2N6653, 54, 55
XGSR15030, 35, 40
XGSR15030-I, 35-I, 40-I

C²R® HIGH SPEED/HIGH POWER SWITCHING TRANSISTORS

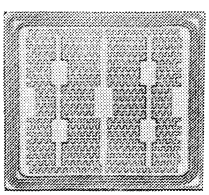
The XGSR series is an NPN double diffused epitaxial transistor designed for high speed switching systems. This unique series utilizes General Semiconductor Industries' C²R technology that provides surface stabilization for high voltage operation and enhances long term reliability. Another design feature is the use of an interdigitated emitter providing a periphery greater than 7.0 inches (18 cm) which improves both the gain characteristics and current handling capability.

These transistors have been specifically designed and engineered for high speed/high voltage switching applications where the designer is concerned with optimizing power conversion efficiency.

The XGSR series is also available in Isolated collector versions for reduction of conducted and radiated EMI.



TO-3



C²R®

FEATURES:
- **High Voltage**
- **High Gain**
- **High Current**
- **Low Saturation Voltages**
- **Fast Switching**
- **Low Leakage Current**
- **Isolated Collector Package Available**

APPLICATIONS:
- **High Speed Switching**
- **Power Conversion**
- **Converters**
- **Inverters**
- **Class D Amplifiers**
- **Class C Amplifiers**

*** MAXIMUM RATINGS** (T_C = 25° C unless otherwise noted)

RATING	SYMBOL	2N6653 XGSR15030 XGSR15030-I	2N6654 XGSR15035 XGSR15035-I	2N6655 XGSR15040 XGSR15040-I	UNIT
Collector-Base Voltage	V_{CBO}	350	400	450	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	7.0	7.0	7.0	Volts
Collector Current—Continuous —Peak	I_C I_{CM}	20 30	20 30	20 30	Amps Amps
Base Current—Continuous	I_B	10	10	10	Amps
Emitter Current—Continuous —Peak	I_E I_{EM}	30 40	30 40	30 40	Amps Amps
Total Power Dissipation at T_C = 100° C	P_D	75	75	75	Watts
Total Power Dissipation at T_C = 25° C	P_D	150	150	150	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.0	1.0	1.0	° C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +175 -65 to +200	-65 to +175 -65 to +200	-65 to +175 -65 to +200	° C ° C

*JEDEC Registered Data (2N6653, 54, 55).

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

		2N6653 XGSR15030 XGSR15030-I		2N6654 XGSR15035 XGSR15035-I		2N6655 XGSR15040 XGST15040-I		
SYMBOL	CONDITIONS	Min	Max	Min	Max	Min	Max	UNITS
V_{CBO}	I_C = 1.0mA	350	—	400	—	450	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1.0mA	7.0	—	7.0	—	7.0	—	Volts
$V_{CEX(SUS)}$	I_C = 50mA, V_{BE} = 1.5V	350	—	400	—	450	—	Volts
$V_{CER(SUS)}$	I_C = 50mA, R = 47Ω	325	—	375	—	425	—	Volts
I_{CBO} (1)	V_{CB} = 80% V_{CB} Rated	—	500	—	500	—	500	μA
(2)	V_{CB} = 100% V_{CB} Rated, V_{BE} = -1.5V	—	100	—	100	—	100	μA
I_{EBO} (1)	V_{EB} = 5.0V	—	100	—	100	—	100	μA
I_{EBO}	V_{EB} = 7.0V	—	50	—	50	—	50	μA
I_{CEO}	V_{CE} = 80% V_{CE} Rated	—	1.0	—	1.0	—	1.0	mA
I_{CEX}	V_{CE} = V_{CEO} Rated, V_{BE} = -1.5V, T_J = 150°	—	3.0	—	3.0	—	3.0	mA
h_{fe} (1)	V_{CE} = 5.0V, I_C = 15A†	10	—	10	—	10	—	
h_{FE} (2)	V_{CE} = 2.0V, I_C = 15A	10	—	10	—	10	—	
$V_{CE(sat)}$	I_C = 15A, I_B = 3.0A †	—	0.6	—	0.6	—	0.6	Volts
$V_{BE(sat)}$	I_C = 15A, I_B = 3.0A†	—	1.3	—	1.3	—	1.3	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, 10MHz	25	75	25	75	25	75	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	100	300	100	300	100	300	pF
t_d	V_{CC} = 200V, I_C = 15A, I_{B1} = I_{B2} = 3.0A, t_p = 10μs, Duty Cycle <2%, Resistive	—	0.05	—	0.05	—	0.05	μsec
t_r		—	0.2	—	0.2	—	0.2	μsec
t_s		—	1.5	—	1.5	—	1.5	μsec
t_f		—	0.35	—	0.35	—	0.35	μsec

*JEDEC Registered Data (2N6653, 54, 55).

†Pulse measurement conditions: Length = 300μsec, Duty Cycle <2% (measured using separate current carrying and voltage sensing leads).

(1) Test conditions and limits for XGSR15030, 14035, 15040

(2) Test conditions and limits for 2N6653, 6654, 6655

DC CHARACTERISTICS

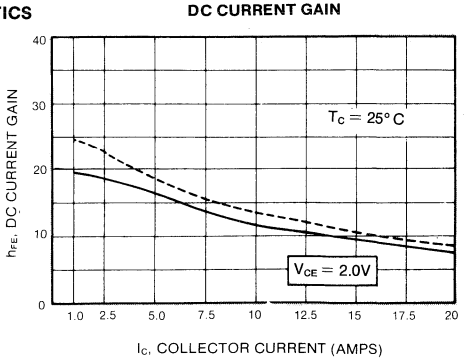
MEDIAN

90th PERCENTILE

MEDIAN: 50% of the test sample will exceed this value and 50% will be less than this value.

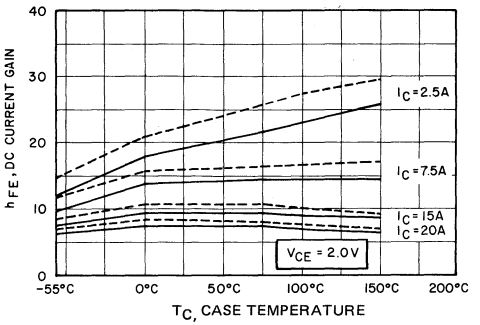
90th PERCENTILE: As used in this document, 90% of the test sample will have values "better than" the specified value.

DC CURRENT GAIN

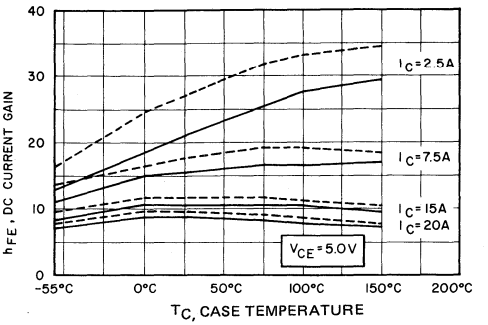


DC CHARACTERISTICS

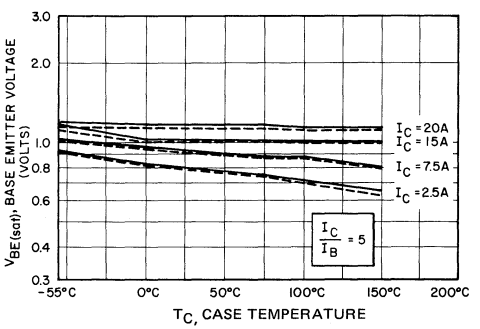
DC CURRENT GAIN



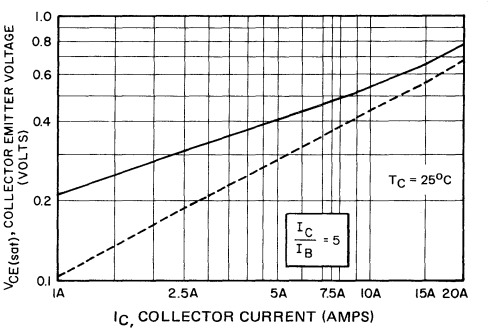
DC CURRENT GAIN



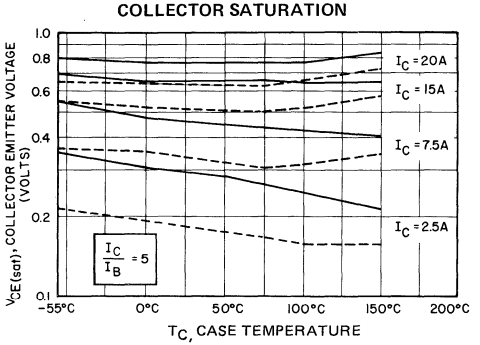
BASE EMITTER SATURATION



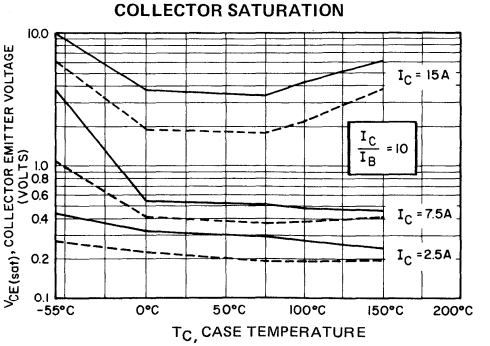
COLLECTOR SATURATION



COLLECTOR SATURATION

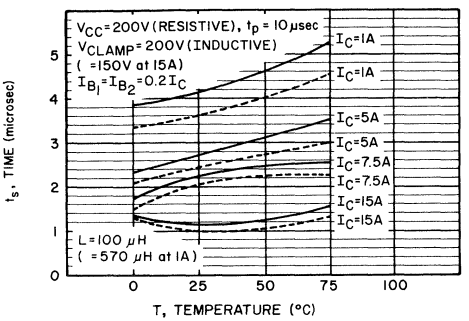


COLLECTOR SATURATION

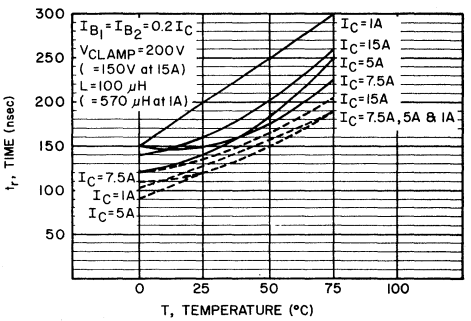


SWITCHING CHARACTERISTICS

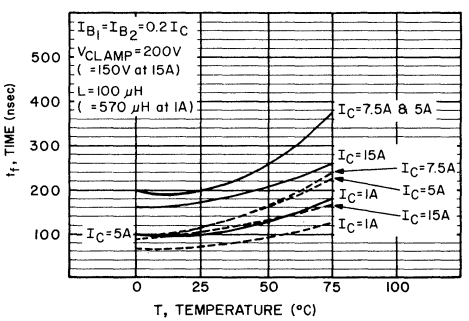
t_s, STORAGE TIME
(RESISTIVE & INDUCTIVE)



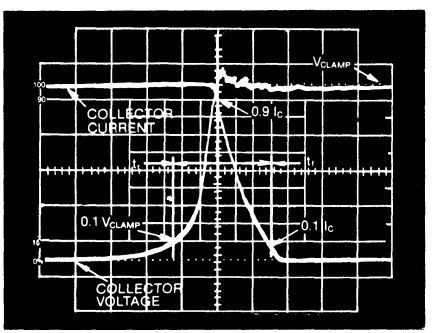
t_r, VOLTAGE RISE TIME
(TURN-OFF, INDUCTIVE)



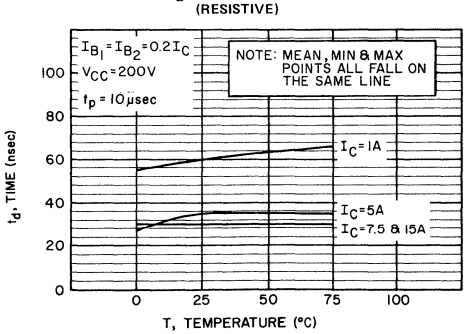
t_f, CURRENT FALL TIME
(TURN-OFF, INDUCTIVE)



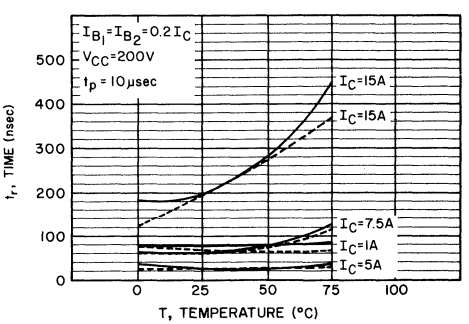
INDUCTIVE SWITCHING TURN-OFF WAVEFORM



t_d, DELAY TIME
(RESISTIVE)

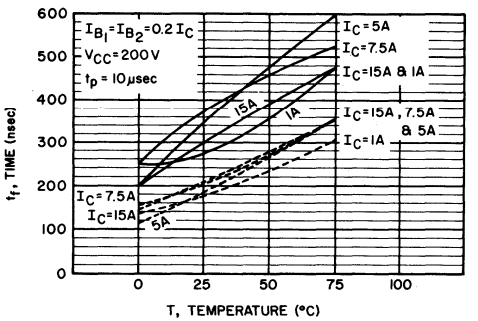


t_r, RISE TIME
(RESISTIVE)

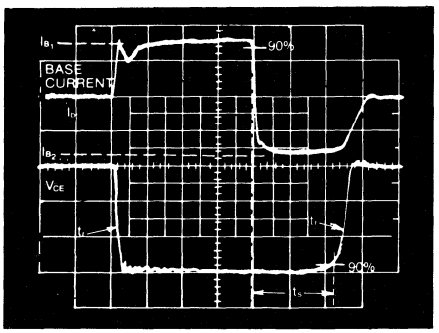


SWITCHING CHARACTERISTICS

t_f, CURRENT FALL TIME (RESISTIVE)

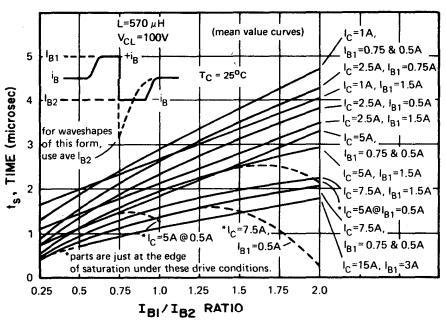


RESISTIVE SWITCHING WAVEFORM

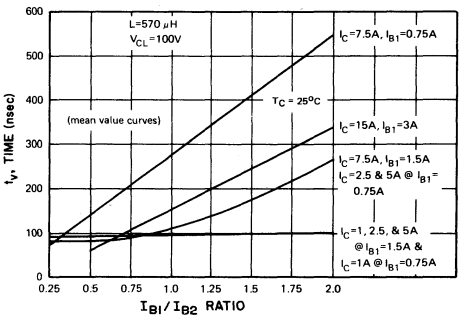


BASE DRIVE CURRENT RELATED SWITCHING CHARACTERISTICS

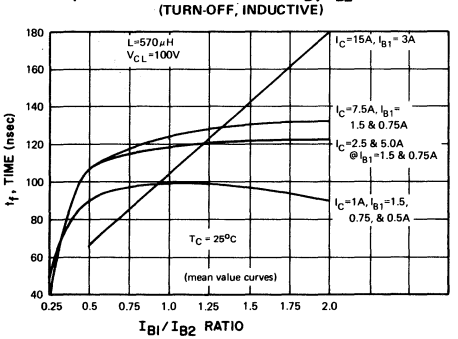
INDUCTIVE STORAGE TIME vs I_{B1}/I_{B2} RATIO



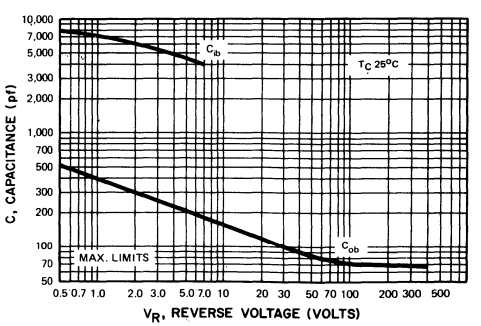
t_v, VOLTAGE RISE TIME vs I_{B1}/I_{B2} RATIO (TURN-OFF, INDUCTIVE)



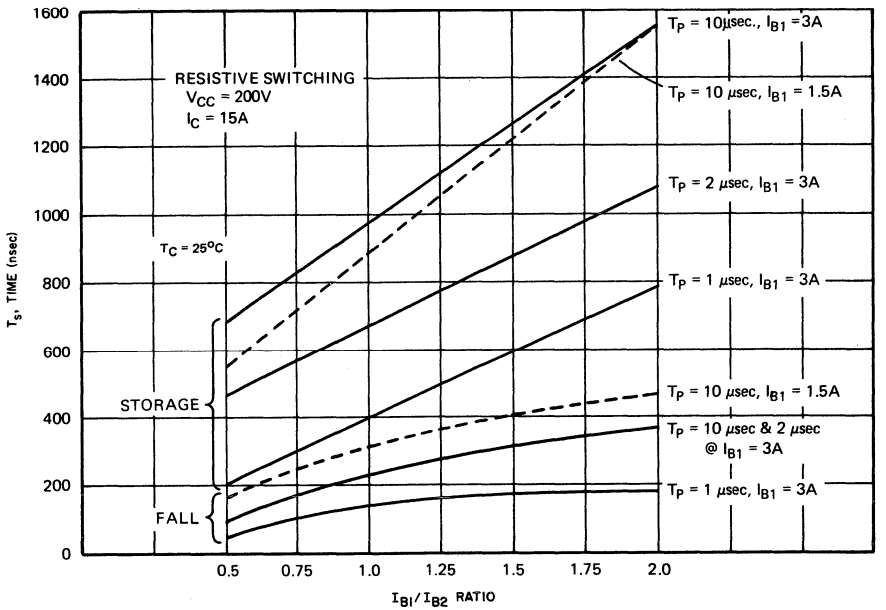
t_f, CURRENT FALL TIME vs I_{B1}/I_{B2} RATIO (TURN-OFF, INDUCTIVE)



CAPACITANCE

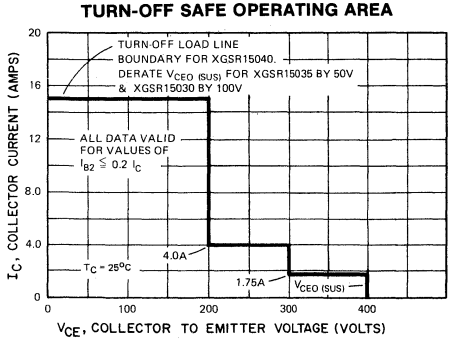


STORAGE & FALL TIME vs PULSE WIDTH (T_P)

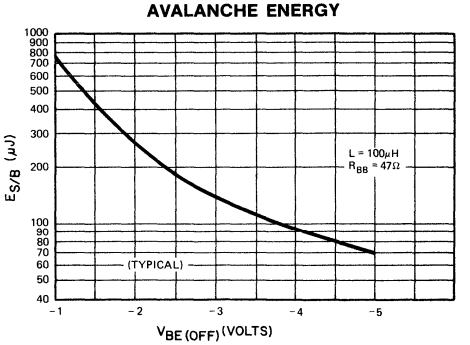


SAFE OPERATING AREA CHARACTERISTICS

TURN-OFF SAFE OPERATING AREA

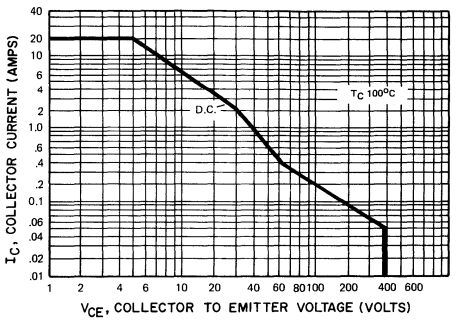


AVALANCHE ENERGY

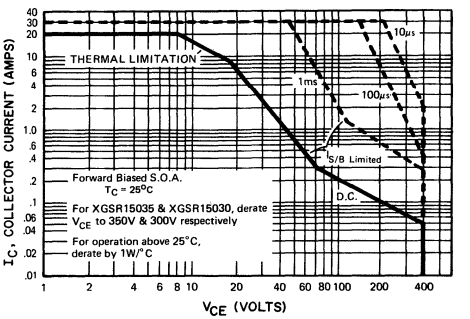


SAFE OPERATING AREA CHARACTERISTICS

FORWARD BIASED SAFE OPERATING AREA



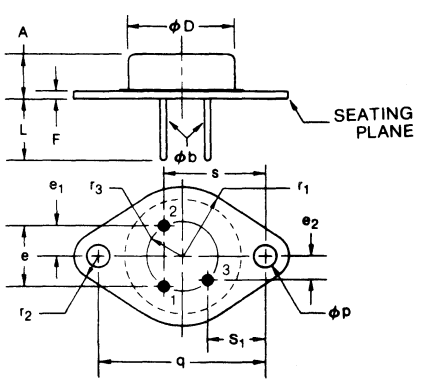
FORWARD BIASED SAFE OPERATING AREA



3

NPN SWITCHING TRANSISTORS

F-30
(3 Terminal TO-3)
Isolated Collector

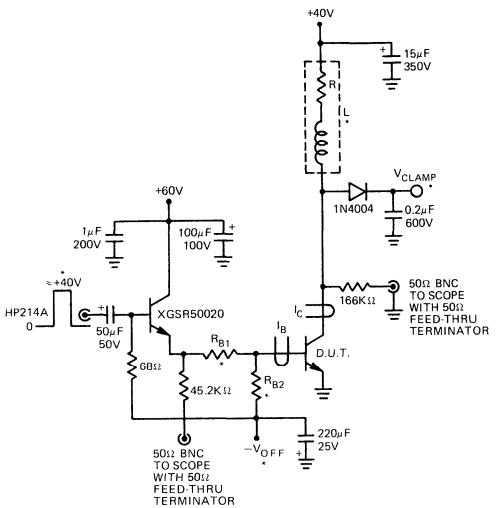


SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	6.35	11.43	0.250	0.450	
ϕb	0.97	1.09	0.038	0.043	3 leads
ϕD		22.23		0.875	
e	10.67	11.18	0.420	0.440	
e_1	5.21	5.72	0.205	0.225	
F		3.43		0.135	
L	7.92		0.312		3 leads
ϕp	3.84	4.09	0.151	0.161	
q	29.90	30.40	1.177	1.197	
r_1		13.34		0.525	
r_2		4.78		0.188	
s	16.64	17.15	0.700	0.730	
S_1	10.03	10.29	0.395	0.405	
e_2	3.68	4.19	0.145	0.165	
r_3	6.30	6.40	0.248	0.252	

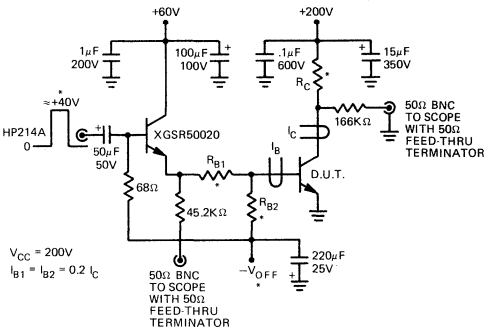
PIN DESCRIPTION:
1. BASE
2. EMITTER
3. COLLECTOR

TEST CIRCUITS

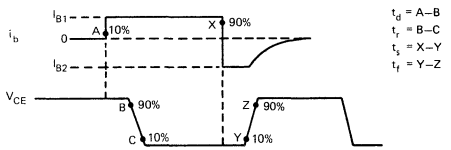
INDUCTIVE SWITCHING CIRCUIT



RESISTIVE SWITCHING CIRCUIT

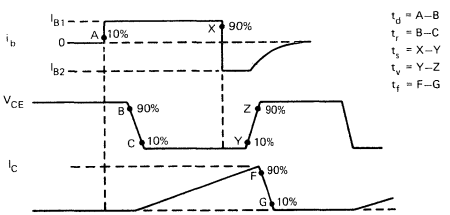


WAVEFORMS
RESISTIVE SWITCHING



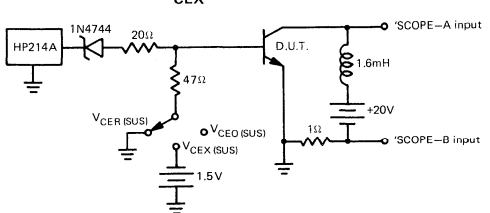
*(1) Select R_C for proper collector current @ 200V.
(2) R_{B1} & R_{B2} selected such that I_{B1} & I_{B2} are the desired values for an input pulse voltage of approximately 40V & $-V_{OFF}$ level of approximately 5V.
I_B & I_C measured with TEK P6302 current probe & AM503 amplifier.
Scope: TEK 7834 Storage Scope; 7892A Time Base; 7A26 dual amplifier.

WAVEFORMS
INDUCTIVE SWITCHING

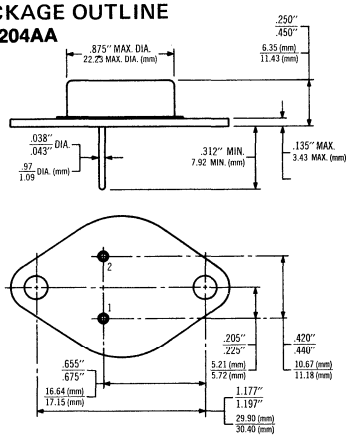


*(1) Value of L (inductor) specified on detail pages: $R_{D.C.}$ of 100μH coil is 0.29Ω; R_{DC} of 570μH is 0.3Ω.
(2) See Note 2 on Resistive Switching Schematic.
(3) See Resistive Switching Schematic for measurement equipment description.

V_{CEX} TEST CIRCUIT



PACKAGE OUTLINE
TO-204AA



General Semiconductor Industries, Inc.

2N6671
2N6672
2N6673

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The 2N6673 series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

NPN
300, 350, 400V
8 AMP SWITCHING
t_f — 250ns TYPICAL

TO-204 MA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted)

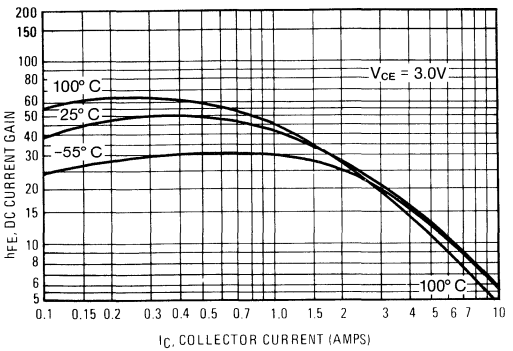
RATING	SYMBOL	2N6671	2N6672	2N6673	UNIT
Collector-Base Voltage	V_{CBO}	450	550	650	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous	I_C	8.0	8.0	8.0	Amps
Peak	I_{CM}	10	10	10	Amps
Base Current—Continuous	I_B	4.0	4.0	4.0	Amps
Total Power Dissipation @ T_C = 25° C	P_D	150	150	150	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.17	1.17	1.17	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

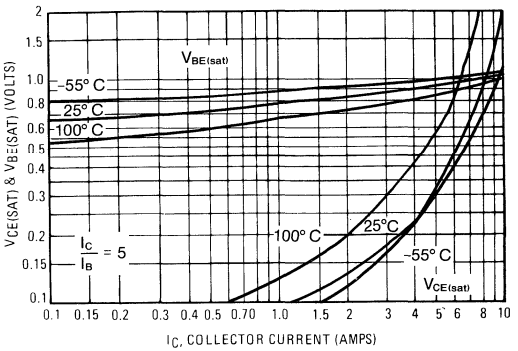
SYMBOL	CONDITIONS	2N6671		2N6672		2N6673		Unit
		Min	Max	Min	Max	Min	Max	
$V_{CEO(sus)}$	I_C = 200mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 2.0mA	8.0	—	8.0	—	8.0	—	Volts
I_{CEV}	V_{CE} = rated V_{CBO}, V_{EB} = 1.5V	—	100	—	100	—	100	μA
I_{CEV} 125° C	V_{CE} = rated V_{CBO}, V_{EB} = 1.5V	—	1.0	—	1.0	—	1.0	mA
h_{FE}†	V_{CE} = 3.0V, I_C = 5.0A	10	40	10	40	10	40	—
$V_{CE(sat)}$†	I_C = 5.0A, I_B = 1.0A	—	1.0	—	1.0	—	1.0	Volts
$V_{CE(sat)}$† 125° C	I_C = 5.0A, I_B = 1.0A	—	2.0	—	2.0	—	2.0	Volts
$V_{CE(sat)}$†	I_C = 8.0A, I_B = 4.0A	—	2.0	—	2.0	—	2.0	Volts
$V_{BE(sat)}$†	I_C = 5.0A, I_B = 1.0A	—	1.6	—	1.6	—	1.6	Volts
f_T	V_{CE} = 10V, I_C = 0.2A, f = 5.0MHz	15	60	15	60	15	60	MHz
C_{obo}	V_{CB} = 10V, f = 0.1MHz	50	300	50	300	50	300	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load**	0.04	0.1	0.04	0.10	0.04	0.1	μs
t_r	V_{CC} = 125V	0.20	0.5	0.20	0.5	0.20	0.5	μs
t_s	I_C = 5.0A, R = 25Ω	1.70	2.5	1.70	2.5	1.70	2.5	μs
t_f	I_{B1} = I_{B2} = 1.0A	0.25	0.4	0.25	0.4	0.25	0.4	μs
t_r 125° C	t_p = 20 μsec	—	0.8	—	0.8	—	0.8	μs
t_s 125° C		—	4.0	—	4.0	—	4.0	μs
t_f 125° C		—	0.8	—	0.8	—	0.8	μs
t_c	**Inductive Load**	0.35	0.4	0.35	0.4	0.35	0.4	μs
t_c 125° C	V_{CC} = 125V, I_C = 5.0A	—	0.8	—	0.8	—	0.8	μs
t_s	L = 170 μH, R = 25Ω	1.80	2.0	1.80	2.0	1.80	2.0	μs
t_s 125° C	I_{B1} = I_{B2} = 1.0A V_{CLAMP} = V_{CEO} plus 50V	—	3.0	—	3.0	—	3.0	μs

*JEDEC registered data. † Pulse conditions: Width = 10μs Duty Cycle ≤ 2% (measured using Kelvin connections).

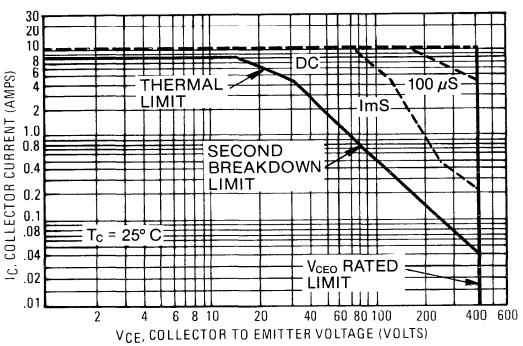
TYPICAL DC CURRENT GAIN



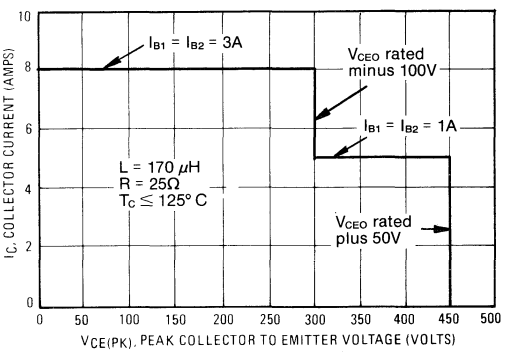
TYPICAL SATURATION VOLTAGE



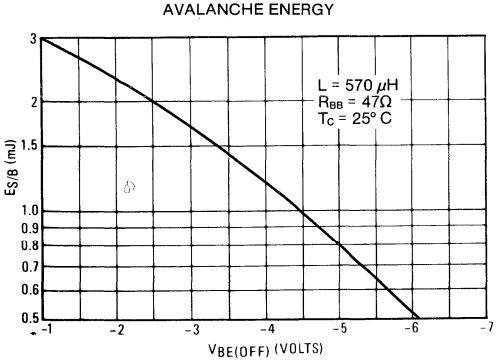
FORWARD BIASED SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA



AVALANCHE ENERGY



General Semiconductor Industries, Inc.

2N6676
2N6677
2N6678
2N6691
2N6692
2N6693

HIGH POWER NPN *Switch Plus*® TRANSISTORS

NPN
300, 350, 400V
15 AMP SWITCHING
t_f — 300ns TYPICAL

This rugged series of NPN transitors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long-term reliability.

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Motor Control**
- **Inverters/Converters**

2N6676-78 TO-204 MA (TO-3)
2N6691-93 TO-61/Iso

***MAXIMUM RATINGS** (Tc = 25°C unless otherwise noted)

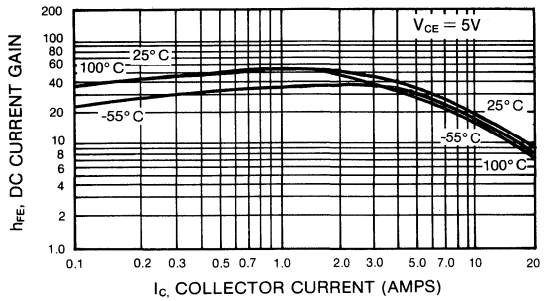
RATING	SYMBOL	2N6676/6691	2N6677/6692	2N6678/6693	UNIT
Collector-Base Voltage	V_{CBO}	450	550	650	Volts
Collector-Emitter Voltage	V_{CEX}	350	400	450	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous	I_C	15	15	15	Amps
Peak	I_{CM}	25	25	25	Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Total Power Dissipation @ T_C =25°C	P_D	175	175	175	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.0	1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

***ELECTRICAL CHARACTERISTICS** (Tc = 25°C unless otherwise noted)

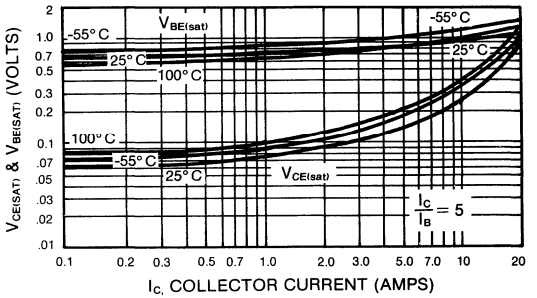
SYMBOL	CONDITIONS	2N6676 Min	2N6676 Max	2N6677 Min	2N6677 Max	2N6678 Min	2N6678 Max	Unit
I_{CEV}	Rated V_{CBO}, V_{EB} = 1.5V	—	0.1	—	0.1	—	0.1	mA
I_{CEV} 100°C	Rated V_{CBO}, V_{EB} = 1.5V	—	1.0	—	1.0	—	1.0	mA
I_{EBO}	V_{EB} = 8.0V	—	2.0	—	2.0	—	2.0	mA
$V_{CEO(sus)}$	I_C = 0.2A	300	—	350	—	400	—	Volts
h_{FE}†	I_C = 15A, V_{CE} = 3.0V	8.0	—	8.0	—	8.0	—	—
$V_{BE(sat)}$†	I_C = 15A, I_B = 3.0A	—	1.5	—	1.5	—	1.5	Volts
$V_{CE(sat)}$†	I_C = 15A, I_B = 3.0A	—	1.0	—	1.0	—	1.0	Volts
$V_{CE(sat)}$†100°C	I_C = 15A, I_B = 3.0A	—	2.0	—	2.0	—	2.0	Volts
f_T	I_C = 1.0A, V_{CE} = 10V, f = 5.0MHz	15	50	15	50	15	50	MHz
C_{OBO}	V_{CB} = 10V, f = 0.1MHz	150	500	150	500	150	500	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load** V_{CC} = 200V, I_C = 15A, I_{B1} = I_{B2} = 3.0A, t_p = 20μs, R = 13.5Ω	0.04	0.10	0.04	0.10	0.04	0.10	μs
t_r		0.30	0.60	0.30	0.60	0.30	0.60	μs
t_s		1.70	2.50	1.70	2.50	1.70	2.50	μs
t_f		0.30	0.50	0.30	0.50	0.30	0.50	μs
t_r 100°C		0.65	1.00	0.65	1.00	0.65	1.00	μs
t_s 100°C		2.20	4.00	2.20	4.00	2.20	4.00	μs
t_f 100°C		0.50	1.00	0.50	1.00	0.50	1.00	μs
t_s	**Inductive Load** V_{CC} = 200V, I_C = 15A, L = 50 μH, I_{B1} = I_{B2} = 3.0A, V_{BB2} = 6.0V, V_{CLAMP} = V_{CEO} rated +50V	1.90	2.70	1.90	2.70	1.90	2.70	μs
t_{rv}		0.20	0.30	0.20	0.30	0.20	0.30	μs
t_{fi}		0.09	0.16	0.09	0.16	0.09	0.16	μs
t_c		0.27	0.50	0.27	0.50	0.27	0.50	μs
t_s 100°C		2.10	3.50	2.10	3.50	2.10	3.50	μs
t_{rv} 100°C		0.25	0.35	0.25	0.35	0.25	0.35	μs
t_{fi} 100°C		0.13	0.25	0.13	0.25	0.13	0.25	μs
t_c 100°C		0.40	0.80	0.40	0.80	0.40	0.80	μs

* JEDEC registered data. † Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

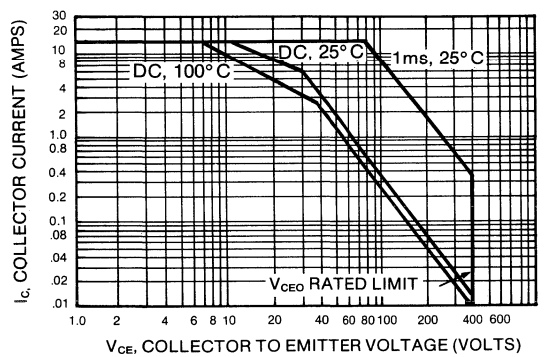
TYPICAL DC CURRENT GAIN



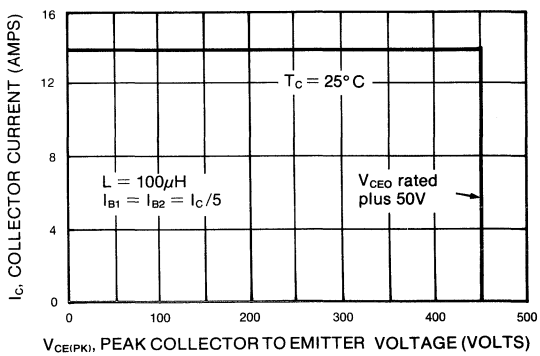
TYPICAL SATURATION VOLTAGE



FORWARD BIASED SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA



HIGH POWER NPN *Switch Plus®III* TRANSISTORS

These NPN silicon transistors offer an unprecedented combination of speed and ruggedness for use in high speed switching systems. This unique series also features General Semiconductor Industries' planar C²R® manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliability.

- **Off-line Power Supplies**
- **Inverters/Converters**
- **Switching Amplifiers**
- **Switching Regulators**

TO-204AA

NPN
UP TO
850V
V_{CEV}
UP TO
500V
INDUCTIVE SWITCHING
At Rated Current
15A
I_C (MAX)
10A
SWITCHING
35ns
t_c
TYPICAL

Switch Plus®III

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	2N6920/A	2N6921/A			UNIT
V_{CEV}	Collector-Emitter Voltage, Blocking	550/850	550/850			Volts
$V_{CEX(sus)}$	Collector-Emitter Voltage, Inductive Switching	450	500			Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining	400	450			Volts
V_{EBO}	Emitter-Base Voltage	8.0				Volts
I_C / I_{CM}	Collector Current—Continuous/Peak	15/20				Amps
I_E / I_{EM}	Emitter Current—Continuous/Peak	25/35				Amps
I_B / I_{BM}	Base Current—Continuous/Peak	10/15				Amps
P_D	Total Power Dissipation @ T_C = 25°C	175				Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range	-65 to +200				°C

***ELECTRICAL CHARACTERISTICS** (Applies to all types unless otherwise noted.)

				T_C = 25°C		T_C = 100°C		
SYMBOL	CONDITIONS		NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE								
$V_{CEO(sus)}$	I_C = 50mA		**2N6920(A)** **2N6921(A)**	400 450				Volts
I_{CEV}	V_{CE} = Rated V_{CEV}				1.0			mA
I_{CEV}	V_{CE} = 80% of Rated V_{CBO}, V_{EB} = 1.5V				10		100	μA
I_{EBO}	V_{EB} = 8.0V				1.0			mA
ON-STATE								
h_{FE}	I_C = 10A, V_{CE} = 2.0V		Pulsed: Notes 1 & 2	8.0				
$V_{CE(sat)}$	I_C = 10A, I_B = 2.0A				1.0		1.5	Volts
$V_{CE(sat)}$	I_C = 15A, I_B = 3.0A				2.5			Volts
$V_{CE(sat)}$	I_C = 20A, I_B = 5.0A		Pulsed: Notes 1 & 3		4.0			Volts
$V_{BE(sat)}$	I_C = 10A, I_B = 2.0A		Pulsed: Notes 1 & 2		1.5		1.5	Volts
DYNAMIC								
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz		Pulsed: Note 2	20	60			MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz			120	350			pF
t_d	I_C = 10A I_{B1} = 2.0A	**Resistive Load** V_{CC} = $V_{CEX(sus)}$			20			ns
t_r					100			ns
t_{sd} (t_f)		**Current Source Load**	Measured to 10V		1.0		2.0	μs
t_{sv}		**Inductive Load**			1.3		1.5	μs
t_{rv}	I_C = 10A	t_p = 30μs			30		40	ns
t_{fi}	I_{B1} = 2.0A	L = 100μH			30		40	ns
t_c	I_{B2} = 4.0A	V_{CLAMP} = $V_{CEX(sus)}$			50		70	ns
THERMAL								
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A		**2N6920(A), 21(A)**		1.0			°C/W

Notes: 1) Measured using Kelvin connections
2) Pulse measurement conditions: Length 300μs, Duty cycle 2%
3) Pulse measurement conditions: Length 10μs, Duty cycle 2%

*JEDEC Registered Data

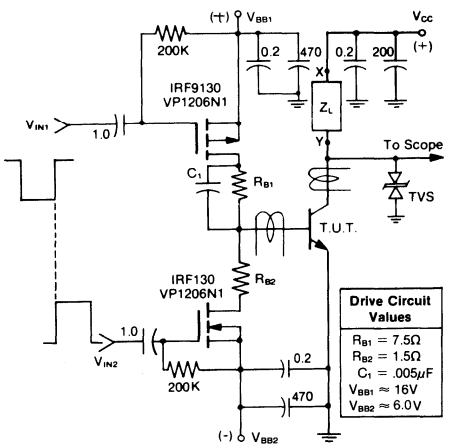


Figure 1—Switching Test Circuit

Load Circuit Values				
Test	$V_{CE(PK)}$	V_{CC}	Z_L	TVS
Resistive				
2N6920	—	450V	45Ω	—
2N6921	—	500V	50Ω	—
Inductive				
2N6920, 80(A)	450V	30V	100μH	SA160C & SA170C
2N6921, 81(A)	500V	30V	100μH	SA170C & SA180C
Dynamic Saturation	—	50V	Fig. 2	—

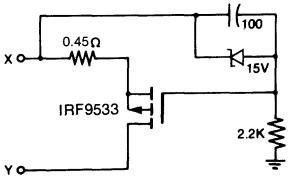


Figure 2—Current Source Load (Z_L)

Notes:

1. Capacitance values in μFd.
2. For inductive switching, the Transient Voltage Suppressor (TVS) diode is selected to allow $V_{CE(PK)}$ to equal rated $V_{CEX(sus)}$. Since some overshoot caused by circuit inductance and TVS heating is inevitable, the specified TVS breakdown voltage will be about 100 volts less than $V_{CEX(sus)}$. Correct voltage may be achieved by stacking TVS diodes and by making minor adjustments in the duty cycle.
3. For resistive switching, R_L is composed of a stack of 2W carbon resistors which may need to be trimmed to obtain the correct I_C. For inductive switching, $I_C \approx t_{ON} V_{CC} / L$. V_{CC} may need minor adjustment to obtain correct I_C. Duty cycle ≤ 1%.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided heavy foil P.C.B. is suggested for the driver stage.
5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic® and metallized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. C_1 is chosen to achieve an essentially flat topped current pulse. V_{BB1} and V_{BB2} are adjusted to obtain correct values for the base currents, I_{B1} and I_{B2}.
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

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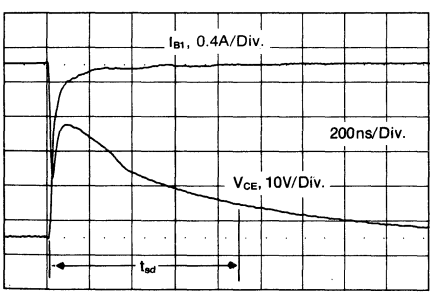


Figure 3—Dynamic Saturation Waveforms

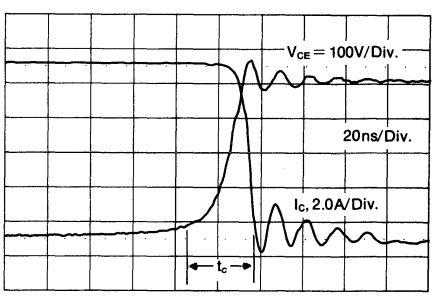


Figure 4—Crossover Waveforms

Digitized Waveforms

STORAGE TIME

Figure 5—Effect of Collector Current

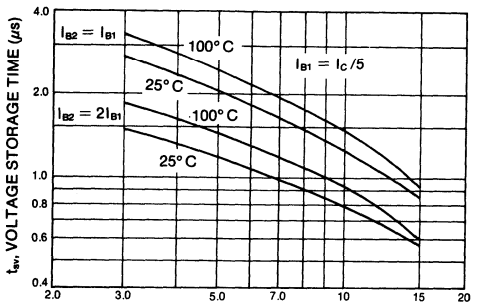
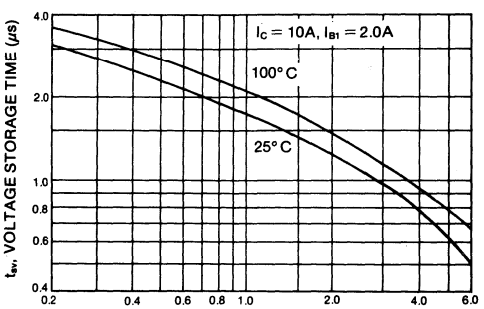


Figure 6—Effect of Reverse Drive



CROSSOVER TIME

Figure 7—Effect of Collector Current

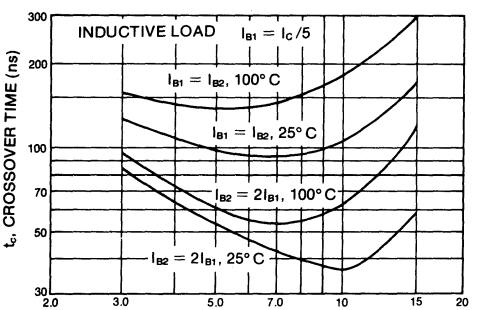
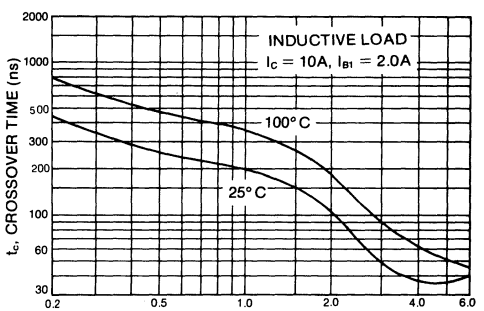


Figure 8—Effect of Reverse Drive



TURN ON TIME

Figure 9—Rise Time

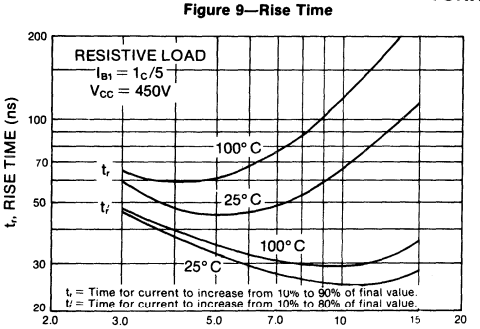
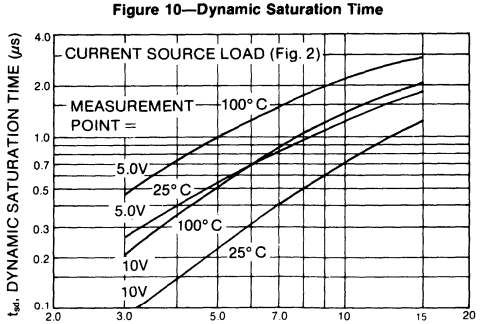


Figure 10—Dynamic Saturation Time



RATINGS & TYPICAL DC CHARACTERISTICS

Figure 11—DC Current Gain

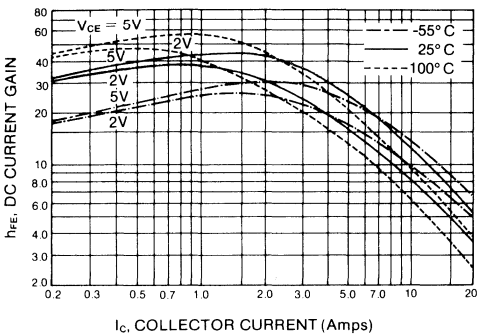


Figure 12—Forward Biased Safe Operating Area

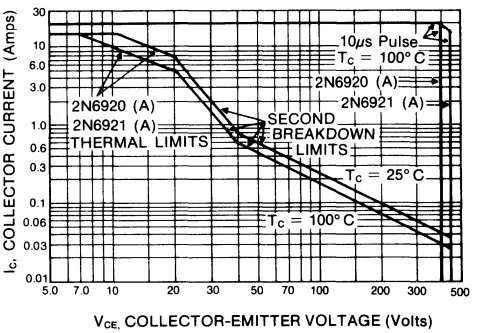


Figure 13—Saturation Voltage

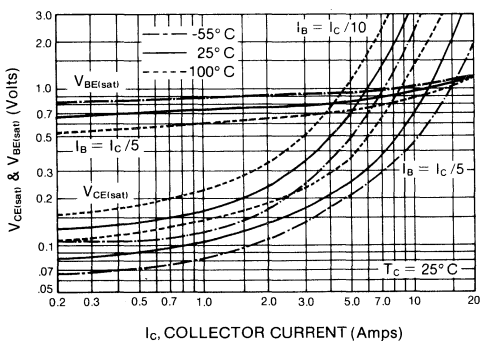


Figure 14—Power Derating

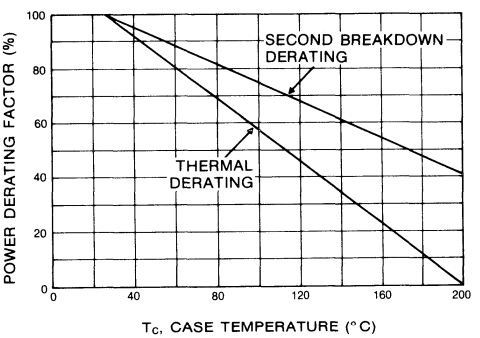


Figure 15—Saturation Region

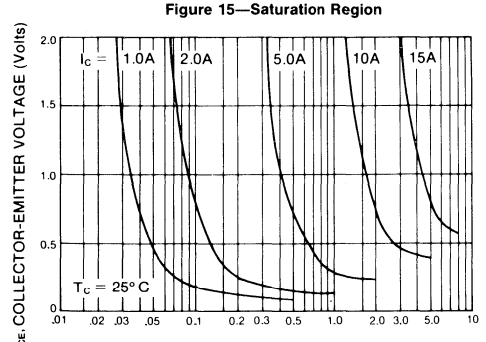
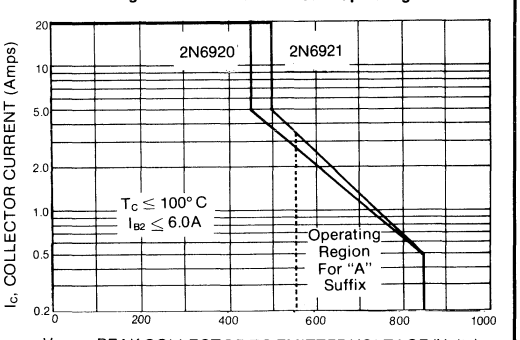


Figure 16—Reverse Bias Safe Operating Area



General Semiconductor Industries, Inc.

2N6922, 2N6922A 2N6923, 2N6923A

HIGH POWER NPN *Switch Plus®III* TRANSISTORS

These NPN silicon transistors offer an unprecedented combination of speed and ruggedness for use in high speed switching systems. This unique series also features General Semiconductor Industries' planar C^2R manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliablity.

- **Off-line Power Supplies**
- **Inverters/Converters**
- **Switching Amplifiers**
- **Switching Regulators**

TO-204AA

NPN
UP TO
850V
V_{CEV}
UP TO
500V
INDUCTIVE SWITCHING
At Rated Current

20A
I_C (MAX)

15A
SWITCHING

35ns
t_c
TYPICAL

Switch Plus®III

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	2N6922/A	2N6923/A			UNIT
V_{CEV}	Collector-Emitter Voltage, Blocking	550/850	550/850			Volts
$V_{CEX(sus)}$	Collector-Emitter Voltage, Inductive Switching	450	500			Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining	400	450			Volts
V_{EBO}	Emitter Base Voltage	8.0				Volts
I_C	Collector Current—Continuous/Peak	20/30				Amps
I_E	Emitter Current—Continuous/Peak	30/40				Amps
I_B	Base Current—Continuous/Peak	10/15				Amps
P_D	Total Power Dissipation @ T_C = 25°C	220				Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range	- 65 to +200				°C

***ELECTRICAL CHARACTERISTICS** (Applies to all types unless otherwise noted.)

			T_C = 25°C		T_C = 100°C		
SYMBOL	CONDITIONS	PART NO/NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
$V_{CEO(sus)}$	I_C = 50mA	**2N6923 (A)** **2N6922 (A)**	400 450				Volts
I_{CEV}	V_{CE} = Rated V_{CEV}, V_{EB} = 1.5V			1.0			mA
I_{CEV}	V_{CE} = 0.8 Rated V_{CEV}, V_{EB} = 1.5V			10		100	μA
I_{EBO}	V_{EB} = 8.0V			1.0			mA
ON-STATE							
h_{FE}	I_C = 15A, V_{CE} = 2.0V	Pulsed: Notes 1 & 2	8.0				
$V_{CE(sat)}$	I_C = 15A, I_B = 3.0A			1.0		1.5	Volts
$V_{CE(sat)}$	I_C = 20A, I_B = 5.0A			2.0			Volts
$V_{CE(sat)}$	I_C = 30A, I_B = 10A	Pulsed: Notes 1 & 3		5.0			Volts
$V_{BE(sat)}$	I_C = 15A, I_B = 3.0A	Pulsed: Notes 1 & 2		1.5			Volts
DYNAMIC							
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	Pulsed: Note 2	15	50			MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz		200	500			pF
t_d	I_C = 15A, I_{B1} = 3.0A — **Resistive Load** V_{CC} = $V_{CEX(sus)}$			20			ns
t_r				50			ns
t_{sd} (t_i)	**Current Source Load**	Measured to 10V		1.0		3.0	μs
t_{sv}	**Inductive Load**			1.0		1.5	μs
t_{rv}	I_C = 15A, t_p = 30μsec			30		40	ns
t_{fi}	I_{B1} = 3.0A, L = 100μH			30		40	ns
t_c	I_{B2} = 6.0A, V_{CLAMP} = $V_{CEX(sus)}$			50		70	ns
THERMAL							
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A	**2N6922, 3 (A)**		0.8			°C/W

Notes: 1) Measured using Kelvin connections.
2) Pulse measurement conditions: Length = 300μs. Duty cycle < 2%.
3) Pulse measurement conditions: Length = 10μs. Duty cycle < 2%.

*JEDEC registered data.

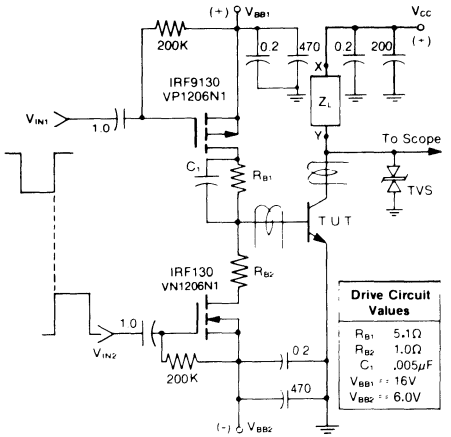


Figure 13—Switching Test Circuit

Load Circuit Values				
Test	$V_{CE(PK)}$	V_{CC}	Z_L	TVS
Resistive				
2N6922	—	450V	30Ω	—
2N6923	—	500V	33Ω	—
Inductive				
2N6922	450V	50V	100μH	2 - SA160CA
2N6923	500V	50V	100μH	2 - SA170CA
Dynamic Saturation	—	50V	Fig. 14	—

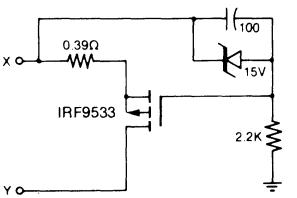


Figure 14—Current Source Load (Z_L)

Notes:

1. Capacitance values in μFd.
2. For inductive switching, the Transient Voltage Suppressor (TVS) diode is selected to allow $V_{CE(PK)}$ to equal rated $V_{CEX(sus)}$. Since some overshoot caused by circuit inductance and TVS heating is inevitable, the specified TVS breakdown voltage will be about 100 volts less than $V_{CEX(sus)}$. Correct voltage may be achieved by stacking TVS diodes and by making minor adjustments in the duty cycle.
3. For resistive switching, R_L is composed of a stack of 2W carbon resistors which may need to be trimmed to obtain the correct I_C. For inductive switching, $I_C \approx T_{ON} V_{CC}/L$. V_{CC} may need minor adjustment to obtain correct I_C. Duty cycle $\leq 1\%$.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided heavy foil P.C.B. is suggested for the driver stage.
5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic® and metalized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. C_1 is chosen to achieve an essentially flat topped current pulse. V_{BB1} and V_{BB2} are adjusted to obtain correct values for the base currents, I_{B1} and I_{B2}.
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

*Registered trademark of Sprague Electric Co.

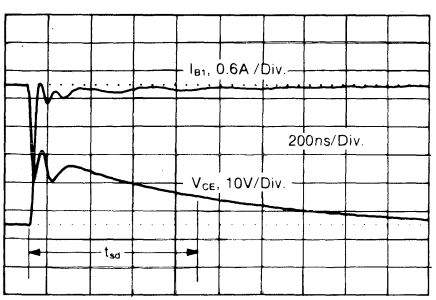


Figure 15—Dynamic Saturation Waveforms

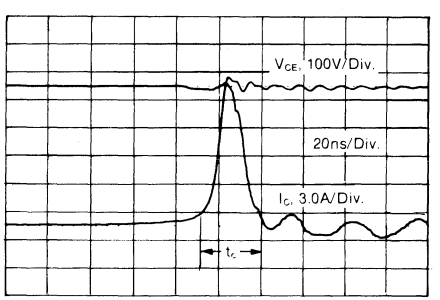


Figure 16—Crossover Waveforms

Digitized Waveforms

INDUCTIVE TURN-OFF CHARACTERISTICS

CROSSOVER TIME

Figure 7—Effect of Collector Current Proportional Drive

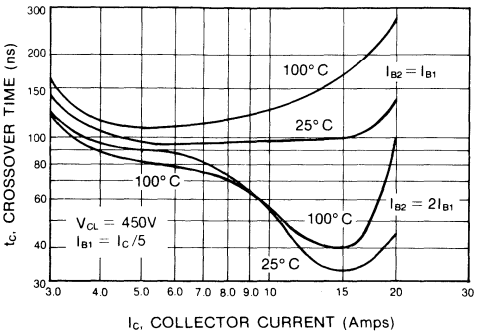


Figure 9—Effect of Collector Current Fixed Drive

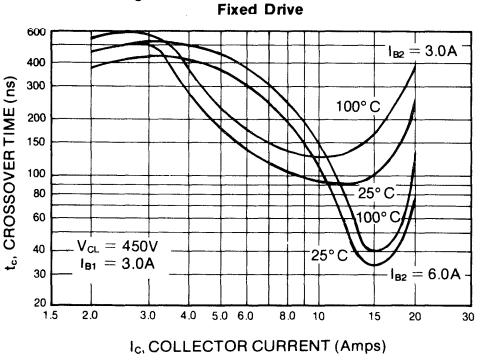
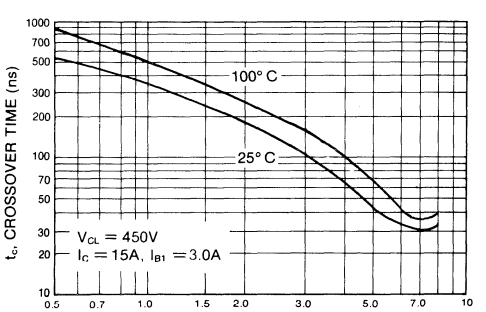


Figure 11—Effect of Reverse Drive



CURRENT FALL TIME

Figure 8—Effect of Collector Current Proportional Drive

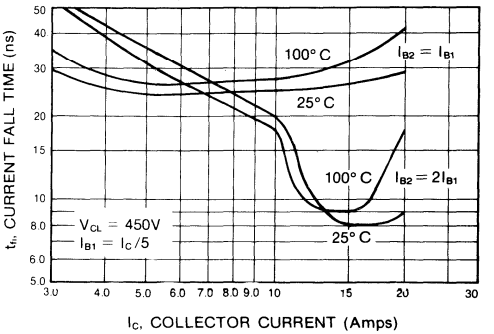


Figure 10—Effect of Collector Current Fixed Drive

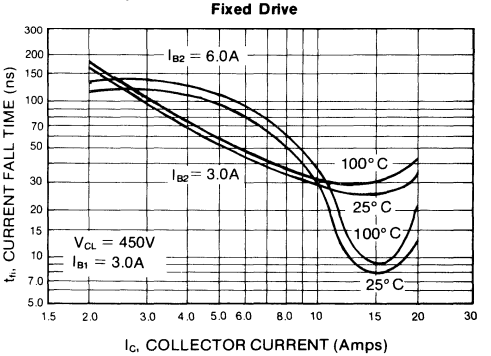
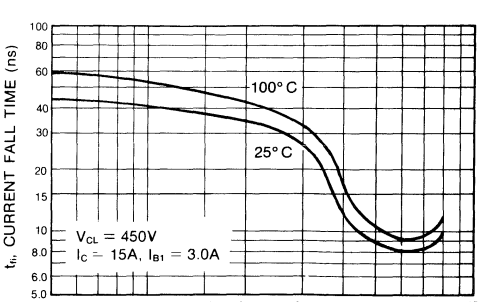


Figure 12—Effect of Reverse Drive



TURN ON TIME

Figure 1—Rise Time

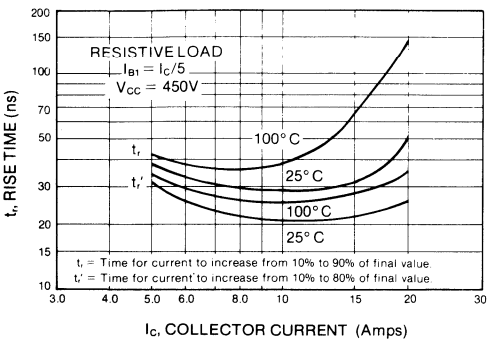
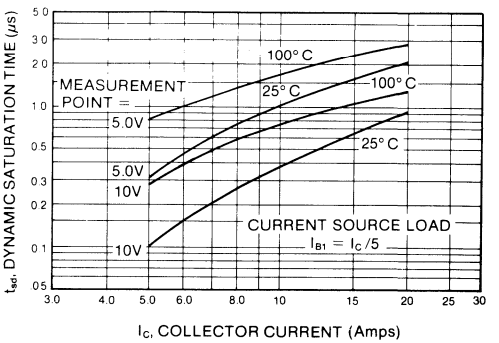


Figure 2—Dynamic Saturation Time



STORAGE TIME

Figure 3—Effect of Collector Current Proportional Drive

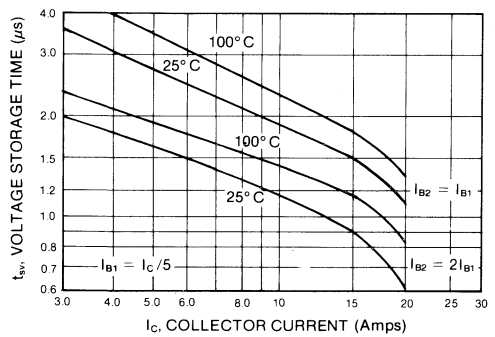


Figure 4—Effect of Collector Current Fixed Drive

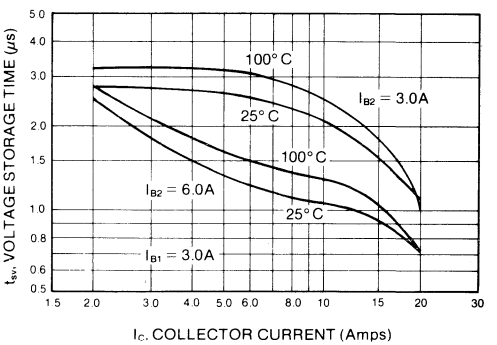


Figure 5—Effect of Pulse Width

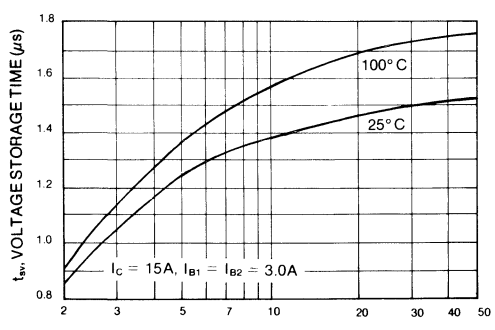
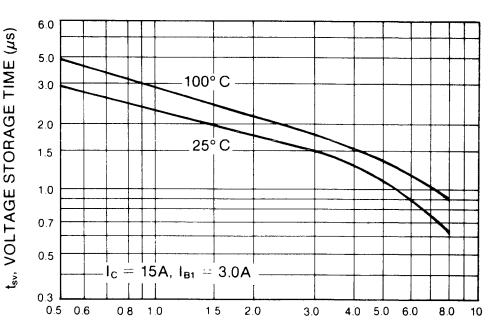


Figure 6—Effect of Reverse Drive



TYPICAL DC CHARACTERISTICS & RATINGS

Figure 17—DC Current Gain

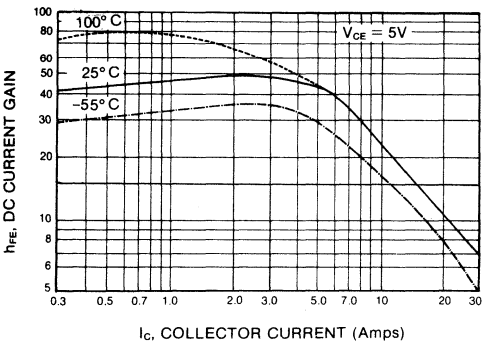


Figure 18—Forward Biased Safe Operating Area

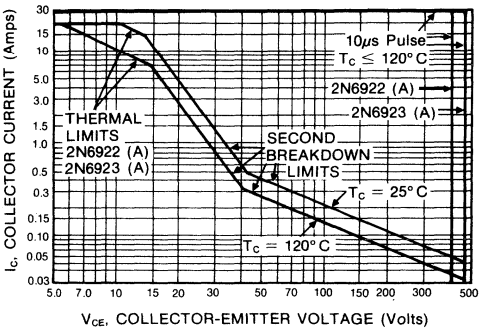


Figure 19—Saturation Voltage

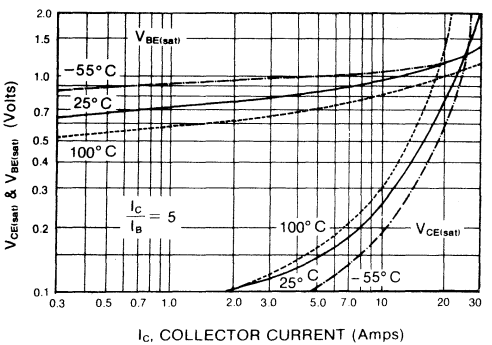


Figure 20—Power Derating

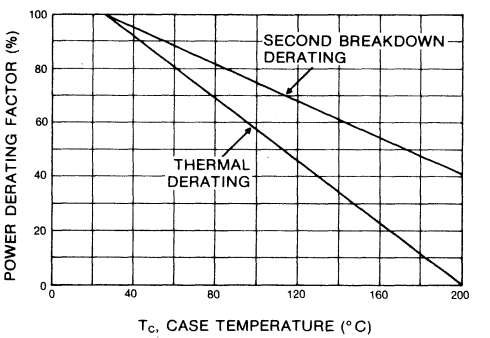


Figure 21—Saturation Region

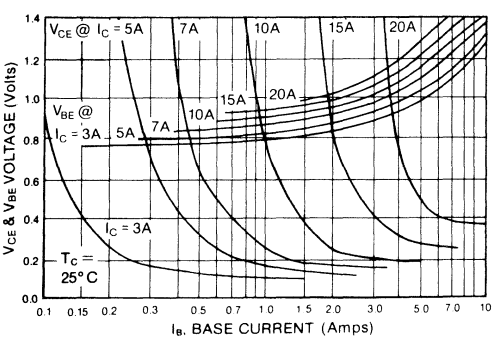
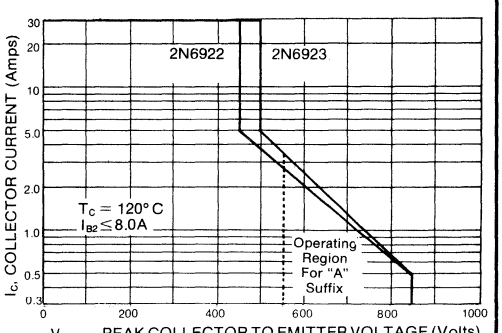
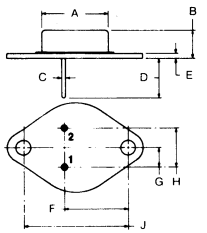


Figure 22—Reverse Bias Safe Operating Area



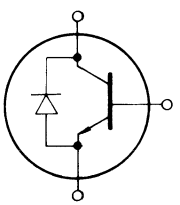
Package Outline TO-204AA



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.875	—	22.23
B	.250	.450	6.35	11.43
C	.038	.043	.97	1.09
D	.312	—	7.92	—
E	—	.135	—	3.43
F	.655	.675	16.64	17.15
G	.205	.225	5.21	5.72
H	.420	.440	10.67	11.18
J	1.177	1.197	29.90	30.40

Pin 1 Base
2 Emitter
Case Collector

(FORMERLY TO-3)



Note:

The technology utilized to produce these devices results in an internal diode between the collector and emitter. In some cases this may eliminate the need for an external diode to clamp inductive loads. At 20 A, t_{rr} = 600 ns and V_F = 1.25V (typical).

General Semiconductor Industries, Inc.

2N6924
2N6924A
2N6925
2N6925A

HIGH POWER NPN *Switch Plus®III* TRANSISTORS

These NPN silicon transistors offer an unprecedented combination of speed and ruggedness for use in high speed switching systems. This unique series also features General Semiconductor Industries' C²R® manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliability.

- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Switching Regulators**

TO-204AE

NPN

UP TO 850V V_{CEV}

UP TO 500V INDUCTIVE SWITCHING At Rated Current

35A $I_{C(MAX.)}$

25A SWITCHING

35ns t_c TYPICAL

Switch Plus®III

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION		2N6924/A	2N6925/A	UNIT
V_{CEV}	Collector-Emitter Voltage, Blocking		550/850	550/850	Volts
$V_{CEX(sus)}$	Collector-Emitter Voltage, Inductive Switching		450	500	Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining		400	450	Volts
V_{EBO}	Emitter-Base Voltage		8.0		Volts
I_C	Collector Current—Continuous/Peak		35/50		Amps
I_E	Emitter Current—Continuous/Peak		50/70		Amps
I_B	Base Current—Continuous/Peak		15/20		Amps
P_D	Total Power Dissipation T_C = 25° C		300		Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range		-65 to +200		°C

***ELECTRICAL CHARACTERISTICS** (Applies to all types unless otherwise noted.)

			T_C = 25° C		T_C = 100° C		
SYMBOL	CONDITIONS	PART NO/NOTES	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
$V_{CEO(sus)}$	I_C = 50mA	2N6924/A 2N6925/A	400 450				Volts
I_{CEV}	V_{CE} = 550V			1.0			mA
I_{CEV}	V_{CE} = 440V, V_{EB} = 1.5V			10		100	μA
I_{EBO}	V_{EB} = 8.0V			1.0			mA
ON-STATE							
h_{FE}	I_C = 25A, V_{CE} = 2.0V	Pulsed: Notes 1 & 2	8.0				
$V_{CE(sat)}$	I_C = 25A, I_B = 5.0A			1.0		1.5	Volts
$V_{CE(sat)}$	I_C = 35A, I_B = 9.0A			2.0			Volts
$V_{CE(sat)}$	I_C = 50A, I_B = 15A	Pulsed: Notes 1 & 3		5.0			Volts
$V_{BE(sat)}$	I_C = 25A, I_B = 5.0A	Pulsed: Notes 1 & 2		1.5			Volts
DYNAMIC							
f_T	V_{CE} = 10V, I_C = 2.0A, f = 10MHz	Pulsed: Note 2	15	50			MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz		300	800			pF
t_d	I_C = 25A, I_{B1} = 5.0A — **Resistive Load**, V_{CC} = $V_{CEX(sus)}$			20			ns
t_r				100			ns
t_{sd} (t_f)	**Current Source Load**	Measured to 10V		1.0		3.0	μs
t_{sv}	**Inductive Load**			1.3		1.6	μs
t_{rv}	I_C = 25A, I_{B1} = 5.0A, I_{B2} = 10A, t_p = 30μsec, L = 100μH, V_{CLAMP} = $V_{CEX(sus)}$			30		60	ns
t_{fi}				30		40	ns
t_c				50		90	ns
THERMAL							
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A			0.583			°C/W

Notes: 1) Measured using Kelvin connections.
2) Pulse measurement conditions: Length = 300μs. Duty cycle · 2%.
3) Pulse measurement conditions: Length - 10μs. Duty cycle ·. 2%.

*JEDEC Registered data.

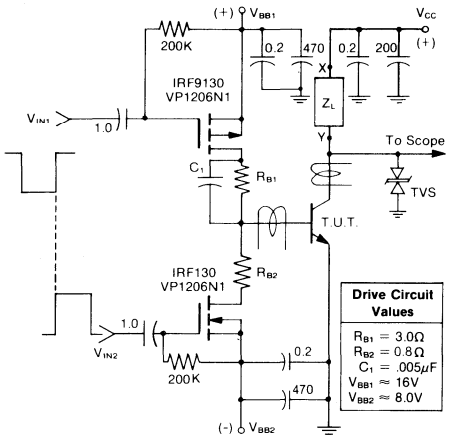


Figure 1—Switching Test Circuit

Load Circuit Values				
Test	$V_{CE(PK)}$	V_{CC}	Z_L	TVS
Resistive				
2N6924	—	450V	18Ω	—
2N6925	—	500V	20Ω	—
Inductive				
2N6924	450V	50V	100μH	2 - SA120C
2N6925	500V	50V	100μH	2 - SA130C
Dynamic Saturation	—	50V	Fig. 2	—

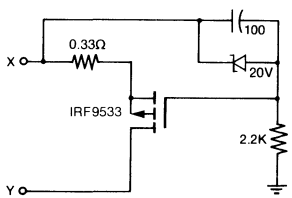


Figure 2—Current Source Load (Z_L)

Notes:

1. Capacitance values in μFd.
2. For inductive switching, the Transient Voltage Suppressor (TVS) diode is selected to allow $V_{CE(PK)}$ to equal rated $V_{CEX(sus)}$. Since some overshoot caused by circuit inductance and TVS heating is inevitable, the specified TVS breakdown voltage will be about 100 volts less than $V_{CEX(sus)}$. Correct voltage may be achieved by stacking TVS diodes and by making minor adjustments in the duty cycle.
3. For resistive switching, R_L is composed of a stack of 2W carbon resistors which may need to be trimmed to obtain the correct I_C. For inductive switching, $I_C \approx T_{ON} V_{CC} / L$. V_{CC} may need minor adjustment to obtain correct I_C. Duty cycle ≤ 1%.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided heavy foil P.C.B. is suggested for the driver stage.
5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic® and metallized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. C_1 is chosen to achieve an essentially flat topped current pulse. V_{BB1} and V_{BB2} are adjusted to obtain correct values for the base currents, I_{B1} and I_{B2}.
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

®Registered trademark of Sprague Electric Co.

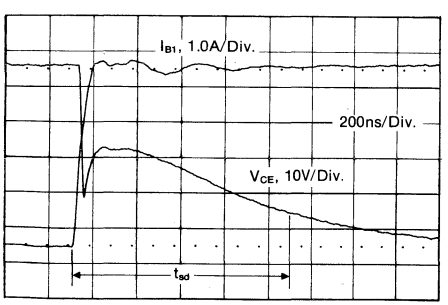


Figure 3—Dynamic Saturation Waveforms

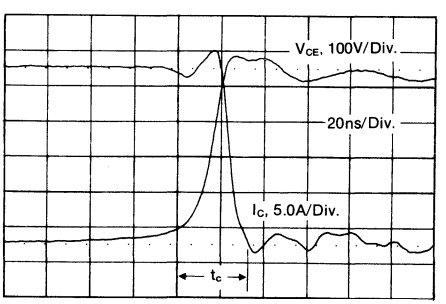


Figure 4—Crossover Waveform

Digitized Waveforms

STORAGE TIME

Figure 5—Effect of Collector Current

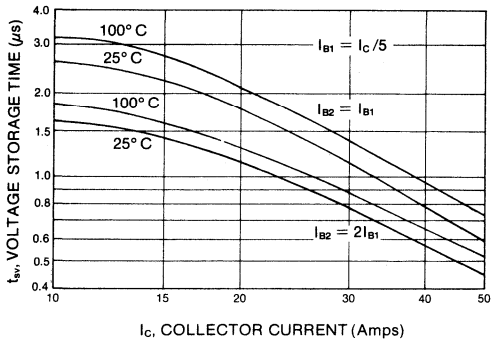
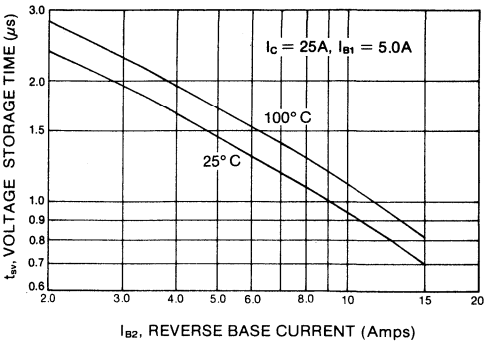


Figure 6—Effect of Reverse Drive



CROSSOVER TIME

Figure 7—Effect of Collector Current

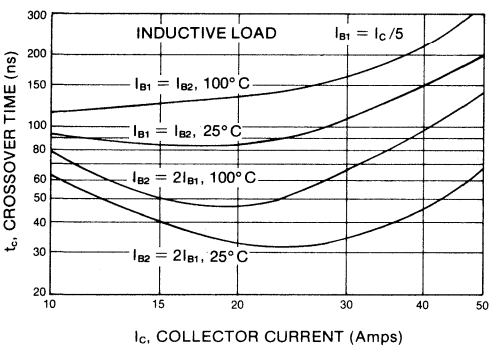
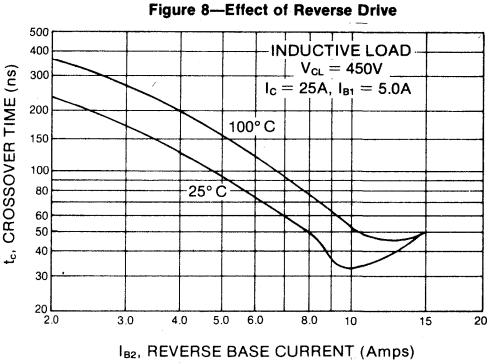


Figure 8—Effect of Reverse Drive



TURN ON TIME

Figure 9—Rise Time

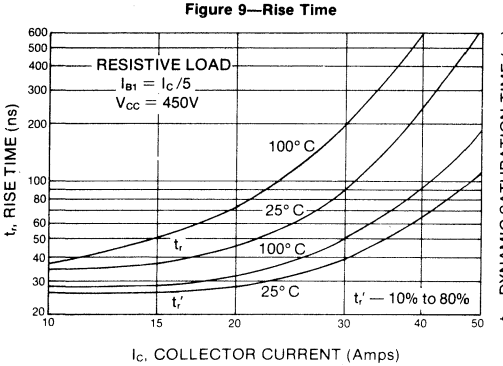
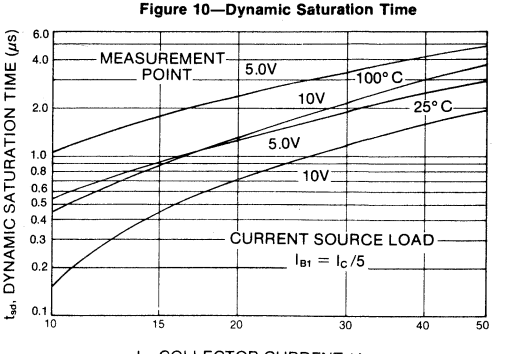


Figure 10—Dynamic Saturation Time



TYPICAL DC CHARACTERISTICS & RATINGS

Figure 11—DC Current Gain

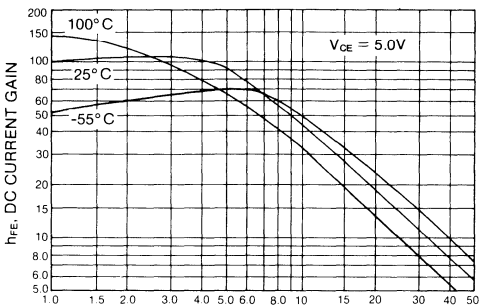


Figure 12—Forward Biased Safe Operating Area

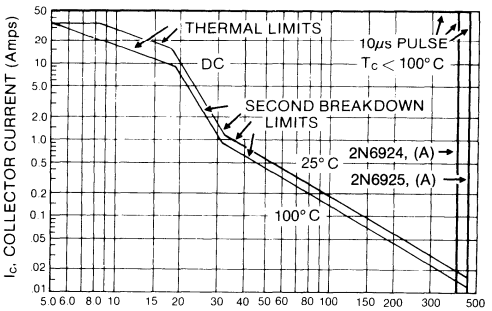


Figure 13—Saturation Voltage

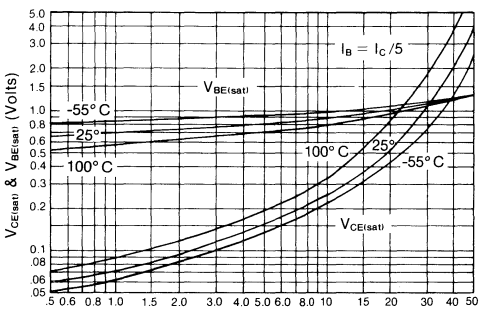


Figure 14—Power Derating

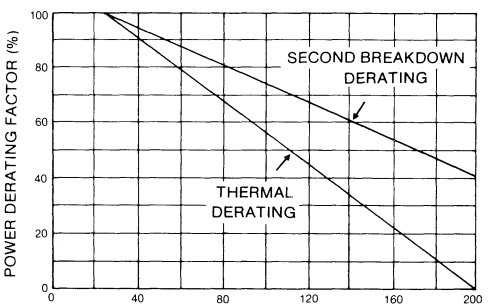


Figure 15—Saturation Region

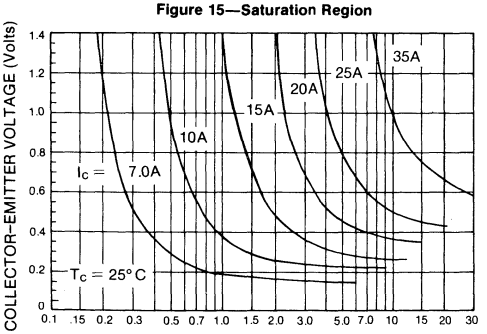
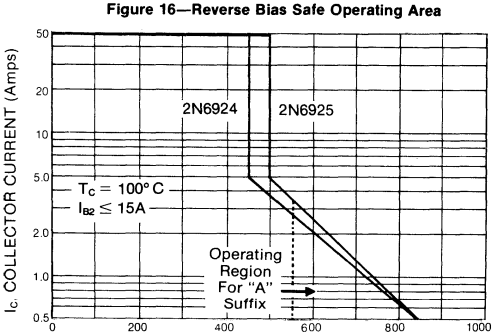


Figure 16—Reverse Bias Safe Operating Area



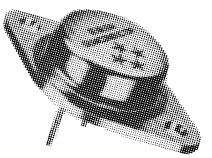
General Semiconductor Industries, Inc.

NPN 180, 200 V. 50 Amp Switching GSDS50018, 20 C²R®

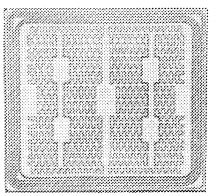
C²R® HIGH SPEED/ HIGH POWER SWITCHING TRANSISTORS

The GSD series is a reliable NPN double diffused epitaxial transistor designed for high speed switching systems. This unique series utilizes General Semiconductor Industries' C²R process (patent applied for) which describes a manufacturing technology that provides surface stabilization for high voltage operation and enhances long term reliability. Another design feature is the use of an interdigitated emitter providing a periphery greater than 7.0 inches (18cm) which improves both the gain characteristics and current handling capability.

These transistors have been specifically designed and engineered for high speed/high voltage switching applications where the designer is concerned with optimizing power conversion efficiency.



TO-204AE (TO-3)



C²R

FEATURES:
- HIGH VOLTAGE
- HIGH GAIN
- HIGH CURRENT
- LOW SATURATION VOLTAGES
- FAST SWITCHING
- RADIATION RESISTANT

APPLICATIONS:
- HIGH SPEED SWITCHING
- POWER CONVERSION
- CONVERTERS
- INVERTERS
- CLASS D AMPLIFIERS
- CLASS C AMPLIFIERS

$V_{CE(sat)}$ at 50 AMPS typically 0.6V

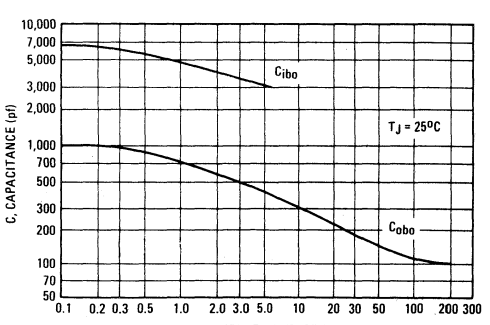
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

RATING	SYMBOL	GSDS50018	GSDS50020	UNIT
Collector-Base Voltage	V_{CBO}	180	200	Volts
Collector-Emitter Voltage	$V_{CEO(SUS)}$	180	200	Volts
Emitter-Base Voltage	V_{EBO}	7.0	7.0	Volts
Collector Current—Continuous Peak	I_C I_{CM}	50 75	50 75	Amps Amps
Base Current—Continuous	I_B	20	20	Amps
Total Power Dissipation @ T_C = 100°C	P_D	100	100	Watts
Θ_{J-C}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ & T_{stg}	-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)						
SYMBOL	CONDITIONS	GSDS50018		GSDS50020		UNIT
		Min	Max	Min	Max	
V_{CBO}	I_C = 1.0mA	180	—	200	—	Volts
$V_{CEO(SUS)}$	I_C = 50mA	180	—	200	—	Volts
V_{EBO}	I_E = 1.0mA	7.0	—	7.0	—	Volts
I_{EBO}	V_{EB} = 6.0V	—	100	—	100	μA
I_{CEO}	V_{CE} = 80% Rated	—	50	—	50	μA
I_{CEX}	V_{CE} = 80% Rated, V_{BE} = −1.5V	—	10.0	—	10.0	μA
$E_{S/B}$	L = 50μH, $V_{BE(OFF)}$ = −1V, R_{BB} = 47Ω	750	—	750	—	μJ
h_{FE}	V_{CE} = 4.0V, I_C = 50A†	8	—	8	—	—
$V_{CE(sat)}$	I_C = 50A, I_B = 10A†	—	1.0	—	1.0	Volts
$V_{BE(sat)}$	I_C = 50A, I_B = 10A†	—	2.0	—	2.0	Volts
$\|h_{fe}\|$	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	3.0	—	3.0	—	—
C_{obo}	V_{CB} = 10V, f = 1MHz	—	350	—	350	pF
t_d	V_{CC} = 100V, I_C = 50A, I_{B1} = I_{B2} = 10A, t_p = 10μs, Duty Cycle <2.0%, Resistive Load.	—	0.04	—	0.04	μsec
t_r		—	0.2	—	0.2	μsec
t_s		—	0.75	—	0.75	μsec
t_f		—	0.175	—	0.175	μsec

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

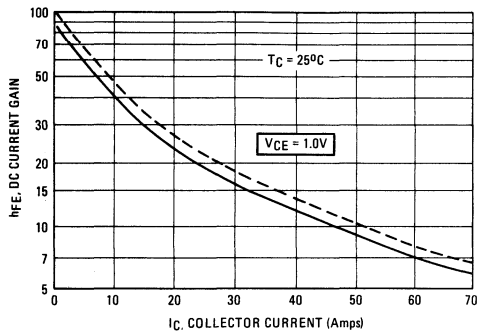
CAPACITANCE



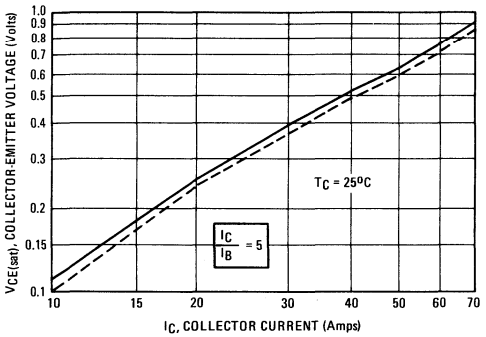
DOTTED LINES – MEDIAN
SOLID LINES – 90TH PERCENTILE

DC CHARACTERISTICS

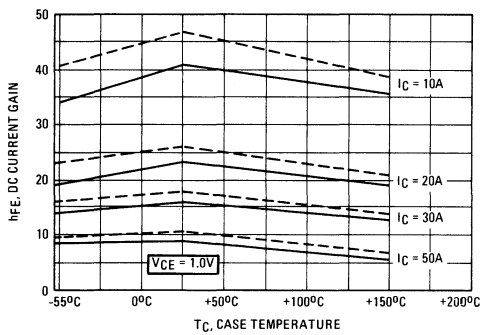
DC CURRENT GAIN



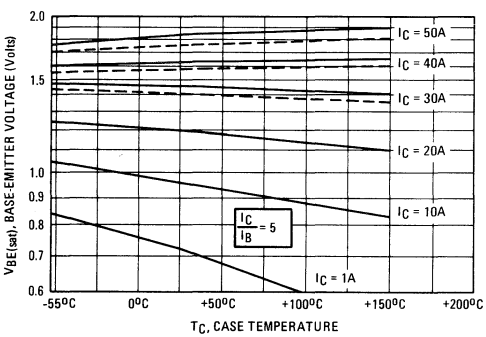
COLLECTOR SATURATION



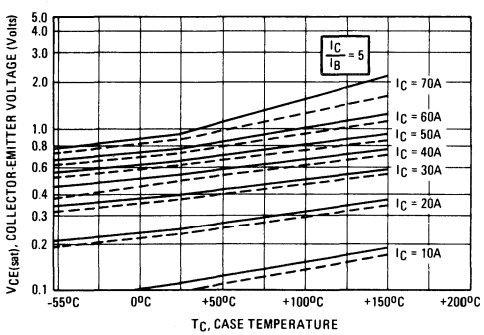
DC CURRENT GAIN



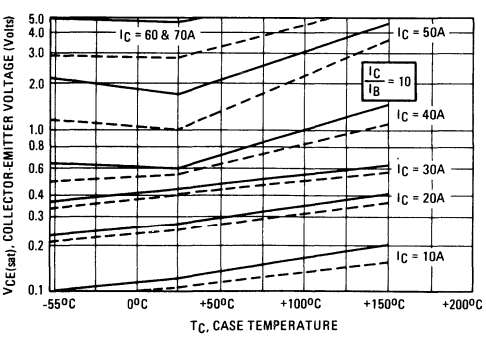
BASE-EMITTER SATURATION



COLLECTOR SATURATION



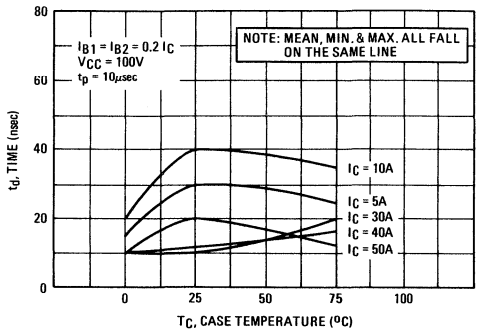
COLLECTOR SATURATION



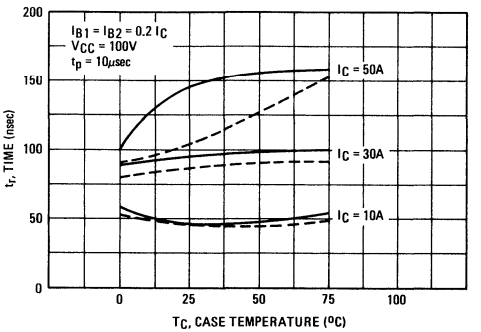
DOTTED LINES – MEDIAN
SOLID LINES – 90TH PERCENTILE

RESISTIVE SWITCHING

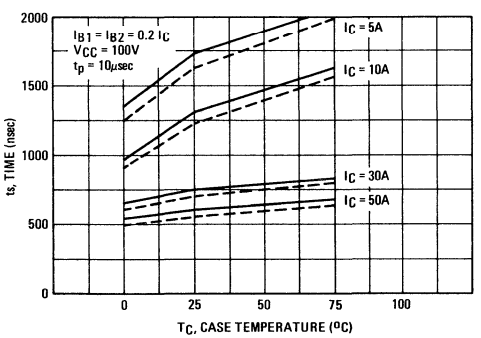
t_d, DELAY TIME



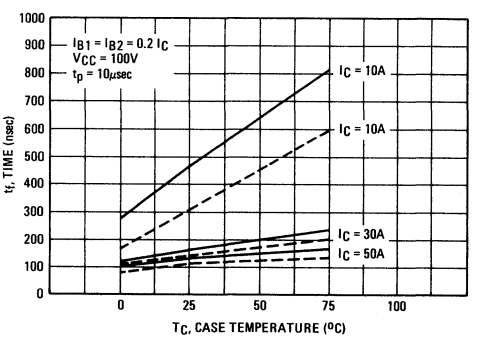
t_r, RISE TIME



t_s, STORAGE TIME

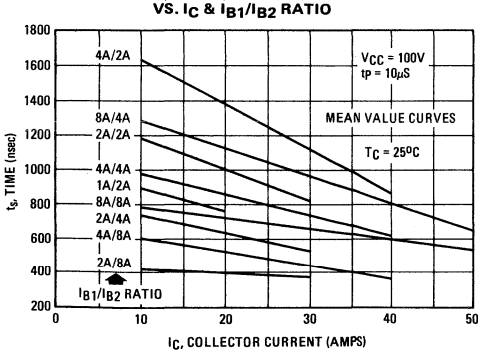


t_f, FALL TIME

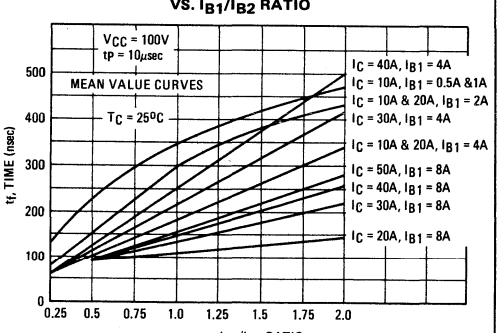


BASE DRIVE EFFECTS (RESISTIVE SWITCHING)

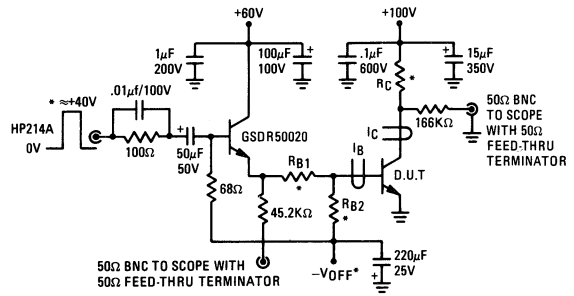
t_s, STORAGE TIME VS. I_C & I_{B1}/I_{B2} RATIO



t_f, FALL TIME VS. I_{B1}/I_{B2} RATIO

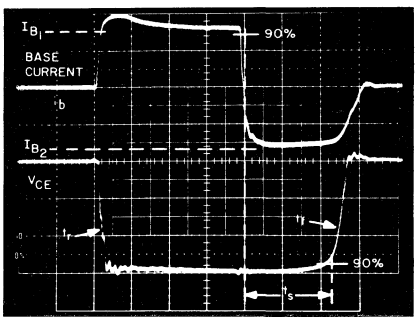


RESISTIVE SWITCHING CIRCUIT



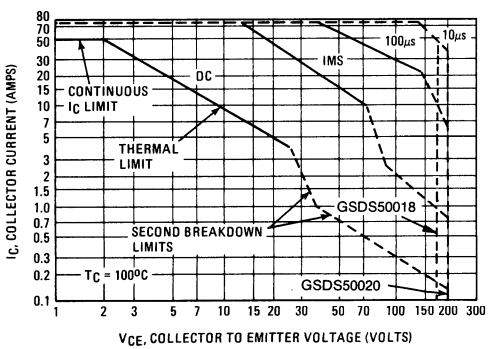
*(1) Select R_C for proper collector current @ 100V.
(2) R_{B1} & R_{B2} selected such that I_{B1} & I_{B2} are the desired values for an input pulse voltage of approximately 40V & $-V_{OFF}$ level of approximately 5V. I_B & I_C measured with TEK P6302 current probe & AM503 amplifier. Scope: TEK 7834 Storage Scope; 7B92A Time Base; 7A26 Dual Amplifier.

RESISTIVE SWITCHING WAVEFORM

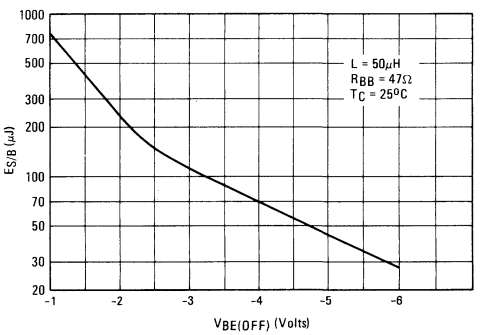


SAFE OPERATING AREA

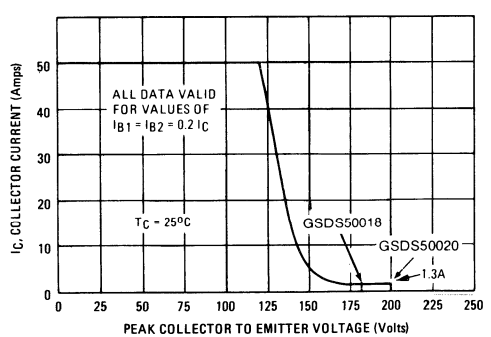
FORWARD BIASED SAFE OPERATING AREA



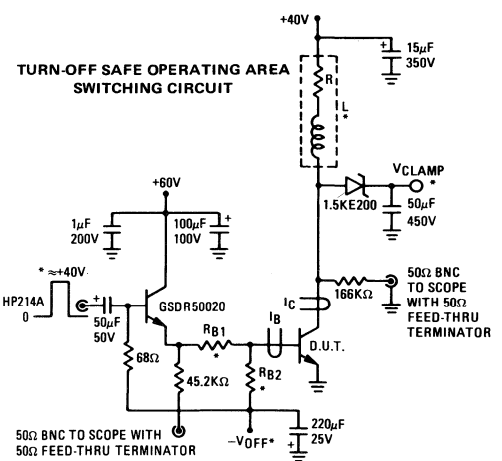
AVALANCHE ENERGY



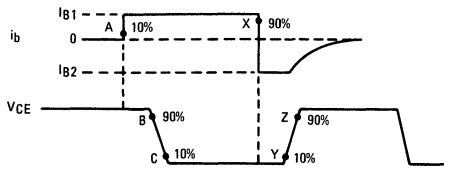
TURN-OFF SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA SWITCHING CIRCUIT

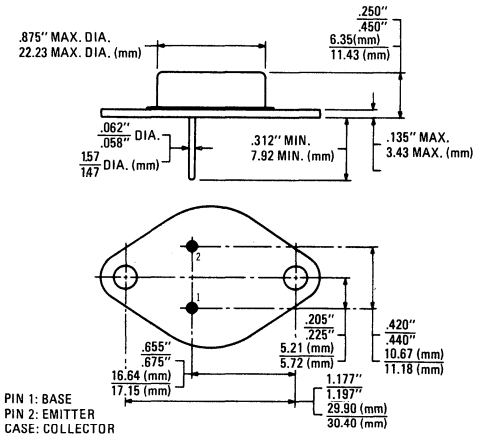


WAVEFORMS
RESISTIVE SWITCHING



$t_d = A - B$
$t_r = B - C$
$t_s = X - Y$
$t_f = Y - Z$

PACKAGE OUTLINE
TO-204AE



*Available as standard TO-3 with 0.040" pins. Contact factory for further information.

General Semiconductor Industries, Inc.

GSRU10030
GSRU10035
GSRU10040

HIGH POWER NPN *Switch Plus® III* TRANSISTORS

NPN
300, 350, 400V
10 AMP SWITCHING
t_f — 100ns TYPICAL

The GSRU series of NPN transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long-term reliability.

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

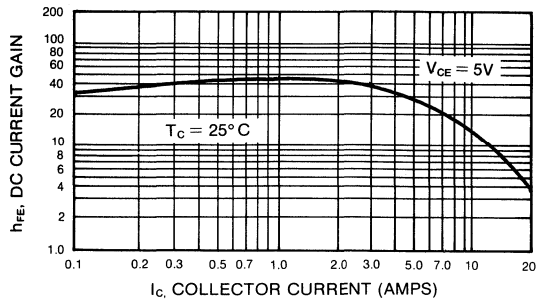
RATING	SYMBOL	GSRU10030	GSRU10035	GSRU10040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous	I_C	15	15	15	Amps
Peak	I_{CM}	20	20	20	Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Total Power Dissipation @ T_C=25°C	P_D	175	175	175	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.0	1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

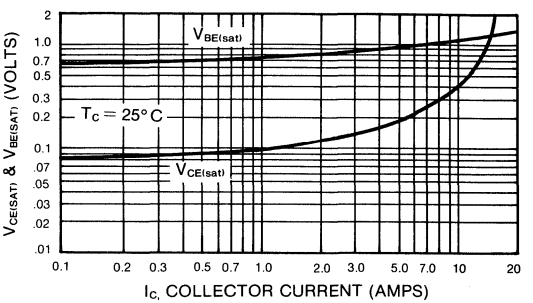
SYMBOL	CONDITIONS	GSRU10030		GSRU10035		GSRU10040		
		Min	Max	Min	Max	Min	Max	Unit
V_{CBO}	I_C = 1mA	400	—	450	—	500	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1mA	8.0	—	8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	—	500	—	500	—	500	μA
I_{EBO}	V_{EB} = 5V	—	100	—	100	—	100	μA
h_{FE}	V_{CE} = 5V, I_C= 10A†	10	—	10	—	10	—	—
$V_{CE(sat)}$	I_C = 10A, I_B = 2A†	—	1.0	—	1.0	—	1.0	Volts
$V_{BE(sat)}$	I_C = 10A, I_B = 2A†	—	1.5	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1A, f = 10Mhz	20	—	20	—	20	—	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	—	350	—	350	—	350	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load**	0.04	0.07	0.04	0.07	0.04	0.07	μs
t_r	V_{CC} = 250V, I_C = 10A R = 25Ω	0.10	0.35	0.10	0.35	0.10	0.35	μs
t_s	I_{B1} = I_{B2} = 2A V_{BB2} = 6V	1.50	2.50	1.50	2.50	1.50	2.50	μs
t_f	t_p = 50μs,	0.10	0.30	0.10	0.30	0.10	0.30	μs
t_s		1.70	2.50	1.70	2.50	1.70	2.50	μs
t_{rv}		0.20	0.35	0.20	0.35	0.20	0.35	μs
t_{fi}	**Inductive Load**	0.05	0.10	0.05	0.10	0.05	0.10	μs
t_c	V_{CC} = 22V, I_C = 10A, L = 100 μH	0.18	0.40	0.18	0.40	0.18	0.40	μs
t_s 100°C	I_{B1} = I_{B2} = 2A, V_{BB2} = 6V	2.00	3.00	2.00	3.00	2.00	3.00	μs
t_{rv} 100°C	V_{CLAMP} = 250V, t_p = 50μs	0.25	0.40	0.25	0.40	0.25	0.40	μs
t_{fi} 100°C		0.10	0.20	0.10	0.20	0.10	0.20	μs
t_c 100°C		0.30	0.60	0.30	0.60	0.30	0.60	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

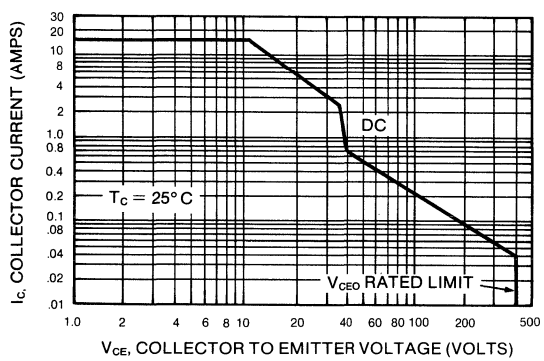
TYPICAL DC CURRENT GAIN



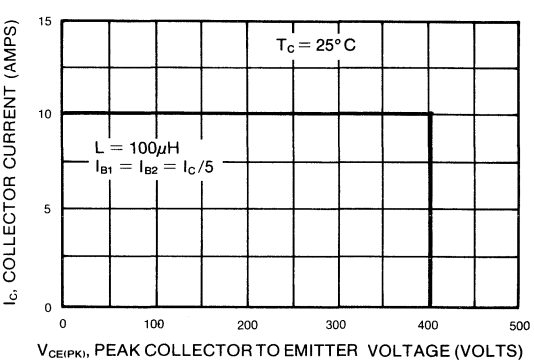
TYPICAL SATURATION VOLTAGE



FORWARD BIASED SAFE OPERATING AREA

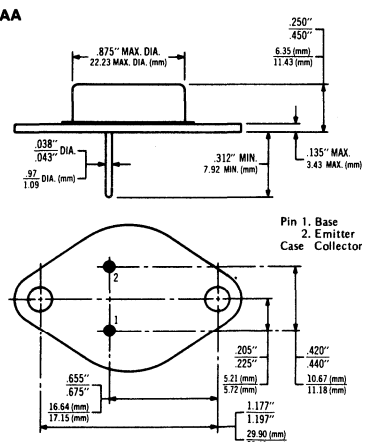


TURN-OFF SAFE OPERATING AREA

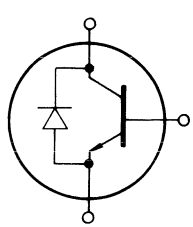


PACKAGE OUTLINE

TO-204AA



(FORMERLY TO-3)



Note:
The technology utilized to produce these devices results in an internal diode between the collector and emitter. In some cases this may eliminate the need for an external diode to clamp inductive loads. At 10A, t_{rr} = 750ns and V_F = 1.05V (typical).

General Semiconductor Industries, Inc.

GSRU14040

HIGH POWER NPN *Switch Plus®III* TRANSISTORS

The GSRU series of NPN silicon transistors is designed for high speed switching systems. The GSRU14040 features General Semiconductor Industries' $C^2R^®$ manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliability.

- **High Speed**
- **Rugged**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Switching Regulators**

TO-3

NPN

400V

V_{CEO}

20A

$I_{C\ (MAX.)}$

14A

SWITCHING

Switch Plus® III

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	GSRU14040	UNIT
V_{CBO}	Collector-Base Voltage	500	Volts
V_{CEO}	Collector-Emitter Voltage	400	Volts
V_{EBO}	Emitter-Base Voltage	8.0	Volts
I_C	Collector Current - Continuous	20	Amps
I_{CM}	Peak	30	Amps
I_B	Base Current -- Continuous	10	Amps
P_D	Total Power Dissipation @ T_C = 25°C	175	Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range	-65 to +200	°C

ELECTRICAL CHARACTERISTICS T_C = 25°C (Applies to all types unless otherwise noted.)

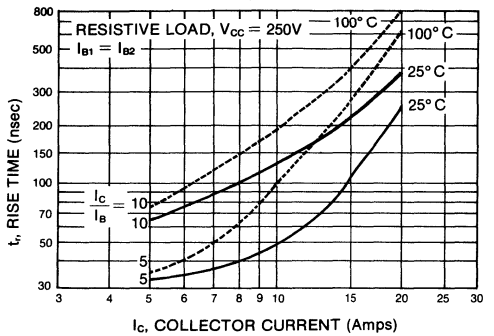
SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
OFF-STATE				
V_{CBO} V_{CES} V_{CEX}	I_C = 1.0mA V_{EB} = 1.5V (V_{CEX} Only)	500		Volts
V_{CEO}	I_C = 50mA	400		Volts
V_{EBO}	I_E =1.0mA	8.0		Volts
I_{CEX}	V_{CE} = 80% of Rated V_{CBO}, V_{EB} = 1.5V		10	µA
I_{EBO}	V_{EB} = 5.0V		10	µA
ON-STATE				
h_{FE}	V_{CE} = 5.0V, I_C = 14A	10		Volts
$V_{CE(sat)}$	I_C = 14A, I_B = 3.0A†		1.0	Volts
$V_{BE(sat)}$	I_C = 14A, I_B = 3.0A†		1.5	Volts
DYNAMIC				
f_T	V_{CE} = 10V, I_C = 1.0A, † f = 10MHz	15	50	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	200	500	pF
t_d	**Resistive**		0.03	µs
t_r	I_C = 14A, V_{CC} = 250V		0.35	µs
t_s	I_{B1} = I_{B2} = 3.0A		1.50	µs
t_f	t_p = 50µsec		0.12	µs
$t_{sd\ (tr)}$	V_{CC} = 40V		1.0	µs
t_{sv}	**Inductive**		1.8	µs
t_{rv}	I_C = 14A, V_{CLAMP} = 250V		0.12	µs
t_{fi}	I_{B1} = I_{B2} = 3.0A, L = 100µH		0.05	µs
t_c			0.18	µs
THERMAL				
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A		1.0	°C/W

† Pulse measurement conditions: Length = 300msec. Duty Cycle <2% (measured using separate current carrying and voltage sensing leads).

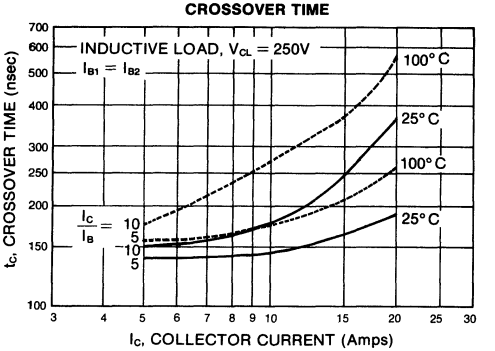
General Semiconductor Industries, Inc. • 2001 West Tenth Place, Tempe, AZ 85281 • (602) 968-3101 • FAX: (602) 966-6396

TYPICAL SWITCHING CHARACTERISTICS & RATINGS

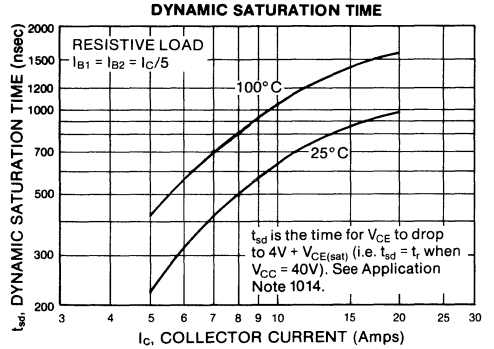
RISE TIME



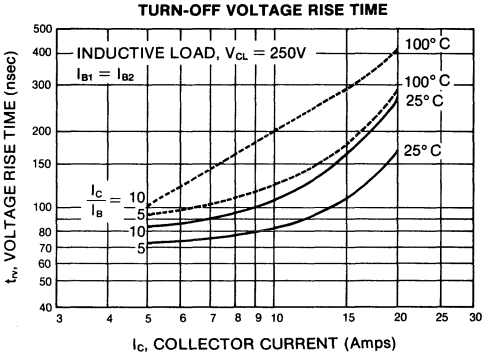
CROSSOVER TIME



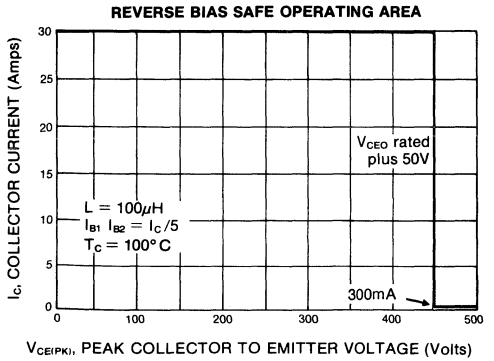
DYNAMIC SATURATION TIME



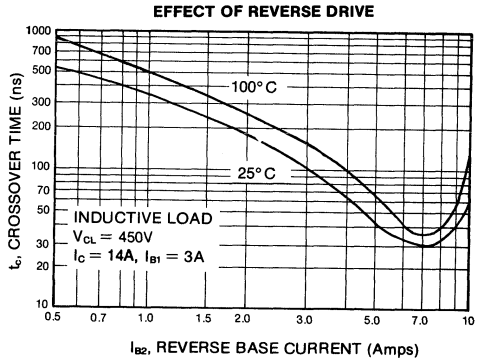
TURN-OFF VOLTAGE RISE TIME



REVERSE BIAS SAFE OPERATING AREA

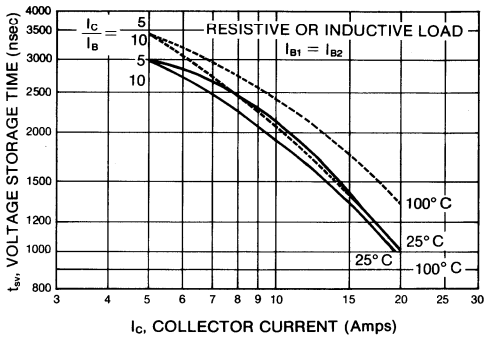


EFFECT OF REVERSE DRIVE

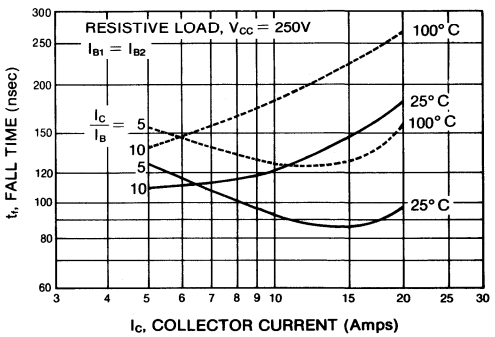


TURN-OFF CHARACTERISTICS

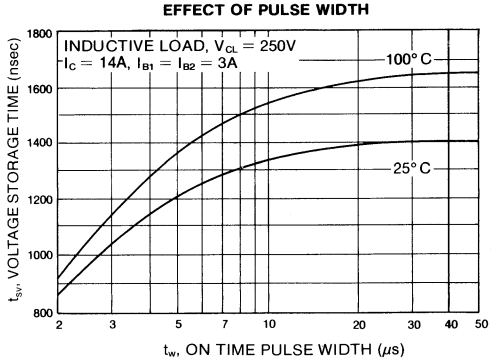
STORAGE TIME



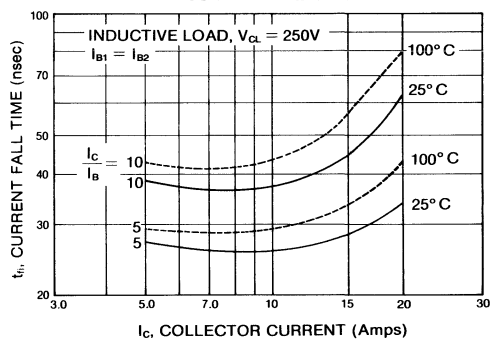
FALL TIME



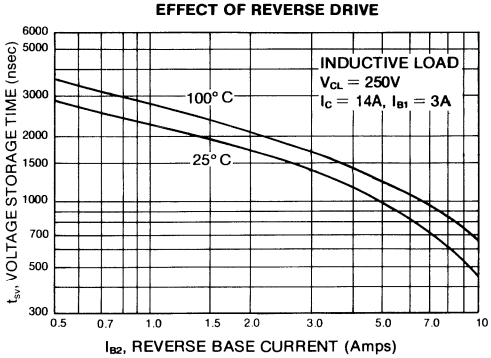
EFFECT OF PULSE WIDTH



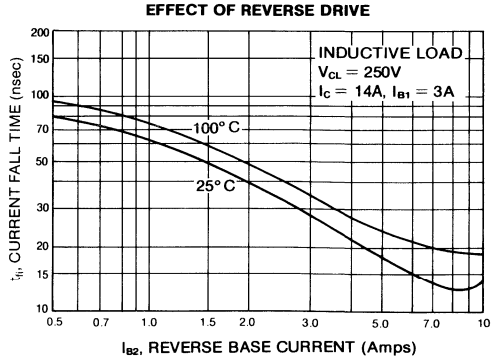
CURRENT FALL TIME



EFFECT OF REVERSE DRIVE

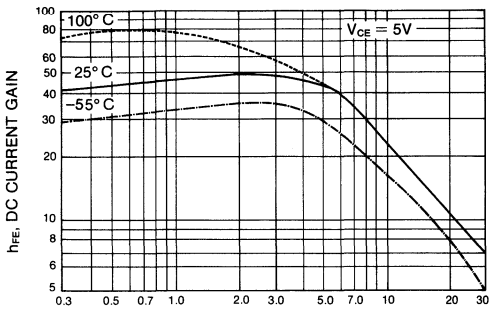


EFFECT OF REVERSE DRIVE

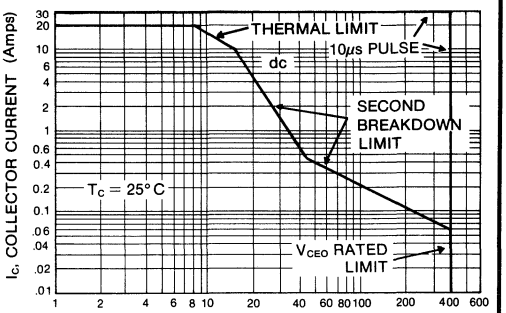


TYPICAL DC CHARACTERISTICS & RATINGS

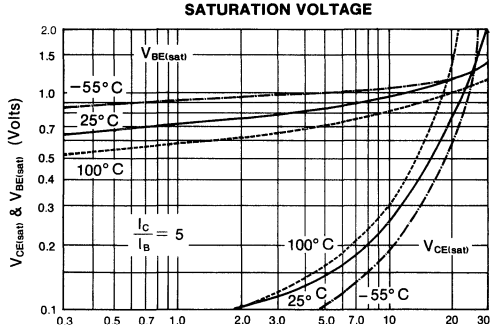
DC CURRENT GAIN



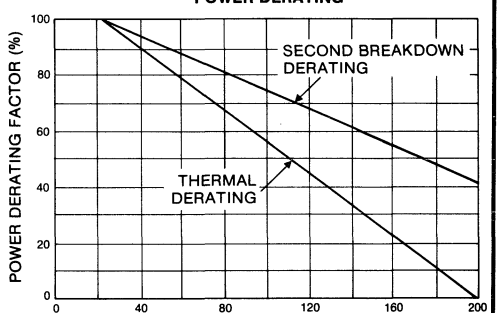
FORWARD BIASED SAFE OPERATING AREA



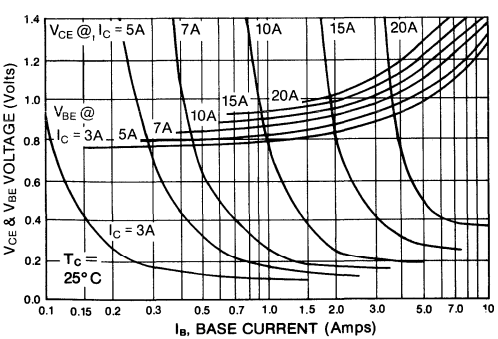
SATURATION VOLTAGE



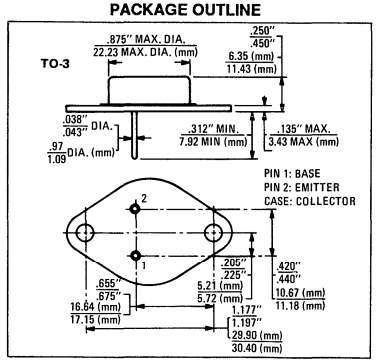
POWER DERATING



SATURATION REGION



PACKAGE OUTLINE



HIGH POWER NPN *Switch Plus®III* TRANSISTORS

"A" Suffix units have 100° C specifications guaranteed.

The GSRU series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process to provide surface stabilization for high voltage operation and to enhance long term reliability.

- **High Speed**
- **Rugged**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Switching Regulators**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

SYMBOL	DESCRIPTION	GSRU15030, A	GSRU15035, A	GSRU15040, A	UNIT
V_{CBO}	Collector-Base Voltage	400	450	500	Volts
V_{CEO}	Collector-Emitter Voltage	300	350	400	Volts
V_{EBO}	Emitter-Base Voltage		8.0		Volts
I_C	Collector Current—Continuous		20		Amps
I_{CM}	Peak		30		Amps
I_B	Base Current—Continuous		10		Amps
P_D	Total Power Dissipation @ T_C = 25°C		175		Watts
$T_{J(oper)}$ T_{stg}	Operating and Storage Junction Temperature Range		-65 to +200		°C

ELECTRICAL CHARACTERISTICS (Applies to all types unless otherwise noted.)

			T_C = 25°C		T_C = 100°C, A only		
SYMBOL	CONDITIONS	PART NO.	MIN.	MAX.	MIN.	MAX.	UNIT
OFF-STATE							
V_{CBO} V_{CES} V_{CEX}	I_C = 1.0mA V_{EB} = 1.5V (V_{CEX} Only)	GSRU15030, A GSRU15035, A GSRU15040, A	400 450 500				Volts
V_{CEO}	I_C = 50mA	GSRU15030, A GSRU15035, A GSRU15040, A	300 350 400				Volts
V_{EBO}	I_E = 1.0mA		8				Volts
I_{CEX}	V_{CE} = 80% of Rated V_{CBO}, V_{EB} = 1.5V			10		100	μA
I_{EBO}	V_{EB} = 5.0V			10			μA
ON-STATE							
h_{FE}	V_{CE} = 5.0V, I_C = 15A†		10				
$V_{CE(sat)}$	I_C = 15A, I_B = 3A†			1.0		1.0	Volts
$V_{BE(sat)}$	I_C = 15A, I_B = 3A†			1.5			Volts
DYNAMIC							
f_T	V_{CE} = 10V, I_C = 1A,† f = 10MHz		15	50			MHz
C_{obo}	V_{CB} = 10V, f = 1MHz		200	500			pF
t_d	**Resistive Load**			0.07			μs
t_r	I_C = 15A, V_{CC} = 250V			0.40			μs
t_s	I_{B1} = I_{B2} = 3A			2.20			μs
t_f	t_p = 50μsec			0.20			μs
t_{sd} (t_r)	V_{CC} = 40V			1.50		2.00	μs
t_{sv}	**Inductive Load**			2.40		3.00	μs
t_{rv}	I_C = 15A, V_{CLAMP} = 250V			0.35		0.40	μs
t_{fi}	I_{B1} = I_{B2} = 3A, L = 100μH			0.12		0.20	μs
t_c	t_p = 50 μs			0.40		0.60	μs
THERMAL							
$R_{\theta JC}$	V_{CE} = 10V, I_C = 10A			1.0			°C/W

†Pulse measurement conditions: Length = 300μsec, Duty Cycle = 2% (measured using separate current carrying and voltage sensing leads).

TO-204AA (TO-3)

NPN

400, 350, 300V V_{CEO}

20 A $I_{C(MAX.)}$

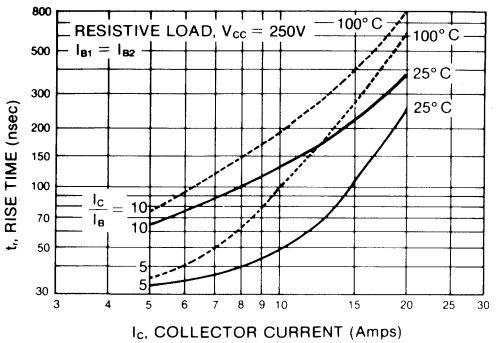
15 A SWITCHING

35ns t_c TYPICAL

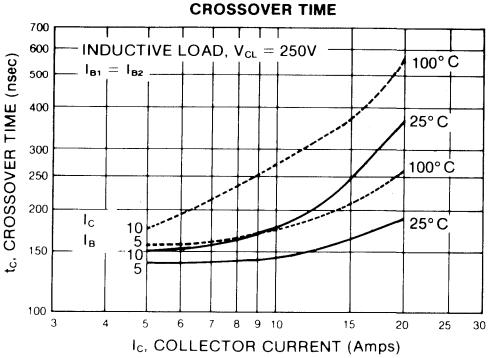
Switch Plus®III

TYPICAL SWITCHING CHARACTERISTICS & RATINGS

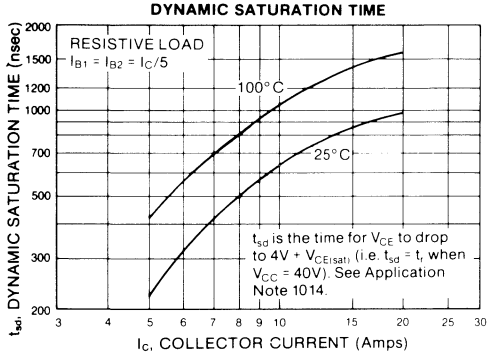
RISE TIME



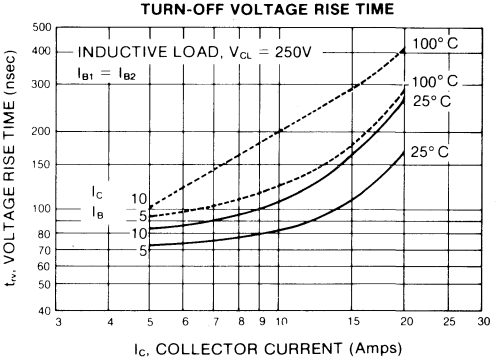
CROSSOVER TIME



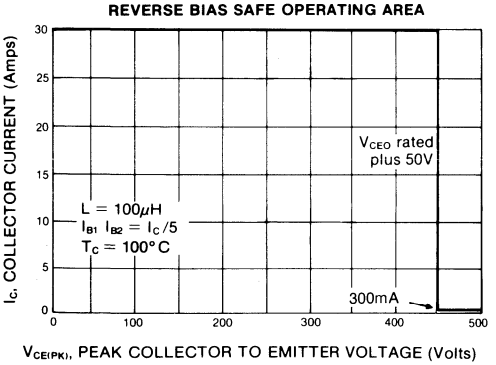
DYNAMIC SATURATION TIME



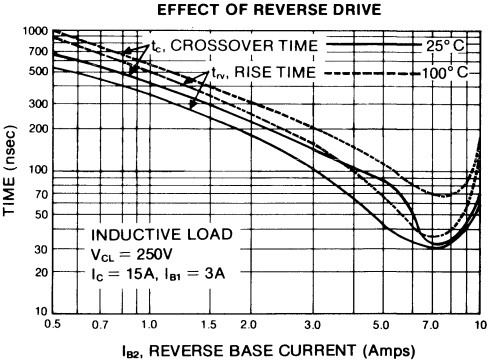
TURN-OFF VOLTAGE RISE TIME



REVERSE BIAS SAFE OPERATING AREA

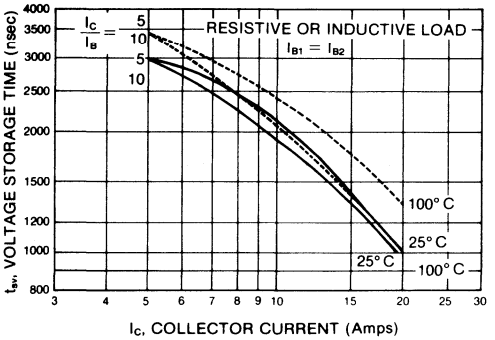


EFFECT OF REVERSE DRIVE

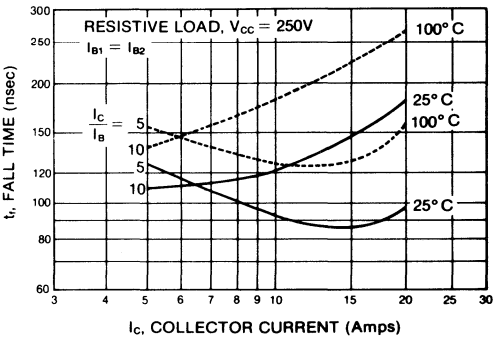


TURN-OFF CHARACTERISTICS

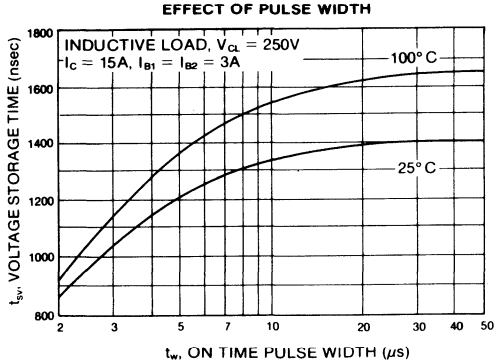
STORAGE TIME



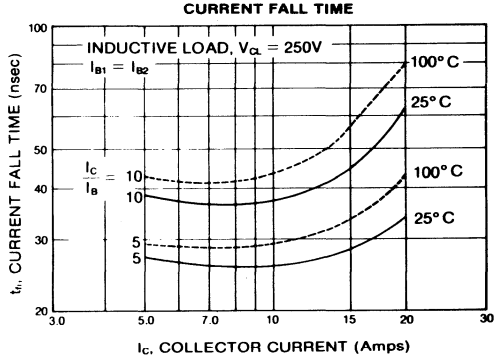
FALL TIME



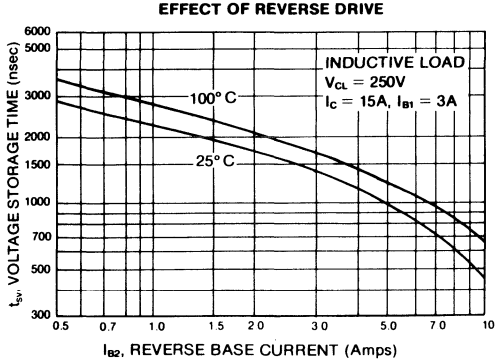
EFFECT OF PULSE WIDTH



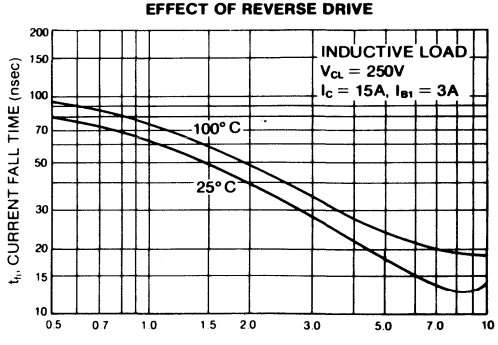
CURRENT FALL TIME



EFFECT OF REVERSE DRIVE

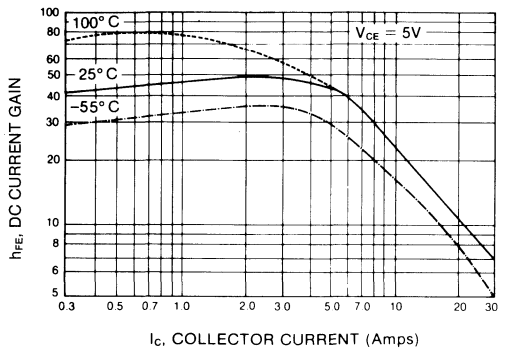


EFFECT OF REVERSE DRIVE

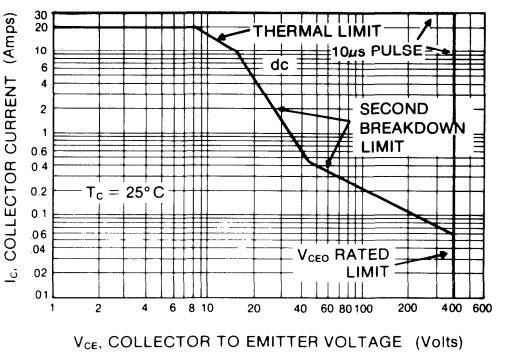


TYPICAL DC CHARACTERISTICS & RATINGS

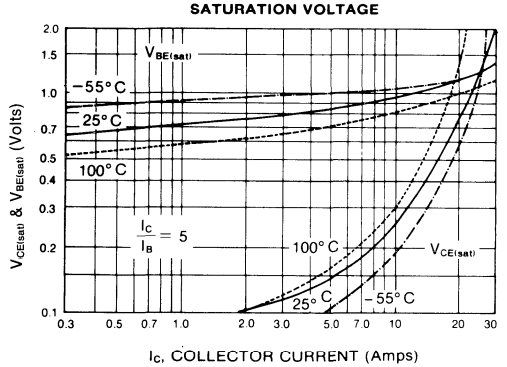
DC CURRENT GAIN



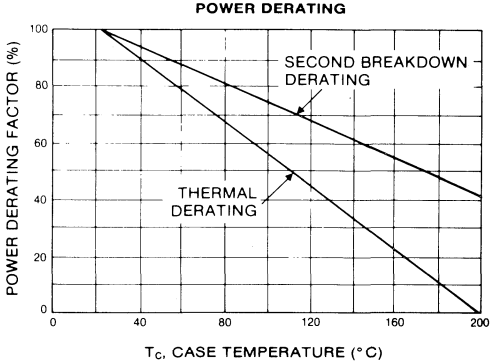
FORWARD BIASED SAFE OPERATING AREA



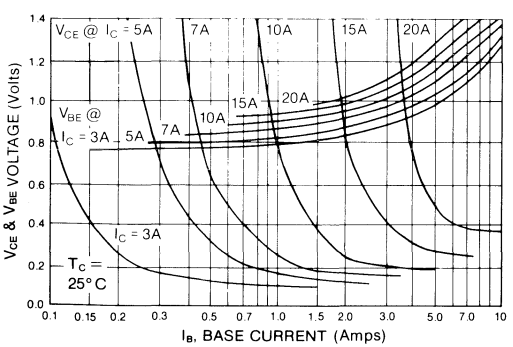
SATURATION VOLTAGE



POWER DERATING

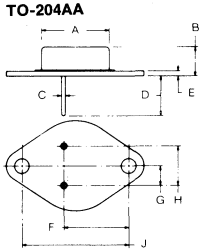


SATURATION REGION



PACKAGE OUTLINE

TO-204AA



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.875	—	22.23
B	.250	.450	6.35	11.43
C	.038	.043	.97	1.09
D	.312	—	7.92	—
E	—	.135	—	3.43
F	.655	.675	16.64	17.15
G	.205	.225	5.21	5.72
H	.420	.440	10.67	11.18
J	1.177	1.197	29.90	30.40

Pin 1 Base
2 Emitter
Case Collector

(FORMERLY TO-3)

General Semiconductor Industries, Inc.

GSRU20030
GSRU20035
GSRU20040

HIGH POWER NPN *Switch Plus® III* TRANSISTORS

The GSRU series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

NPN
300, 350, 400V
20 AMP SWITCHING
t_f — 100ns TYPICAL

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

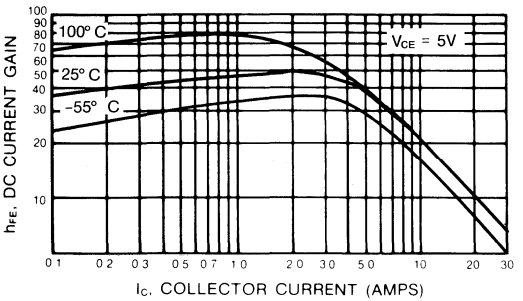
RATING	SYMBOL	GSRU20030	GSRU20035	GSRU20040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous Peak	I_C I_{CM}	25 30	25 30	25 30	Amps Amps
Base Current—Continuous	I_B	10	10	10	Amps
Total Power Dissipation @ T_C = 25° C	P_D	200	200	200	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	.875	.875	.875	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	−65 to +200	−65 to +200	−65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

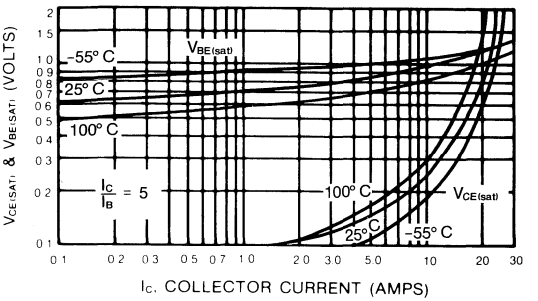
SYMBOL	CONDITIONS	GSRU20030		GSRU20035		GSRU20040		Unit
		Min	Max	Min	Max	Min	Max	
V_{CBO}	I_C = 1.0mA	400	—	450	—	500	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1.0mA	8.0	—	8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	—	100	—	100	—	100	μA
I_{EBO}	V_{EB} = 5.0V	—	10	—	10	—	10	μA
h_{FE}†	V_{CE} = 5.0V, I_C = 20A	8.0	—	8.0	—	8.0	—	—
$V_{CE(sat)}$†	I_C = 20A, I_B = 4.0A	—	1.5	—	1.5	—	1.5	Volts
$V_{BE(sat)}$†	I_C = 20A, I_B = 4.0A	—	1.6	—	1.6	—	1.6	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	20	—	20	—	20	—	MHz
C_{obo}	V_{CB} = 10V, f = 1.0MHz	—	500	—	500	—	500	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load** V_{CC} = 250V I_C = 20A, R = 12.5Ω $I_{B_1} = I_{B_2}$ = 4.0A t_p = 50μsec	0.05	0.07	0.05	0.07	0.05	0.07	μs
t_r		0.25	0.50	0.25	0.50	0.25	0.50	μs
t_s		2.00	2.50	2.00	2.50	2.00	2.50	μs
t_f		0.10	0.20	0.10	0.20	0.10	0.20	μs
t_s	**Inductive Load** V_{CLAMP} = 250V I_C = 20A, L = 100 μH $I_{B_1} = I_{B_2}$ = 4.0A t_p = 50μsec	1.70	2.40	1.70	2.40	1.70	2.40	μs
t_{rv}		0.20	0.35	0.20	0.35	0.20	0.35	μs
t_{fi}		0.07	0.12	0.07	0.12	0.08	0.12	μs
t_c		0.30	0.50	0.30	0.50	0.30	0.50	μs
t_s 100° C		2.00	3.00	2.00	3.00	2.00	3.00	μs
t_{rv} 100° C		0.25	0.40	0.25	0.40	0.25	0.40	μs
t_{fi} 100° C		0.10	0.20	0.10	0.20	0.10	0.20	μs
t_c 100° C		0.40	0.70	0.40	0.70	0.40	0.70	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

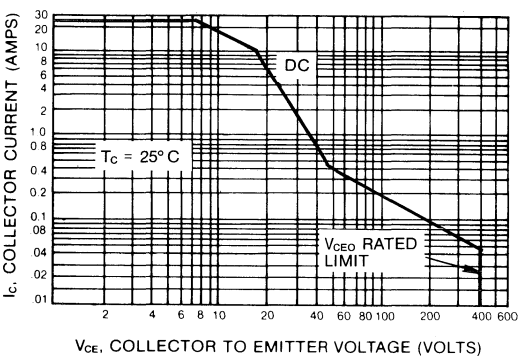
TYPICAL DC CURRENT GAIN



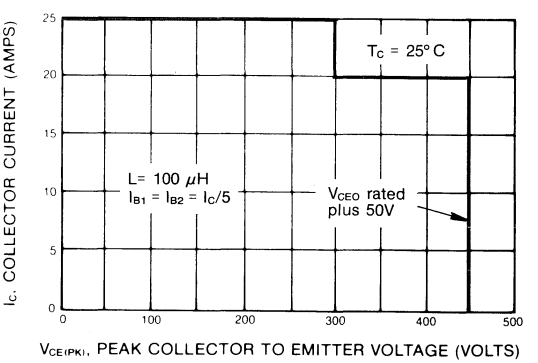
TYPICAL SATURATION VOLTAGE



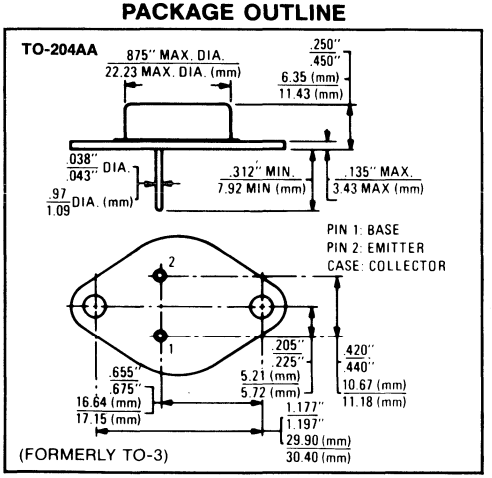
FORWARD BIASED SAFE OPERATING AREA

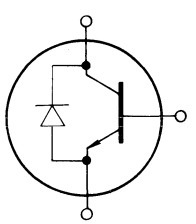


TURN-OFF SAFE OPERATING AREA



PACKAGE OUTLINE





Note:

The technology utilized to produce these devices results in an internal diode between the collector and emitter. In some cases this may eliminate the need for an external diode to clamp inductive loads. At 20 A, t_{rr} = 600 ns and V_F = 1.25V (typical).

General Semiconductor Industries, Inc.

GSTU4030 GSTU4035 GSTU4040

HIGH POWER NPN *Switch Plus*® TRANSISTORS

NPN
300, 350, 400V
4 AMP SWITCHING
t_f — 250ns TYPICAL

TO-204AA (TO-3)

The GSTU series is a NPN silicon transistor designed for high speed switching systems. This unique series utilizes General Semiconductor Industries' C2R process which describes a manufacturing technology that provides surface stabilization for high voltage operation and enhances long term reliability.

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

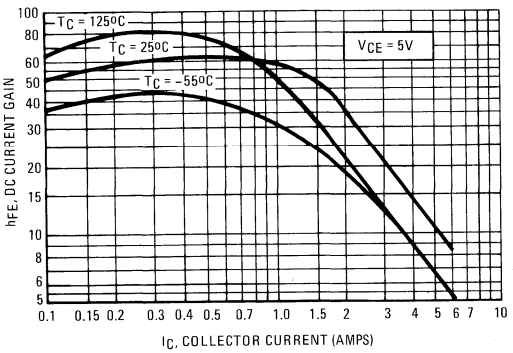
RATING	SYMBOL	GSTU4030	GSTU4035	GSTU4040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	7.0	7.0	7.0	Volts
Collector Current-Continuous Peak	I_C I_{CM}	6 10	6 10	6 10	Amps Amps
Base Current-Continuous	I_B	4	4	4	Amps
Total Power Dissipation @ T_C = 25°C	P_D	125	125	125	Watts
$\Theta_{j\text{-}c}$, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	1.4	1.4	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	−65 to +200 −65 to +200	−65 to +200 −65 to +200	−65 to +200 −65 to +200	°C °C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

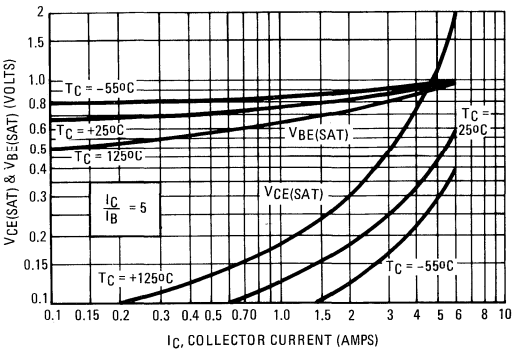
SYMBOL	CONDITIONS	GSTU4030 Min	GSTU4030 Max	GSTU4035 Min	GSTU4035 Max	GSTU4040 Min	GSTU4040 Max	Unit
V_{CBO}	I_C = 1.0mA	400	–	450	–	500	–	Volts
V_{CEO}	I_C = 50mA	300	–	350	–	400	–	Volts
V_{EBO}	I_E = 1.0mA	7.0	–	7.0	–	7.0	–	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	–	500	–	500	–	500	μA
I_{EBO}	V_{EB} = 5.0V	–	100	–	100	–	100	μA
h_{FE}*	V_{CE} = 5.0V, I_C = 4A†	10	–	10	–	10	–	–
$V_{CE(sat)}$*	I_C = 4A, I_B = 0.8A †	–	1.0	–	1.0	–	1.0	Volts
$V_{BE(sat)}$*	I_C = 4A, I_B = 0.8A†	–	1.2	–	1.2	–	1.2	Volts
f_T	V_{CE} = 10V, I_C = 1.0A	10	–	10	–	10	–	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	–	150	–	150	–	150	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d**	**Resistive Load**	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r**	V_{CC} = 200V, I_C = 6A,	0.18	0.25	0.18	0.25	0.18	0.25	μs
t_s	$I_{B1} = I_{B2}$ = 1.2A, t_p = 50μs,	1.70	2.20	1.70	2.20	1.70	2.20	μs
t_f	Duty Cycle < 2.0%,	0.25	0.40	0.25	0.40	0.25	0.40	μs
t_s	**Inductive Load**	2.00	2.50	2.00	2.50	2.00	2.50	μs
t_{rv}	V_{CLAMP} = 200V,	0.20	0.30	0.20	0.30	0.20	0.30	μs
t_{fi}	I_C = 6A, L = 100μH,	0.15	0.30	0.15	0.30	0.15	0.30	μs
t_c	$I_{B1} = I_{B2}$ = 1.2A, t_p = 50μsec,	0.35	0.60	0.35	0.60	0.35	0.60	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

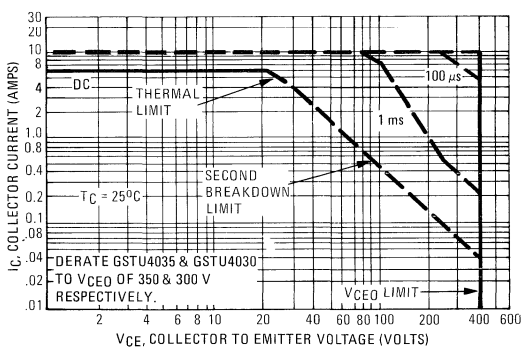
TYPICAL DC CURRENT GAIN



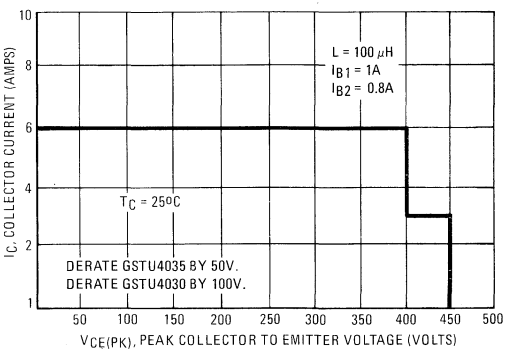
TYPICAL SATURATION VOLTAGE



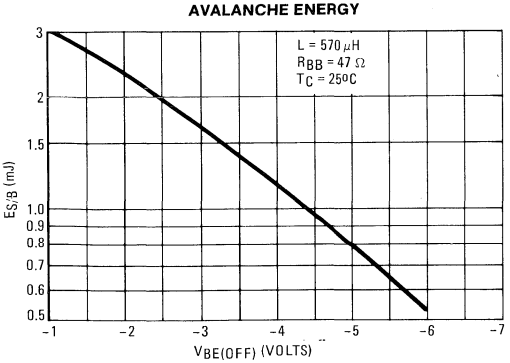
FORWARD BIASED SAFE OPERATING AREA



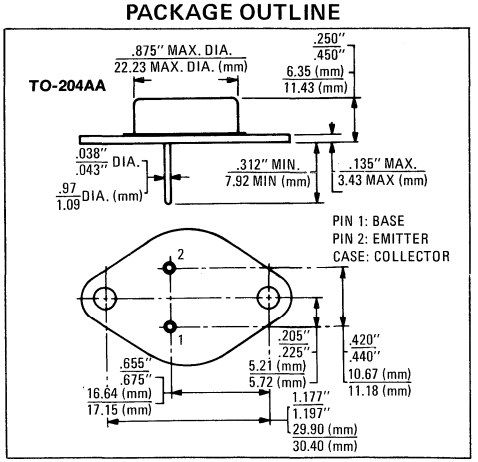
TURN-OFF SAFE OPERATING AREA



AVALANCHE ENERGY



PACKAGE OUTLINE



General Semiconductor Industries, Inc.

GSTU6030
GSTU6035
GSTU6040

HIGH POWER NPN *Switch Plus*™ TRANSISTORS

NPN
300, 350, 400V
6 AMP SWITCHING
t_f — 250ns TYPICAL

TO-204AA (TO-3)

The GSTU series is a NPN silicon transistor designed for high speed switching systems. This unique series utilizes General Semiconductor Industries' C²R process which describes a manufacturing technology that provides surface stabilization for high voltage operation and enhances long term reliability.

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

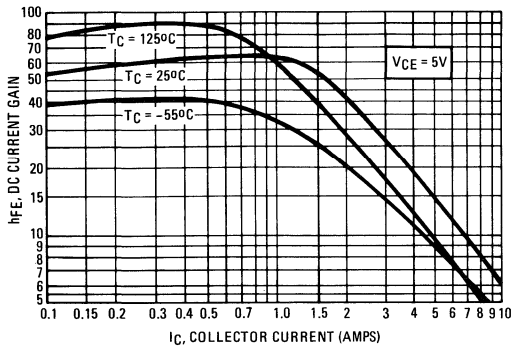
RATING	SYMBOL	GSTU6030	GSTU6035	GSTU6040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	7.0	7.0	7.0	Volts
Collector Current-Continuous Peak	I_C I_{CM}	9 15	9 15	9 15	Amps Amps
Base Current-Continuous	I_B	5	5	5	Amps
Total Power Dissipation @ T_C = 25°C	P_D	125	125	125	Watts
$\Theta_{j\text{-}c}$, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	1.4	1.4	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	−65 to +200 −65 to +200	−65 to +200 −65 to +200	−65 to +200 −65 to +200	°C °C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

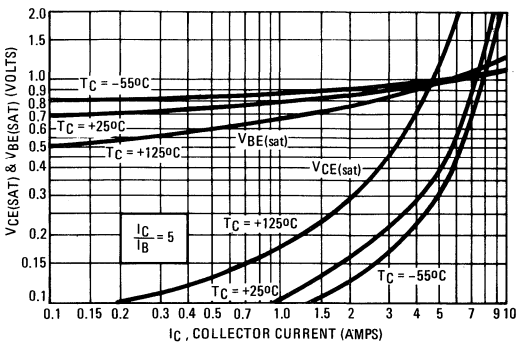
SYMBOL	CONDITIONS	GSTU6030 Min	GSTU6030 Max	GSTU6035 Min	GSTU6035 Max	GSTU6040 Min	GSTU6040 Max	Unit
V_{CBO}	I_C = 1.0mA	400	–	450	–	500	–	Volts
V_{CEO}	I_C = 50mA	300	–	350	–	400	–	Volts
V_{EBO}	I_E = 1.0mA	7.0	–	7.0	–	7.0	–	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	–	500	–	500	–	500	μA
I_{EBO}	V_{EB} = 5.0V	–	100	–	100	–	100	μA
h_{FE}	V_{CE} = 5.0V, I_C = 6A†	10	–	10	–	10	–	–
$V_{CE(sat)}$	I_C = 6A, I_B = 1.2A †	–	1.0	–	1.0	–	1.0	Volts
$V_{BE(sat)}$	I_C = 6A, I_B = 1.2A†	–	1.2	–	1.2	–	1.2	Volts
f_T	V_{CE} = 10V, I_C = 1.0A	15	–	15	–	15	–	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	–	150	–	150	–	150	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load**	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r	V_{CC} = 200V, I_c = 6A,	0.18	0.25	0.18	0.25	0.18	0.25	μs
t_s	I_{B1} = I_{B2} = 1.2A, t_p = 50μs,	1.70	2.20	1.70	2.20	1.70	2.20	μs
t_f	Duty Cycle < 2.0%,	0.25	0.40	0.25	0.40	0.25	0.40	μs
t_s	**Inductive Load**	1.70	2.20	1.70	2.00	1.70	2.00	μs
t_{rv}	V_{CLAMP} = 200V,	0.20	0.30	0.20	0.30	0.20	0.30	μs
t_{fi}	I_C = 6A, L = 100μH,	0.15	0.30	0.15	0.30	0.15	0.30	μs
t_c	I_{B1} = I_{B2} = 1.2A, t_p = 50μsec,	0.35	0.60	0.35	0.60	0.35	0.60	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

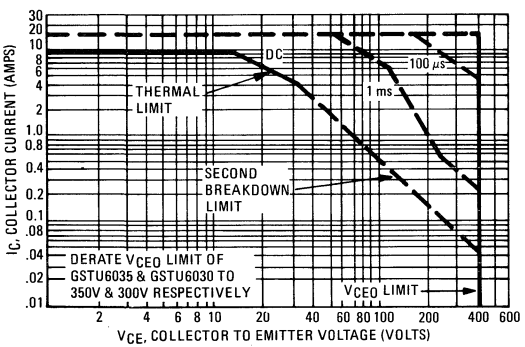
TYPICAL DC CURRENT GAIN



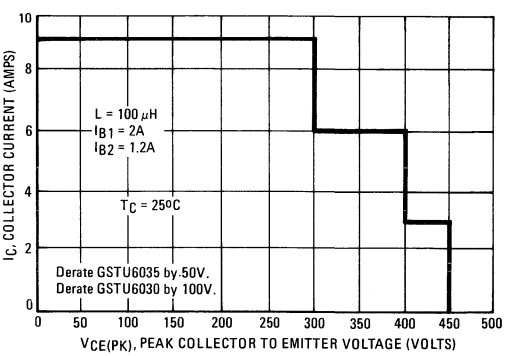
TYPICAL SATURATION VOLTAGES



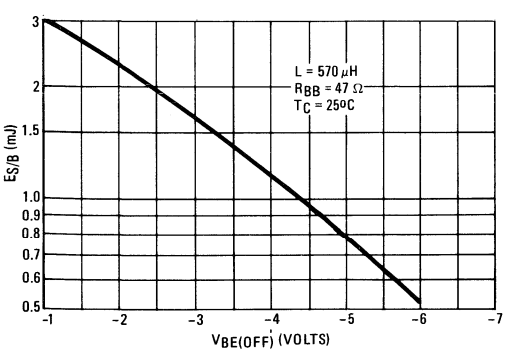
FORWARD BIASED SAFE OPERATING AREA



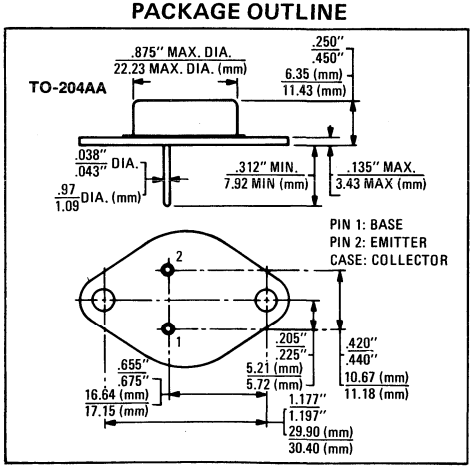
TURN-OFF SAFE OPERATING AREA



AVALANCHE ENERGY



PACKAGE OUTLINE



General Semiconductor Industries, Inc.

GSTU8030
GSTU8035
GSTU8040

HIGH POWER NPN *Switch Plus*® TRANSISTORS

NPN
300, 350, 400V
8 AMP SWITCHING
t_f — 280ns TYPICAL

The GSTU8040 series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

3

NPN SWITCHING TRANSISTORS

MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

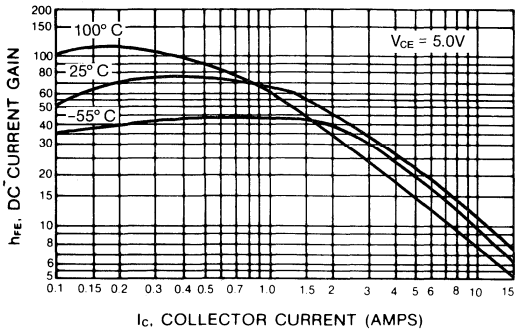
RATING	SYMBOL	GSTU8030	GSTU8035	GSTU8040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous	I_C	12	12	12	Amps
Peak	I_{CM}	16	16	16	Amps
Base Current—Continuous	I_B	4.0	4.0	4.0	Amps
Total Power Dissipation @ T_C = 25° C	P_D	175	175	175	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.0	1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

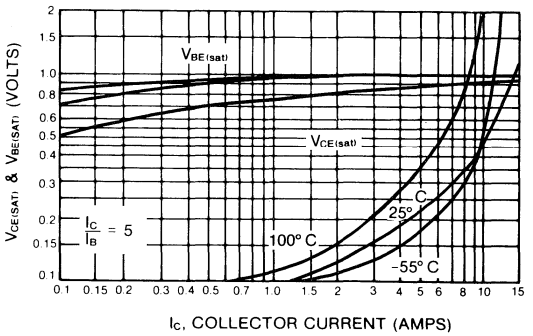
SYMBOL	CONDITIONS	GSTU8030		GSTU8035		GSTU8040		Unit
		Min	Max	Min	Max	Min	Max	
V_{CBO}	I_C = 1.0mA	400	—	450	—	500	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1.0mA	8.0	—	8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	—	100	—	100	—	100	μA
I_{EBO}	V_{EB} = 5.0V	—	10	—	10	—	10	μA
h_{FE}†	V_{CE} = 5.0V, I_C = 8.0A	10	—	10	—	10	—	—
$V_{CE(sat)}$†	I_C = 8.0A, I_B = 1.6A	—	1.0	—	1.0	—	1.0	Volts
$V_{BE(sat)}$†	I_C = 8.0A, I_B = 1.6A	—	1.5	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	25	—	25	—	25	—	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	—	300	—	300	—	300	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load** V_{CC} = 250V I_C = 8.0A, R = 31Ω $I_{B_1} = I_{B_2}$ = 1.6A t_p = 50 μsec	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r		0.15	0.25	0.15	0.25	0.15	0.25	μs
t_s		1.60	2.50	1.60	2.50	1.60	2.50	μs
t_f		0.28	0.40	0.28	0.40	0.28	0.40	μs
t_s	**Inductive Load** V_{CLAMP} = 250V I_C = 10A, L = 100 μH $I_{B_1} = I_{B_2}$ = 2.0A t_p = 50 μsec	1.80	2.50	1.80	2.50	1.80	2.50	μs
t_{rv}		0.27	0.40	0.27	0.40	0.27	0.40	μs
t_{fi}		0.13	0.25	0.13	0.25	0.13	0.25	μs
t_c		0.35	0.50	0.35	0.50	0.35	0.50	μs
t_s 100° C		2.70	4.00	2.70	4.00	2.70	4.00	μs
t_{rv} 100° C		0.40	0.60	0.40	0.60	0.40	0.60	μs
t_{fi} 100° C		0.15	0.30	0.15	0.30	0.15	0.30	μs
t_c 100° C		0.60	1.00	0.60	1.00	0.60	1.00	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

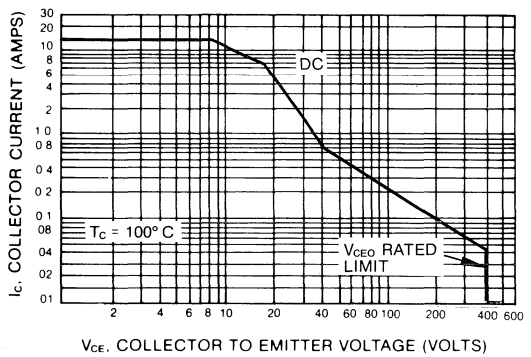
TYPICAL DC CURRENT GAIN



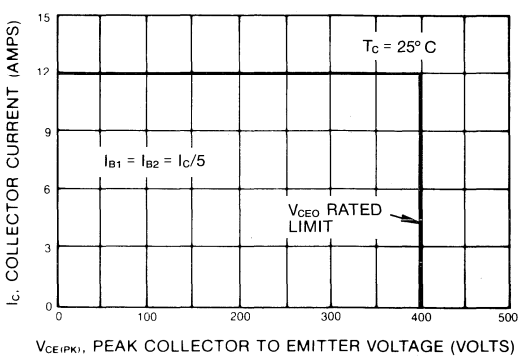
TYPICAL SATURATION VOLTAGE



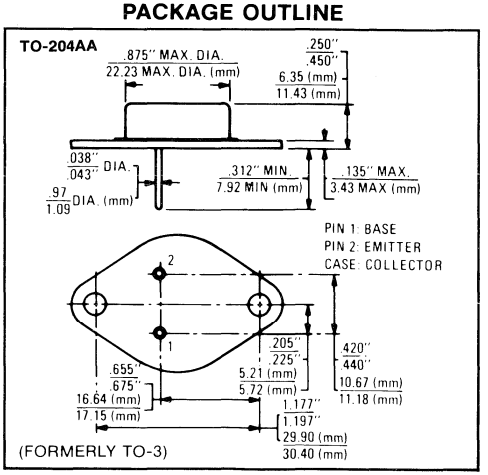
FORWARD BIASED SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA



PACKAGE OUTLINE



General Semiconductor Industries, Inc.

GSTU10030
GSTU10035
GSTU10040

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The GSTU10040 series of NPN silicon transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long term reliability.

NPN
300, 350, 400V
10 AMP SWITCHING
t_f — 280ns TYPICAL

TO-204AA (TO-3)

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Off-line Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

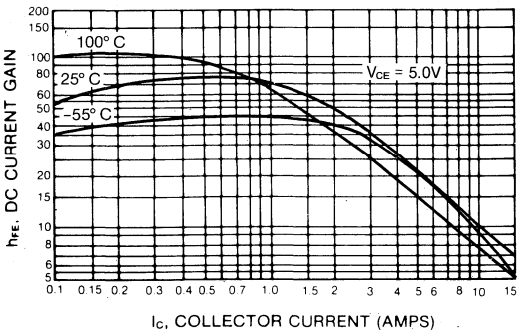
RATING	SYMBOL	GSTU10030	GSTU10035	GSTU10040	UNIT
Collector-Base Voltage	V_{CBO}	400	450	500	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	8.0	Volts
Collector Current—Continuous Peak	I_C I_{CM}	15 20	15 20	15 20	Amps Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Total Power Dissipation @ T_C = 25° C	P_D	175	175	175	Watts
Θ_{j-c}, Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.0	1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

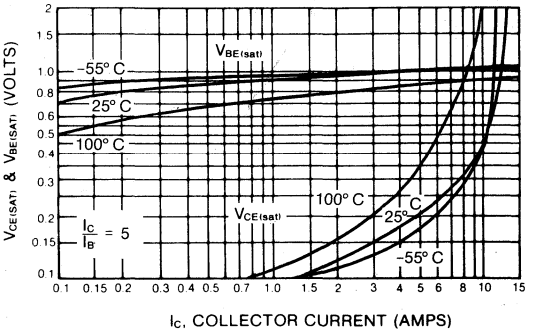
SYMBOL	CONDITIONS	GSTU10030 Min	GSTU10030 Max	GSTU10035 Min	GSTU10035 Max	GSTU10040 Min	GSTU10040 Max	Unit
V_{CBO}	I_C = 1.0mA	400	—	450	—	500	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1.0mA	8.0	—	8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	—	100	—	100	—	100	μA
I_{EBO}	V_{EB} = 5.0V	—	10	—	10	—	10	μA
h_{FE}†	V_{CE} = 5.0V, I_C = 10A	10	—	10	—	10	—	—
$V_{CE(sat)}$†	I_C = 10A, I_B = 2.0A	—	1.0	—	1.0	—	1.0	Volts
$V_{BE(sat)}$†	I_C = 10A, I_B = 2.0A	—	1.5	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, f = 10MHz	25	—	25	—	25	—	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	—	300	—	300	—	300	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load** V_{CC} = 250V I_C = 10A, R = 25Ω $I_{B_1} = I_{B_2}$ = 2.0A t_p = 50 μsec	0.04	0.05	0.04	0.05	0.04	0.05	μs
t_r		0.15	0.25	0.15	0.25	0.15	0.25	μs
t_s		1.50	2.50	1.50	2.50	1.50	2.50	μs
t_f		0.28	0.40	0.28	0.40	0.28	0.40	μs
t_s	**Inductive Load** V_{CLAMP} = 250V I_C = 10A, L = 100 μH $I_{B_1} = I_{B_2}$ = 2.0A t_p = 50 μsec	1.70	2.50	1.70	2.50	1.70	2.50	μs
t_{rv}		0.27	0.40	0.27	0.40	0.27	0.40	μs
t_{fi}		0.13	0.25	0.13	0.25	0.13	0.25	μs
t_c		0.35	0.50	0.35	0.50	0.35	0.50	μs
t_s 100° C		2.70	4.00	2.70	4.00	2.70	4.00	μs
t_{rv} 100° C		0.40	0.60	0.40	0.60	0.40	0.60	μs
t_{fi} 100° C		0.15	0.30	0.15	0.30	0.15	0.30	μs
t_c 100° C		0.60	1.00	0.60	1.00	0.60	1.00	μs

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

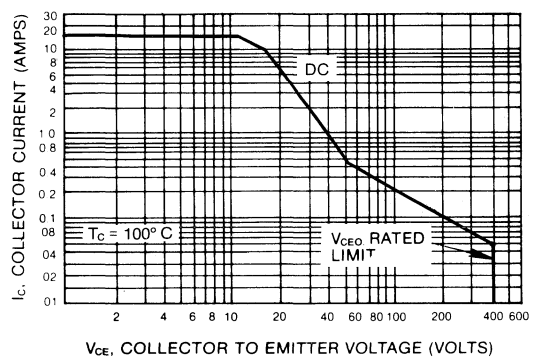
TYPICAL DC CURRENT GAIN



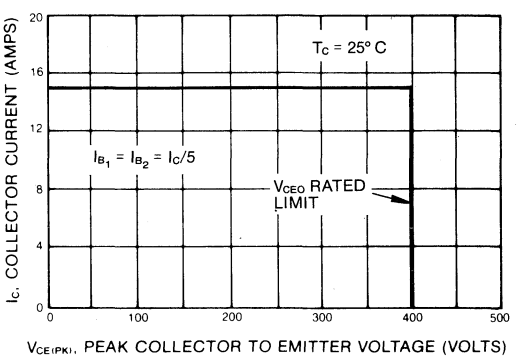
TYPICAL SATURATION VOLTAGE



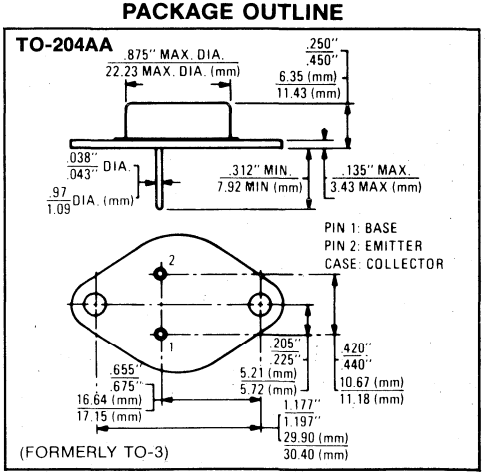
FORWARD BIASED SAFE OPERATING AREA



TURN-OFF SAFE OPERATING AREA



PACKAGE OUTLINE



General Semiconductor Industries, Inc.

GSTU15018
GSTU15020

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The GSTU series of NPN transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long-term reliability.

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

NPN
180, 200, V
15 AMP SWITCHING
t_f — 200ns TYPICAL

TO-204AA (TO-3)

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

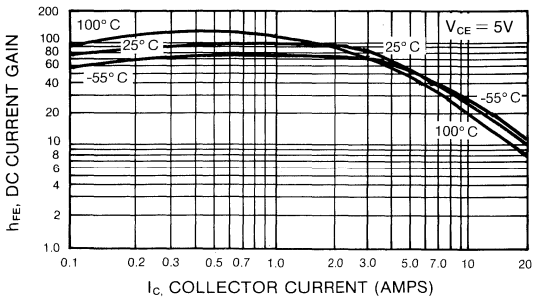
RATING	SYMBOL	GSTU15018	GSTU15020	UNIT
Collector-Base Voltage	V_{CBO}	250	300	Volts
Collector-Emitter Voltage	V_{CEO}	180	200	Volts
Emitter-Base Voltage	V_{EBO}	8.0	8.0	Volts
Collector Current—Continuous	I_C	20	20	Amps
Peak	I_{CM}	25	25	Amps
Base Current—Continuous	I_B	5.0	5.0	Amps
Total Power Dissipation @ T_C=25°C	P_D	140	140	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.25	1.25	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

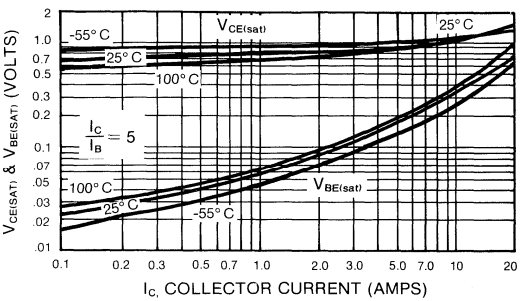
SYMBOL	CONDITIONS	GSTU15018 Min	GSTU15018 Max	GSTU15020 Min	GSTU15020 Max	Unit
V_{CBO}	I_C = 1mA	300	—	350	—	Volts
V_{CEO}	I_c = 50mA	180	—	200	—	Volts
V_{EBO}	I_E = 1mA	8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}	—	100	—	100	μA
I_{EBO}	V_{EB} = 5V	—	100	—	100	μA
h_{FE}	V_{CE} = 5V, I_C = 15A†	10	—	10	—	—
$V_{CE(sat)}$	I_C = 15A, I_B = 3A†	—	0.8	—	0.8	Volts
$V_{BE(sat)}$	I_C = 15A, I_B = 3A†	—	1.5	—	1.5	Volts
f_T	V_{CE} = 10V, I_C = 1A, f = 10MHz	25	—	25	—	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	—	200	—	200	pF
SWITCHING		**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load**	0.04	0.05	0.04	0.05	μs
t_r	V_{CC} = 125V, I_C = 15A, R = 8.3Ω	0.40	0.60	0.40	0.60	μs
t_s	I_{B1} = I_{B2} = 3A, V_{BB2} = 6V	0.70	1.20	0.70	1.20	μs
t_f	t_p = 50μs,	0.20	0.30	0.20	0.30	μs
t_s		0.60	1.40	0.60	1.40	μs
t_{rv}	**Inductive Load**	0.10	0.25	0.10	0.25	μs
t_{fi}		0.10	0.30	0.10	0.30	μs
t_c	V_{CC} = 30V, I_C = 15A, L = 100μH	0.20	0.50	0.20	0.50	μs
t_s 100°C	I_{B1} = I_{B2} = 3A, V_{BB2} = 6V	0.80	1.60	0.80	1.60	μs
t_{rv} 100°C	V_{CLAMP} = 125V, t_p = 50μs	0.15	0.20	0.15	0.20	μs
t_{fi} 100°C		0.15	0.30	0.15	0.30	μs
t_c 100°C		0.30	0.50	0.30	0.50	μs

† Pulse Conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

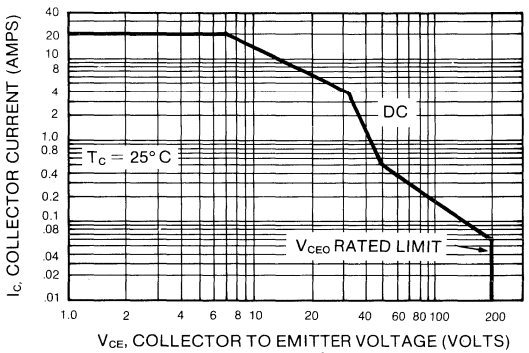
TYPICAL DC CURRENT GAIN



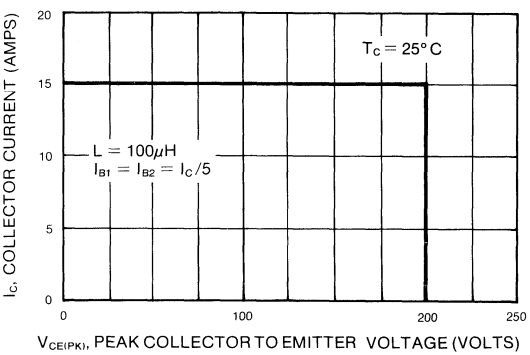
TYPICAL SATURATION VOLTAGE



FORWARD BIASED SAFE OPERATING AREA

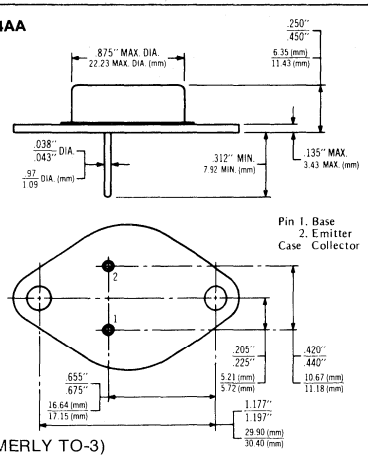


TURN-OFF SAFE OPERATING AREA



PACKAGE OUTLINE

TO-204AA



(FORMERLY TO-3)

General Semiconductor Industries, Inc.

GSTU30018
GSTU30020

HIGH POWER NPN *Switch Plus*® TRANSISTORS

The GSTU series of NPN transistors is designed for high speed switching systems. This unique series features General Semiconductor Industries' C²R® manufacturing process which provides surface stabilization for high voltage operation and enhances long-term reliability.

- **High Speed**
- **Rugged**
- **Cost Effective**
- **Power Supplies**
- **Switching Amplifiers**
- **Inverters/Converters**
- **Motor Speed Control Circuits**
- **Switching Regulators**
- **Solenoid & Relay Drivers**

NPN
180, 200, V
30 AMP SWITCHING
t_f — 150ns TYPICAL

TO-204AA (TO-3)

3

NPN SWITCHING TRANSISTORS

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

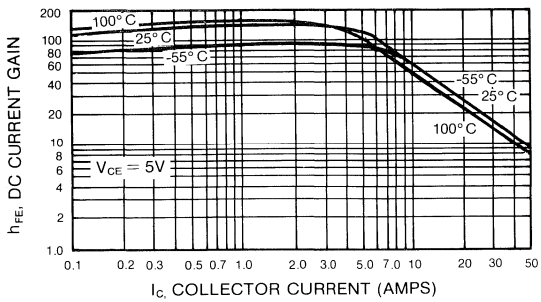
RATING	SYMBOL		GSTU30018	GSTU30020	UNIT
Collector-Base Voltage	V_{CBO}		250	300	Volts
Collector-Emitter Voltage	V_{CEO}		180	200	Volts
Emitter-Base Voltage	V_{EBO}		8.0	8.0	Volts
Collector Current—Continuous	I_C		30	30	Amps
Peak	I_{CM}		50	50	Amps
Base Current—Continuous	I_B		10	10	Amps
Total Power Dissipation @ T_C=25°C	P_D		175	175	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$		1.0	1.0	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}		-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

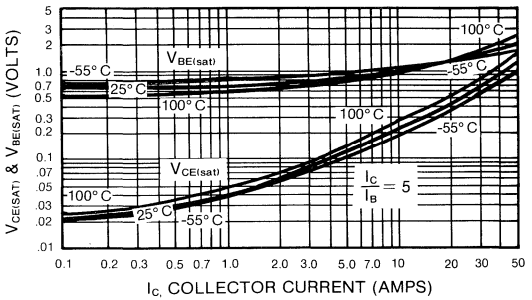
SYMBOL	CONDITIONS		GSTU30018 Min	GSTU30018 Max	GSTU30020 Min	GSTU30020 Max	Unit
V_{CBO}	I_C = 1mA		250	—	300	—	Volts
V_{CEO}	I_C = 50mA		180	—	200	—	Volts
V_{EBO}	I_E = 1mA		8.0	—	8.0	—	Volts
I_{CBO}	V_{CB} = 80% of Rated V_{CBO}		—	500	—	500	μA
I_{EBO}	V_{EB} = 5V		—	100	—	100	μA
h_{FE}	V_{CE} = 5V, I_C = 30A†		10	—	10	—	—
$V_{CE(sat)}$	I_C = 30A, I_B = 6A†		—	1.0	—	1.0	Volts
$V_{BE(sat)}$	I_C = 30A, I_B = 6A†		—	2.0	—	2.0	Volts
f_T	V_{CE} = 10V, I_C = 1A, f = 10Mhz		20	—	20	—	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz		—	350	—	350	pF
SWITCHING			**Typ**	**Max**	**Typ**	**Max**	**Unit**
t_d	**Resistive Load**		0.04	0.05	0.04	0.05	μs
t_r	V_{CC} = 125V, I_C = 30A R = 4.2Ω		0.30	0.60	0.30	0.60	μs
t_s	I_{B1} = I_{B2} = 6A V_{BB2} = 6V		0.75	1.40	0.75	1.40	μs
t_f	t_p = 50μs,		0.15	0.30	0.15	0.30	μs
t_s			0.70	1.10	0.70	1.10	μs
t_{rv}			0.10	0.20	0.10	0.20	μs
t_{fi}	**Inductive Load**		0.10	0.30	0.10	0.30	μs
t_c	V_{CC} = 60V, I_C = 30A, L = 100 μH		0.20	0.50	0.20	0.50	μs
t_s 100°C	I_{B1} = I_{B2} = 6A, V_{BB2} = 6V		1.00	1.60	1.00	1.60	μs
t_{rv} 100°C	V_{CLAMP} = 125V, t_p = 50μs		0.15	0.30	0.15	0.30	μs
t_{fi} 100°C			0.15	0.40	0.15	0.40	μs
t_c 100°C			0.30	0.70	0.30	0.70	μs

† Pulse Conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

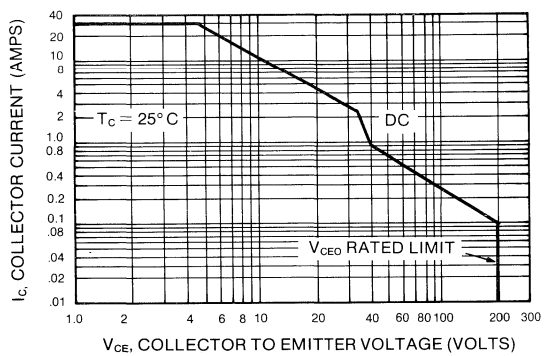
TYPICAL DC CURRENT GAIN



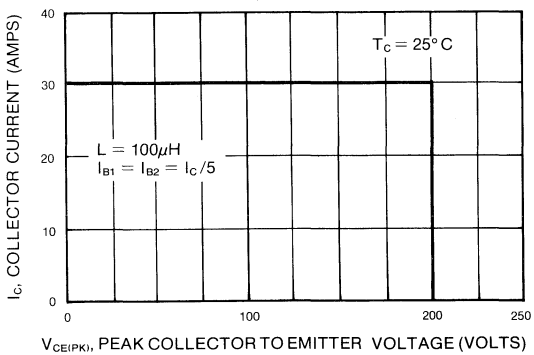
TYPICAL SATURATION VOLTAGE



FORWARD BIASED SAFE OPERATING AREA

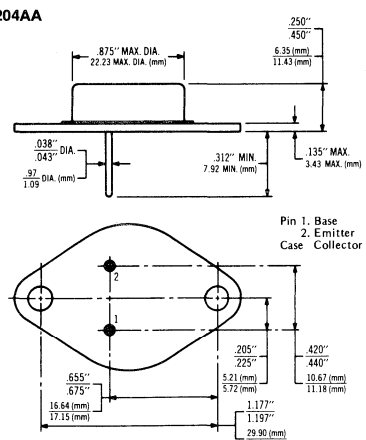


TURN-OFF SAFE OPERATING AREA



PACKAGE OUTLINE

TO-204AA



(FORMERLY TO-3)

General Semiconductor Industries, Inc.

NPN XGS7001 XGS7002

SILICON NPN TRANSISTORS

These double diffused, epitaxial collector devices are oxide passivated. They are designed for use in switching and many amplifier applications. The latest technologies are used to provide optimum performance and the highest degree of reliability.

NPN
30, 60V
1.5 AMP SWITCHING

TO-39

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

RATING	SYMBOL		XGS7001	XGS7002	UNIT
Collector-Base Voltage	V_{CBO}		50	70	Volts
Collector—Emitter Voltage	V_{CEO}		30	60	Volts
Emitter-Base Voltage	V_{EBO}		5.0	5.0	Volts
Collector Current—Continuous	I_C		3.0	3.0	Amps
Base Current—Continuous	I_B		1.0	1.0	Amps
Total Power Dissipation @T_C = 25°C	P_D^*		5.0	5.0	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$		35	35	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}		-65 to +200	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

SYMBOL	CONDITIONS		XGS7001 Min	XGS7001 Max	XGS7002 Min	XGS7002 Max	Unit
V_{CBO}	I_C = 100μA		50	—	70	—	Volts
V_{CEO}	I_C = 10mA		30	—	60	—	Volts
V_{EBO}	I_E = 10μA		5.0	—	5.0	—	Volts
I_{CBO}	V_{CB} = 30V		—	10	—	—	μA
I_{CBO}	V_{CB} = 40V		—	—	—	10	μA
h_{FE}†	V_{CE} = 2.0V, I_C = 2.0A		20	—	15	—	
$V_{CE(sat)}$†	I_C = 1.0A, I_B = 0.1A		—	1.0	—	1.0	Volts
$V_{BE(sat)}$†	I_C = 1.0A, I_B = 0.1A		—	1.5	—	1.5	Volts
$\|h_{FE}\|$	V_{CE} = 5.0V, I_C = 0.1A, f = 20MHz		6.0	—	6.0	—	
C_{ob}	V_{CB} = 10V, I_C = 0, f = 1.0MHz		—	40	—	40	pF
SWITCHING							
t_{on}	**Resistive Load**		—	40	—	40	ns
t_{off}	V_{CC} = 30V		—	100	—	100	ns
	I_C = 1.5A						
	$I_{B1} = I_{B2}$ = 150mA						
	t_P = 10μs						

† Pulse conditions: Width = 300μs; Duty Cycle ≤ 2% (measured using Kelvin connections).

General Semiconductor Industries, Inc.

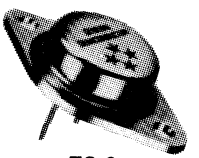
10 Amp NPN
300, 350, 400V
XGSR10030, 35, 40
XGSR10030-I, 35-I, 40-I

C²R® HIGH SPEED/HIGH POWER SWITCHING TRANSISTORS

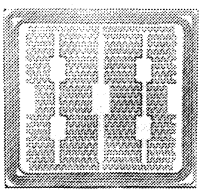
The XGSR series is an NPN double diffused epitaxial transistor designed for high speed switching systems. This unique series utilizes General Semiconductor Industries' C²R technology that provides surface stabilization for high voltage operation and enhances long term reliability. Another design feature is the use of an interdigitated emitter providing a periphery greater than 7.0 inches (18 cm) which improves both the gain characteristics and current handling capability.

These transistors have been specifically designed and engineered for high speed/high voltage switching applications where the designer is concerned with optimizing power conversion efficiency.

The XGSR series is also available in Isolated collector versions for reduction of conducted and radiated EMI.



TO-3



C²R®

FEATURES:
- **High Voltage**
- **High Gain**
- **High Current**
- **Low Saturation Voltages**
- **Fast Switching**
- **Low Leakage Current**
- **Available in TO-3 and TO-3 Isolated Packages**

APPLICATIONS:
- **High Speed Switching**
- **Power Conversion**
- **Converters**
- **Inverters**
- **Class D Amplifiers**
- **Class C Amplifiers**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

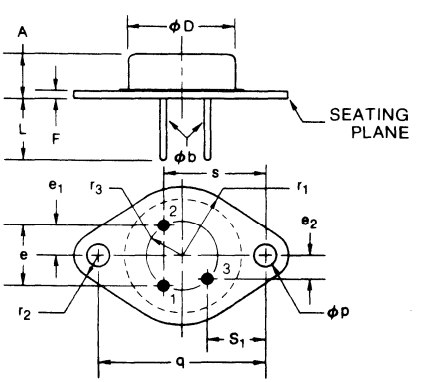
RATING	SYMBOL	XGSR10030 XGSR10030-I	XGSR10035 XGSR10035-I	XGSR10040 XGSR10040-I	UNIT
Collector-Base Voltage	V_{CBO}	350	400	450	Volts
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Emitter-Base Voltage	V_{EBO}	7.0	7.0	7.0	Volts
Collector Current—Continuous —Peak	I_C I_{CM}	15 20	15 20	15 20	Amps Amps
Base Current—Continuous	I_B	5.0	5.0	5.0	Amps
Emitter Current—Continuous —Peak	I_E I_{EM}	20 30	20 30	20 30	Amps Amps
Total Power Dissipation at T_C = 100°C	P_D	100	100	100	Watts
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.75	0.75	0.75	°C/W
Operating and Storage Junction Temperature Range	$T_{J(oper)}$ T_{stg}	-65 to +175 -65 to +200	-65 to +175 -65 to +200	-65 to +175 -65 to +200	°C °C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

		XGSR10030 XGSR10030-I		XGSR10035 XGSR10035-I		XGSR10040 XGSR10040-I		
SYMBOL	CONDITIONS	Min	Max	Min	Max	Min	Max	UNIT
V_{CBO}	I_C = 1.0mA	350	—	400	—	450	—	Volts
V_{CEO}	I_C = 50mA	300	—	350	—	400	—	Volts
V_{EBO}	I_E = 1.0mA	7.0	—	7.0	—	7.0	—	Volts
$V_{CEX(SUS)}$	I_C = 50mA, V_{BE} = 1.5V	350	—	400	—	450	—	Volts
$V_{CER(SUS)}$	I_C = 50mA, R = 47Ω	325	—	375	—	425	—	Volts
I_{CBO}	V_{CB} = 80% V_{CB} Rated	—	500	—	500	—	500	μA
I_{EBO}	V_{EB} = 5.0V	—	100	—	100	—	100	μA
I_{CEO}	V_{CE} = 80% V_{CE} Rated	—	1.0	—	1.0	—	1.0	mA
I_{CEX}	V_{CE} = V_{CEO} Rated, V_{BE} = -1.5V, T_J = 150° C	—	3.0	—	3.0	—	3.0	mA
h_{FE}	V_{CE} = 5.0V, I_C = 10A†	10	—	10	—	10	—	
$V_{CE(sat)}$	I_C = 10A, I_B = 2.0A†	—	0.8	—	0.8	—	0.8	Volts
$V_{BE(sat)}$	I_C = 10A, I_B = 2.0A†	—	1.3	—	1.3	—	1.3	Volts
f_T	V_{CE} = 10V, I_C = 1.0A, 10MHz	25	75	25	75	25	75	MHz
C_{obo}	V_{CB} = 10V, f = 1MHz	100	350	100	350	100	350	pF
t_d	V_{CC} = 200V, I_C = 10A, I_{B1} = I_{B2} = 2.0A, t_p = 10μs, Duty Cycle < 2%, Resistive	—	0.05	—	0.05	—	0.05	μsec
t_r		—	0.2	—	0.2	—	0.2	μsec
t_s		—	1.5	—	1.5	—	1.5	μsec
t_f		—	0.5	—	0.5	—	0.5	μsec

† Pulse measurement conditions: Length = 300μsec, Duty Cycle < 2%(measured using separate current carrying and voltage sensing leads).

F-30
(3 Terminal TO-3)
Isolated Collector



SYMBOL	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	6.35	11.43	0.250	0.450	
ϕb	0.97	1.09	0.038	0.043	3 leads
ϕD		22.23		0.875	
e	10.67	11.18	0.420	0.440	
e_1	5.21	5.72	0.205	0.225	
F		3.43		0.135	
L	7.92		0.312		3 leads
ϕp	3.84	4.09	0.151	0.161	
q	29.90	30.40	1.177	1.197	
r_1		13.34		0.525	
r_2		4.78		0.188	
s	16.64	17.15	0.700	0.730	
S_1	10.03	10.29	0.395	0.405	
e_2	3.68	4.19	0.145	0.165	
r_3	6.30	6.40	0.248	0.252	

PIN DESCRIPTION:
1. BASE
2. EMITTER
3. COLLECTOR

SECTION 4

APPLICATION NOTES

TYPICAL TRANSZORB TVS APPLICATIONS

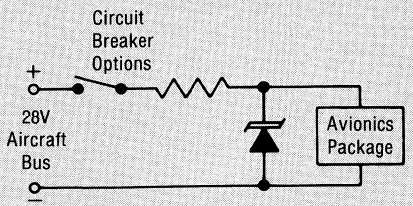


Figure 1—28V D.C. Supply Protection

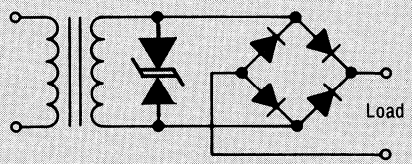


Figure 2—115V A.C. Supply Protection

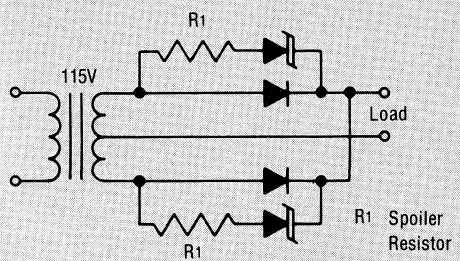


Figure 3—Breakdown Voltage Rectifier Protection

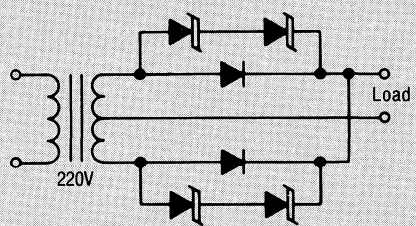


Figure 4—Breakdown Voltage Rectifier Protection*

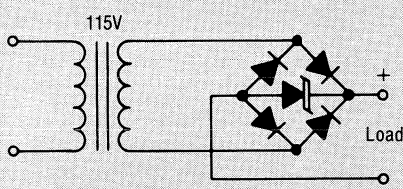


Figure 5—115V A.C. Supply Protection

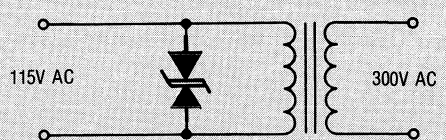


Figure 6—Circuit Protection from Overvoltage Supply Power

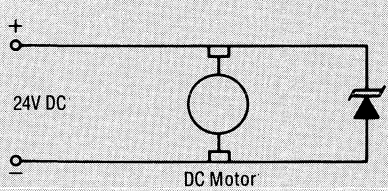


Figure 7—EMI Limiting

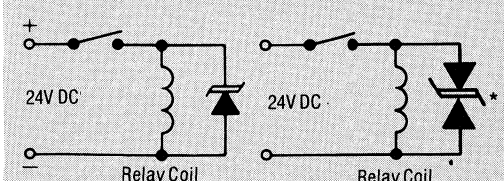


Figure 8—Relay and Contactor Transient Limiting

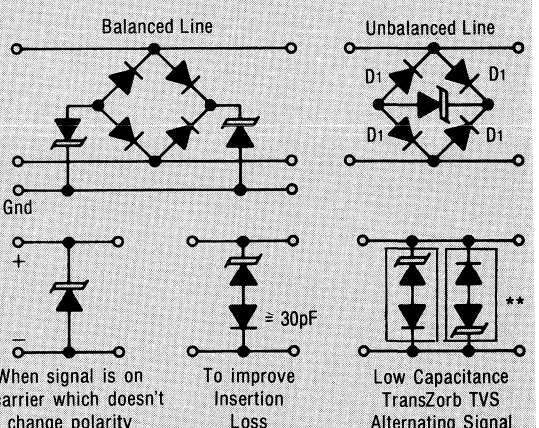
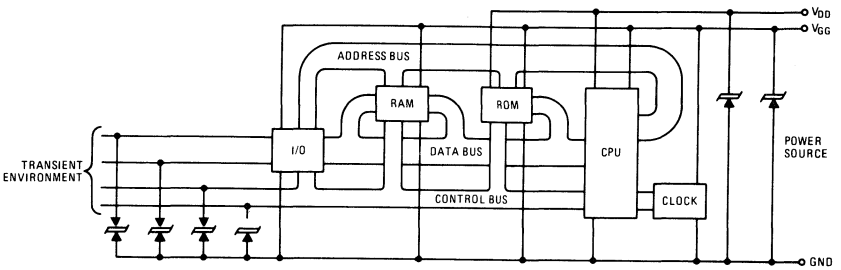


Figure 9—R.F. Coupling

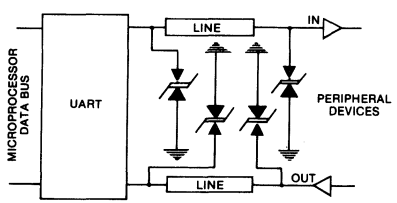
*Will not appreciably affect the "drop out" time of the relay or contactor.

**LC Series

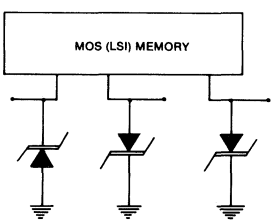
TransZorb TVSs are characterized by the reverse stand-off voltage (V_R). They are synonymous with the integrated or micro circuit power supply voltage. The breakdown voltage (B_V) is that point at which the TransZorb TVS is in avalanche breakdown. This point is temperature dependent and has a positive temperature coellicient. Allowance has been made in establishing the minimum breakdown voltage at 25° C to provide a safe operation over the full temperature range of -65° C to +150° C.



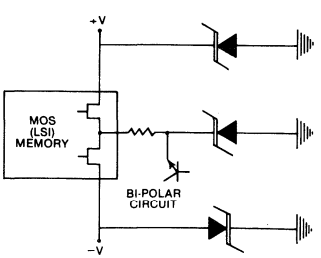
The TransZorb TVS on the signal and input power lines prevent microprocessor system failures caused by transients (electrostatic charges), AC power surges, or during switching of the power supply to ON or OFF. A static discharge can exceed 10,000V for 10 microseconds with a 60 Amp current potential. 10V applied to a typical T^2L circuit for 30 nanoseconds will cause destruction. Placing TransZorb TVSs across the signal lines to ground will keep unwanted transients out of the Data and Control Buses. TransZorb TVSs which are shunted across the power lines maintain a continuous operating voltage during AC line surges and switching transients.



Transients generated on the line can vary from a few microseconds to several milliseconds duration and up to 10,000 volts. This threat of potential energy has given rise to high noise immunity integrated circuits. High immunity and super high immunity circuits are prone to damage by noise transients as a result of the power being dissipated by the substrate input diode. Excess current passing through the input diode can cause an open circuit condition or slow degradation of the circuit performance. TransZorb TVSs located on the signal line can absorb this excess energy. For some circuit applications a low capacitance unit may be required, which is available upon request.

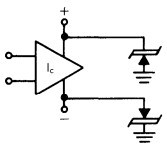


The TransZorb TVSs protect the internal MOSFET from transients introduced on the power supply line. When interfaced with bipolar TTL circuits, the same power supply is often used. A common practice is to place a series protection diode from source to gate, but this does not offer protection from source to ground and is usually limited on peak power dissipation. A TransZorb TVS is required on each voltage supply line to the integrated circuit.

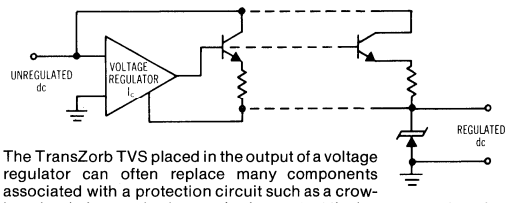


Totem pole output circuits often generate current spikes requiring decoupling capacitors. While maintaining circuit continuity, the TransZorb TVS is capable of absorbing the energy pulse as well as eliminating noise spikes due to such things as cross-talk, etc. A clamp diode in the IC substrate is limited in conduction current, <100 mA, providing a minimum protection.

DC LINE APPLICATIONS

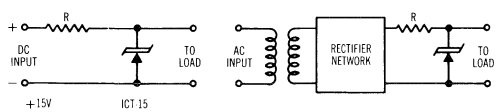


The TransZorb TVS on the power line prevents IC failures caused by transients (electrostatic discharge), power supply reversals or during switching of the power supply to on or off.

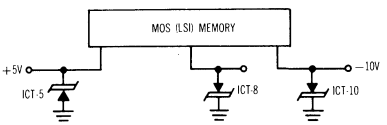


The TransZorb TVS placed in the output of a voltage regulator can often replace many components associated with a protection circuit such as a crowbar circuit. It may also be required to protect the bypass transistor from voltage spikes across the collector to emitter terminals.

Typical power sources employing the TransZorb TVS for transient protection.

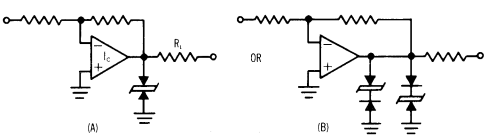


The TransZorb TVS is chosen in which the reverse stand-off voltage is equal to or greater than the DC output voltage. For certain applications it may be more desirable to replace the series resistor (R) with an inductor. In most applications, a fuse in the line is desirable. Elimination of a transformer will require an LC filter on the line for most industrial applications, when the TransZorb TVS is placed on the input to the power supply and with an input voltage greater than 40 volts.

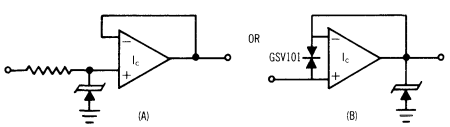


The TransZorb TVSs protect the internal MOSFET from transients introduced on the power supply line. When interfaced with bipolar TTL circuits, the same power supply is often used. A common practice is to place a series protection diode from source to gate, but this does not offer protection from source to ground and is usually limited on peak power dissipation. A TransZorb TVS is required on each voltage supply line to the integrated circuit.

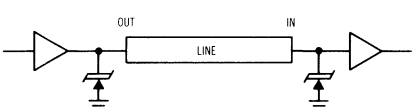
SIGNAL LINE APPLICATIONS



A TransZorb TVS on the output of an Op-amp will prevent a voltage transient, due to a short circuit or an inductive load, from being transmitted into the output stage. Fig. A is for linear circuits whereas Fig. B may be required for reducing effective capacity at the output. The TransZorb TVS and a blocking diode is available as a single unit.

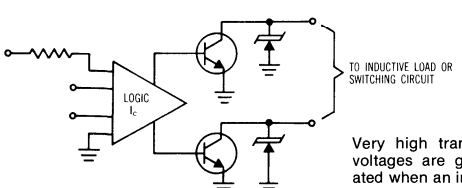


Input states are vulnerable to low energy, high voltage static discharges or crosstalk transmitted on the signal wires. Limited protection is provided by the clamp diode or an input network within the IC substrate. The diodes, however, must have a breakdown voltage greater than the supply voltage (V_{CC}) and are limited in current capacity.



Transients generated on the line can vary from a few microseconds to several milliseconds duration and up to 10,000 volts. This threat of potential energy has given rise to high noise immunity integrated circuits. An independent study* has found that high immunity and super high immunity circuits are prone to damage by noise transients as a result of the power being dissipated by the substrate input diode. Excess current passing through the input diode can cause an open circuit condition or a slow degradation of the circuit performance. TransZorb TVSs located on the signal line can absorb this excess energy.

*The Radio & Electronic Engineer, Vol. 43, No. 4, April 1973.



Very high transient voltages are generated when an inductive load is disconnected, such as motors, relay coils and solenoids. The TransZorb TVS provides protection for the output transistor as well as the IC, eliminating a resistor/capacitor network. The ICT series TransZorb TVS is capable of dissipating the full load current for short duration pulses (<8.3 msec). For longer pulses, the TransZorb TVS is available in stud or press fit package.

TransZorb TVSs can be used in series or parallel to increase their power handling capability. No precautions are required when using TransZorb TVSs in a series string since power dissipation for two or more devices of the same type is equally shared. When using TransZorb TVSs in parallel it is necessary for the units to be closely matched (approx. 0.1 volt of each other) in order for equal sharing to take place. Matched sets can be ordered from the factory for an additional charge.

POWER SUPPLY VOLTAGE TRANSIENT ANALYSIS AND PROTECTION

by
Richard D. Winters
General Semiconductor Industries, Inc., Tempe, Arizona

Voltage Transient

Definition: Unanticipated Change In Voltage

Any discussion on transients should begin with a basic definition and characterization. A voltage transient can be readily defined as "an unexpected or unanticipated change in voltage caused by an unpredictable and sometimes unprecedented occurrence."

One must also differentiate between what is a voltage transient and a power surge. The cause of the two are *different*. The magnitude and destructive capabilities or energy in the two are *different*, and the technology for suppressing the two are often quite *different*, so therefore, a distinction is essential. At General Semiconductor Industries, we arbitrarily have chosen 8.4 millisecond as a time duration which separates the two.

ARBITRARY DEFINITION

TRANSIENTS ARE:

1. **LESS THAN 8.4 mS IN DURATION.**
2. **CHARACTERIZED BY SINUSOIDAL OR EXPONENTIAL WAVE SHAPES.**
3. **NORMALLY ASSOCIATED WITH HIGH IMPEDANCE SOURCES.**
4. **TRANSIENT VOLTAGE LEVELS CAN RANGE FROM A FEW MILLI VOLTS TO 18,000 VOLTS IN A NORMAL WORKING ENVIRONMENT.**

SURGES ARE:

1. GREATER THAN 8.4 mS IN DURATION.
2. CHARACTERIZED BY A SQUARE WAVE OR EXPONENTIAL WAVE FORM.
3. NORMALLY ASSOCIATED WITH LOW IMPEDANCE SOURCES.
4. 90% OF SURGE MAGNITUDES WILL BE LESS THAN 2X NORMAL OPERATING LEVELS.
5. 99% OF SURGE MAGNITUDES WILL BE LESS THAN 3X NORMAL OPERATING LEVELS.

Transient vs. Surges

Transients, therefore, are characterized by high-voltage departures which are less than 8.4 millisecond in duration.

Power surges are characterized by low voltage excursions, lasting greater than 8.4 milliseconds in duration. (On a 60 cycle ac line, any departure from normal power over one-half of the sinewave can almost always be traced to the power source or associated equipment.)

Transients can be categorized into four basic threats:

1. Lightning
2. NEMP or Nuclear Electro-Magnetic Pulse
3. Electro-Static Discharge (ESD).
4. Inductive Switching

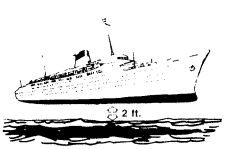
This paper will deal primarily with the transients associated with inductive switching, however, in most instances, with proper component selection and design consideration, the transient suppressors can protect a system from all transient sources. Lightning, NEMP, and electro-static discharge (ESD) are each a study unto themselves, and will be discussed here only briefly in order to leave you with an appreciation of the problems which each present.

Lightning

The power supply manufacturer, by systems definition, normally receives a security blanket of protection from his O.E.M. customer. The exception comes if he is dealing directly with any utility or telecommunication company. It is then that government specification, such as REA PE60 or Bell Telephone requirements, become contractual.

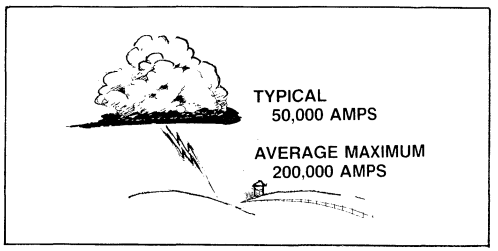
Since the days of Ben Franklin, lightning is the most studied natural phenomenon which we know the least about. It can be stated, that "lightning is Predictably Unpredictable."

The return lightning strike can contain currents in excess of 200,000 amperes, with a total collective energy to lift the QE 2, two feet in the water.



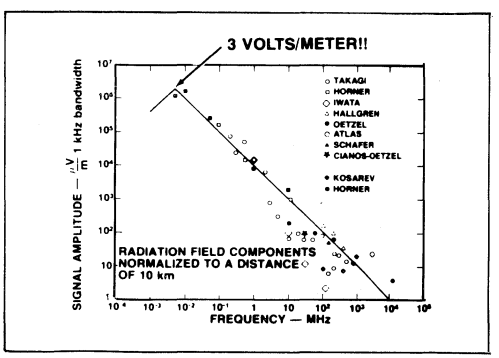
SUFFICIENT ENERGY TO LIFT THE QUEEN ELIZABETH II *2 FEET!*

No one suppresses economically or effectively the energy of a direct strike. What we are concerned with are the secondary inductive effects, and subsequent direct coupling of any earth to cloud, intracloud, or cloud to cloud discharge. The inductive effects of lightning have been characterized and if one were to protect from 95% of the induced voltages and currents associated with this type of electrical activity, the system must be able to withstand voltage up to 5,000 volts and currents in excess of 50 amperes.



Stanford Research has published a report on lightning. Included in the report are two extremely interesting tables which document the effect of induced lightning.

1. Maximum peak amplitude in volts normalized at 10 kilometers.
2. Static magnetic field in amps per meter.



Peak Received Amplitude For Signals Radiated By Lightning

PEAK CURRENT (kA)	STATIC MAGNETIC FIELD (A/m)		
	10m FROM FLASH	100m FROM FLASH	10 km FROM FLASH
10	1.6×10^{2}	16	1.9×10^{-2}
20	3.2×10^{2}	32	3.8×10^{-2}
30	4.8×10^{2}	48	5.8×10^{-2}
70	1.1×10^{3}	1.1×10^{2}	13×10^{-2}
100	1.6×10^{3}	1.6×10^{2}	19×10^{-2}
140	2.2×10^{3}	2.2×10^{2}	27×10^{-2}
200	3.2×10^{3}	3.2×10^{2}	38×10^{-2}

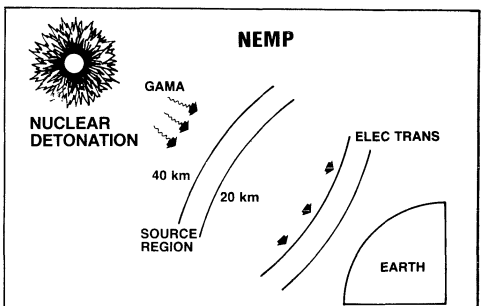
Static Magnetic Fields From Close Lightning

Nuclear Electro-Magnetic Pulse (NEMP)

Nuclear Electro-Magnetic Pulse (NEMP) have certain characteristics which relate directly with characteristics one can encounter with static discharge. Specifically, fast rise time and large voltage potentials.

During a high altitude nuclear detonation, gamma rays are released and set into motion high speed electrons which, subsequently, are curved or partially deflected by the electromagnetic belt surrounding the earth. This reaction creates the electromagnetic pulse. The upset occuring by the deflection generates a voltage pulse of 50,000 volts per meter—300 miles from actual point of detonation, with a rise time of approximately 5,000 volts per nanosecond.

In a small way NEMP is comparable to lightning which has a field density of 3 volts per meter, six miles from point of discharge, with a rise time of 600 volts per microsecond. Because of the large magnitude and frequency spectrum NEMP represents, there are basically no "off-the-shelf" R-C or L-C filters that can effectively reduce or eliminate the NEMP pulses.



	FIELD DENSITY OR MAGNITUDE	RISE TIME
NEMP	50KV/m @ 500 km	5KV/ηS
LIGHTNING	3V/m @ 10 km	600V/μS
STATIC DISCHARGE	20KV AT IMPACT	2KV/ηS

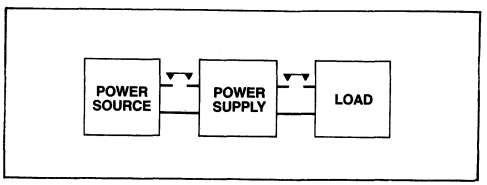
Electro-Static Discharge (ESD)

According to studies made at Sandia Laboratories in Albuquerque, static discharge has a rise time of 2 kilovolts per nanosecond, with voltage magnitudes in excess of 20,000 volts, from a normal body discharge.

It might be interesting to know that the normal charge, in identical conditions from a man is approximately 16,000 volts whereas a woman could have a charge build-up of approximately 20,000 volts. The makeup of the body chemistry is different between a man and a woman, contributing to a significant variance in the dielectric, and this accounts for the larger charge build-up in the woman. The body capacitance can vary from 80 to 500 pFd at the extremes with a discharge resistance of 50 to 5000 Ohms.

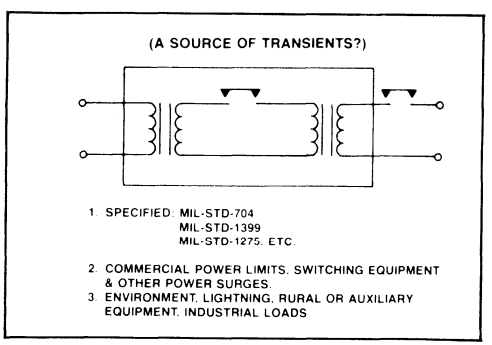
The switching power supply designer is confronted with transients from all sides, from the power source, from the load, and from the power supply itself.

First of all let's look at the power source as the major transient generator. Quite often the power supply is destined to be used in an application which has been defined by a military specification such as MIL-STD-704, for aircraft power; MIL-STD-1399, for shipboard application; and MIL-STD-1275 for mobile vehicles are the governing documents. In addition, the designer must consider commercial



Inductive Switching Within The Power Supply

power limits and various types of switching equipment and power surges associated with electrical distribution. The power source is also subjected to environmental conditions, such as, lightning, auxiliary power equipment, and various large inductive industrial loads. In other words, the power source is indeed, a generator of innumerable transients of which the design engineer has no control.



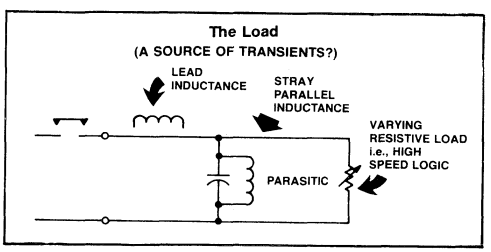
The Power Source

Specified power source transients can be real, imagined, or wishful thinking. There is probably no better example of this than MIL-STD-704, which was issued as a fully coordinated standard in October of 1959. It replaced MIL-E-7894, which was developed in controversy between Aircraft-Electrical System Designers and Utilization Equipment Designers. Electric Power Designers try to maintain wider limits while Utilization Equipment Designers try to narrow the same limits. The original MIL-STD-704 made no recognition of spikes or voltage transients. Spikes did exist and so did systems failures. In 1967, ARINC (Aeronautical Radia, Inc.) published a study which vehemently attacked MIL-STD-704, and in essence said, "Damned if you do, and damned if you don't." If one abided by MIL-STD-704 and protected to worse case interpretation of the ambiguous document, cost of incorporating maximum transient protection put the supplier in a non-competitive situation, On the other hand, because the short duration transients were not documented, transient generated systems failures were a reality.

The MIL-STD-1399 specification covering shipboard electrical power documents the 2,500 volt spike or transient. On numerous occasions the system designers have interpreted this specification utilizing worse case conditions. When that happens, MIL-STD-1399 comes out as ambiguous as MIL-STD-704 because the worse case source impedance on the ship becomes the impedance of the generator, which is approximately 30 milliohms. Based on an I^2R situation, the 2,500 volt spike, the transient surge is 200 megawatts!! More recent revisions of this spec call out a source impedance of the transient spike of 5 Ohms, which is reduced to 1000V. Based on this 5 Ohms, the peak current for a 115V ac circuit is less than 150A and well within the capability of a device such as the 60KS200C.

The Load: A Source Of Transients?

The power supply load is always a potential transient generator. The load can consist of lead inductance, stray parallel inductance, a varying resistive



load or a partially inductive load. In many situations, lead inductance need not be a major consideration, however, in applications where high speed switching occurs the voltage generated due to lead inductance becomes a major concern. The voltage generated by inductance is defined by $V = L\ di/dt$. In a high speed computer application, a 5 volt 1,000 watt supply can be used to feed 1,000 T^2L circuits with power to spare. Each gate typically pulls 1 to 10 milliamps, and each circuit has 15 gates. A total of 15,000 gates could have current consumption of 150 amperes. The probability of 1% of the gates or logic shifting at any given instant is very high. Let us assume the following:

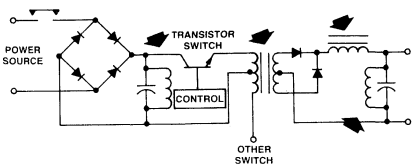
1. Lead length from the power supply to the logic board is 3 meters.
2. The inductance of the lead is 10^{-6}H/meter.
3. The switching time of the T^2L logic is 20 nanoseconds.

We now have a transient generator capable of producing anywhere from 23 volts to 225 volts on the 5 volt logic bus. The "over-voltage protector," the "remote voltage sense," and a current foldback system have no effect or protective capabilities which shunt the fast rise time transient.

The Power Supply: A Source Of Transients?

Without a doubt the switching power supply is a source of transients. Not only is it a transient generator, it's an EMI generator, a surge generator, and to us, a semiconductor manufacturer of switching transistors, a *transistor destroyer*.

The Power Supply
(A SOURCE OF TRANSIENTS?)



The transient producing elements of the power supply are primarily:

1. The filter circuits consisting of a filter capacitor and sometimes a large filter inductor.
2. The switching transistor in conjunction with the inverter transformer.

Both the storage time and the fall time of the transistor have an effect on the transient waveform with respect to voltage magnitude and duration.

The harder the transistor is driven the faster the fall time, the higher the magnitude of the spike voltage which is generated by the output transformer. Most switching circuits today utilize transistors with a V_{CEO} two and one-half times the supply voltage and a "clamp" or "snubber" circuit to cope with the self-generated spikes.

The power supply is in a very unique, if not hazardous situation. Not only is it faced with transients from the power source, transients from the load, but it must also be able to operate with its own internally generated transients.

In a switching environment, many electronic components are subjected to a "wear-out" phenomenon, in other words, the components gradually degrade in their functional parameters to a point they are no longer within their electrical tolerances, and the power supply or electronic equipment becomes inoperative, therefore reliability is a major consideration.

Failure Threshold

The design engineer should be aware that it is not necessarily the total energy within any transient that is the destructive element to his semiconductors, but quite often the voltage magnitude which causes the breakdown within the intrinsic region of a semiconductor, or in some cases, the breakdown of the electrical insulation or passivation.

The following table shows the failure threshold of various semiconductors to fast rise time pulses. It is a proven fact that the energy capability or withstand surge capability of a semiconductor decreases rapidly as the rise time of the pulse increases, in other words, the threshold of failure is significantly lower with fast rise time pulses.

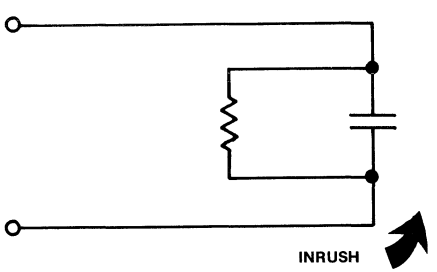
TYPE	MINIMUM JOULE ENERGY	MATERIAL	FUNCTION
MC715	8×10^{-5}	Si	Data Input Gate Integrated Circuit
2N1066	3×10^{-4}	Ge	PNP HF Drift Transistor
RCA CA3005	8×10^{-6}	Si	RF Analog Integrated Circuit
1N3659	8×10^{-3}	Si	Automotive Rectifier Diode
1N457	3×10^{-4}	Si	General Purpose Diode
1N277	2×10^{-5}	Si	High Speed Switching Diode
1N647	2×10^{-3}	Si	General Purpose Diode
1N538	6×10^{-4}	Si	Rectifier Diode
1N126A	1×10^{-5}	Ge	General Purpose Diode
1N23B	1×10^{-7}	Si	Microwave Diode
2N3528	3×10^{-3}	Si	Silicon Controlled Rectifier

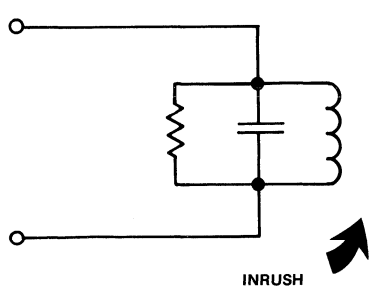
Semiconductor Devices Failure Theshold

Solution

The Capacitor

Transients are normally associated with high frequency components which are several orders of magnitude above the steady state voltage frequency. The obvious solution is to instal a low pass filter. The simplest form of a filter is a capacitor, and hopefully, the capacitor will present a much lower impedance than the transient source, forming a voltage divider. A capacitor, whether it's in the power supply, or on the load, or on the power source works quite well as long as it:



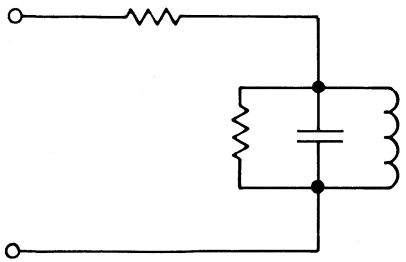


1. Does not load down the system and does not create any current "in-rush" problems.

2. Does not have any parasitic inductance which will spoil the high frequency admittance of the device.

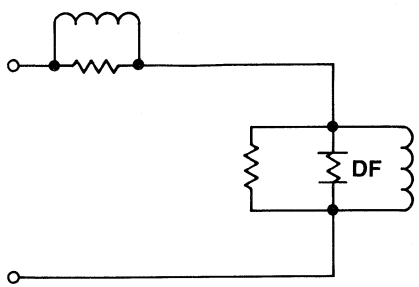
3. Does not degrade with time or ripple current.

Sometimes a resistor in series will reduce the current "in-rush" problem, but then alas, it also reduces the effectiveness of the capacitor.



If the transient has high ac current components in either polarity, the capacitor will also become ineffective and the inductance associated with our filter resistor will also reduce the effectivity. As you can see from this figure, our simple capacitor filter is now, not quite so simple.

In addition, transient oscillations or ringing can



develop. When that happens our capacitor can have the effect of increasing the transient voltage if the transient source is inductive.

Transient Voltage Suppressors

Most transient voltage suppressors are characterized by a clamping, Zenering or avalanching action. There are several types of these products available on the market. Most popular are selinium, metal oxide varistors and silicon junction devices that have been designed and manufactured primarily for voltage suppression, rather than regulation. One of these, the TransZorb® TVS, is of the latter category. In evaluating any type of voltage suppressor, the following characteristics must be taken into consideration.

1. The overall performance which includes power rating, maximum operating temperature, size, response times, parasitic leakage, and capacitance.
2. Clamping factor. The clamping factor is the ratio of the breakdown of the device at extremely small current and the maximum voltage appearing across the device during a specified transient condition.
3. Available voltage. What is the selection of available voltages? Quite often the operational limits of equipment incorporating semiconductors is very close to the failure threshold of the devices and the voltage selection becomes of extreme importance.
4. Cost per joule. What is the actual cost for transient protection in terms of watt-seconds should be the prime concern to the design engineer.
5. Reliability. Is it a Mil-Spec item? Will it operate over maximum temperature ranges? Does it also have a "wear-out" in a transient environment?

	SELENIUM	VARISTOR	TRANSZORB (Silicon Junction)
Overall Performance	Poor	Better	Best
Clamping Factor	Poor	Better	Best
Voltage Availability	Poor	Better	Best
Cost per joule	Better	Best	Poor*
Reliability	Poor	Better	Best

*On a dollar per watt or dollar per joule, Silicon devices are two times the cost.

Comparison Of Voltage Suppressors

Selecting A Transient Suppressor

In selecting the transient suppressor for the application, one first must be able to describe or evaluate the transient conditions.

1. The transient waveform should be defined both with respect to source impedance and voltage or peak current. The voltage or peak current waveform can best be described as an impulse on a decaying damped sine wave.
2. The "stand-off" voltage should be selected. This voltage is equal to or slightly greater than the maximum steady state voltage rating of the equipment.
3. A determination must be made of the maximum power dissipation, which includes repetition rate.

And last, and probably the most important is, what is the clamping voltage of the unit? The clamping voltage is the maximum voltage appearing across a suppressor due to the peak pulse current and temperature. A clamping voltage must be selected below the threshold failure level of the circuit components.

Transient Description	A — Define voltage waveform B — Define source impedance
Stand-off Voltage (V_R)	Maximum steady-state voltage rating
Maximum power dissipation (P_{Pmax})	Define transient and peak pulse power for a specified time duration and repetition rate.
Clamping Voltage (V_C)	Maximum voltage appearing across a suppressor due to the peak pulse current and temperature.

Selection Guide

Protecting The Power Switching Supply

The following illustrations depict various methods of protecting the voltage sensitive elements within the switching power supply.

PREFERRED

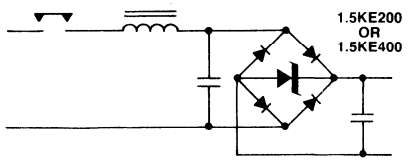


FIGURE 1—Protecting From Line Transients

The TransZorb TVS placed across the bridge rectifier will clamp most line transient or load "spikes". (It should be noted that the rectifier diode peak surge current ratings must be compatible with the maximum surge current expected through the TransZorb TVS.)

Selection of the approximate TransZorb TVS would proceed as follows:

1. Determine the maximum dc plus peak ripple voltage, then add the high side tolerance to this value.
2. Select a TransZorb TVS to have a reverse stand-off voltage equal to or greater than the maximum circuit voltage, as defined in 1 above. This will allow for operating over the temperature range of -65°C to +175°C.
3. Define the waveshape or duration of the transient.
4. Determine the peak pulse current the TransZorb TVS will be required to pass. Check this against the maximum Peak Pulse Current shown on the TransZorb TVS data sheet. If the predicted current exceeds the device rating, don't dispair—as covered later in this discussion—something can be done.
5. If the current to be handled is within the device rating, proceed to determine the maximum peak pulse power the TransZorb TVS must handle. This value is obtained by multiplying the transient peak pulse current by the maximum clamping voltage of the selected device.
6. If peak pulse power is within the maximum rating of the TransZorb TVS, use the device.

   To evaluate this, the following criteria shoud be used:

   (a) For a transient pulse width of an exponential delay, define "pulse time" as the duration of the pulse from the 10% amplitude point on the leading edge to the 50% amplitude point on the trailing edge. From the TransZorb TVS data sheet chart of "Peak Pulse Power vs Pulse Time," determine the Peak Pulse Power rating of the device for the computed "Pulse Time" of the incident pulse.

   (b) For transients which approximate a "sine wave" in pulse waveshape, use the total pulse width as the "Pulse Time" and multiply the corresponding "Peak Pulse Power" value by 0.75 to obtain the effective TransZorb TVS rating.

   (c) For "Square wave" shaped transients, multiply the "Peak Pulse Power" value for the corresponding pulse time by 0.66 to obtain the effective TransZorb TVS rating.

   (d) If the transient is a rapidly damped sine wave, or rapidly damped square wave, with one time constant within eight cycles, rate the same as if the device were subjected to just one cycle (highest amplitude) of the wave train.

   (e) For any other transient conditions, consideration must be given to the *average* power handling capability of the device and/or the total transient energy must be summed and evaluated in respect to thermal deratings.
7. If the peak pulse power of the incident pulse is greater than the rating of the TransZorb TVS, devices may be "stacked" in series to increase the power rating for voltage above 16 volts. Notice that, when stacking the same *Power rating* devices, the current rating goes up in proportion to the number of devices stacked! It is impossible to achieve the necessary power rating by stacking the devices in series, parallel stacking can be done effecively for voltages below 100 volts. Close mathcing, about 200mV between each device, is necessary to assure even loading of the transient between the TransZorb TVSs. Series/parallel stacking can be done for higher voltages and powers. This must be done at the factory for optimum results.
8. Observe the maximum clamping voltage, which is 1.33 times the Breakdown Voltage. If this is greater than the circuit can withstand, devices can be constructed to reduce the clamping factor of approximately 1.2 as compared to the 1.33 clamping factor for a single device.
9. Surge protection assemblies are also available when it is necessary to "short" extremely large current pulses. This assembly utilizes a gas gap with the TransZorb TVS. Requests for this type of protection product must be coordinated with the factory.

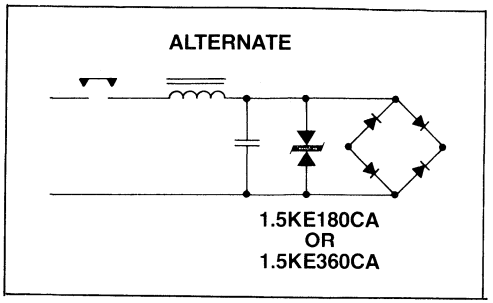


FIGURE 2—Protecting From Line Transients (Alternative)

Alternate (Figure 2)

In a situation where the surge currents to be handled by the TransZorb TVS would overstress the rectifier diodes, a bipolar TransZorb TVS can be used directly across the input filter capacitor with equal line shunting effectiveness.

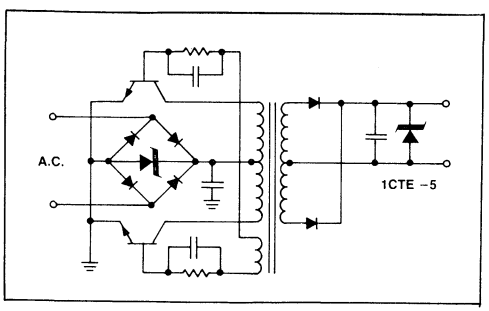


FIGURE 3—Protecting The Low Voltage Schottkys

Low Voltage Schottkys (Figure 3)

Placing a second TransZorb TVS across the output terminals of the Schottky rectifiers, as shown in Figure 3, provides protection for the Schottky devices from any load voltage transients and simultaneously provides effective protection from any secondary leakage inductance voltage "spikes."

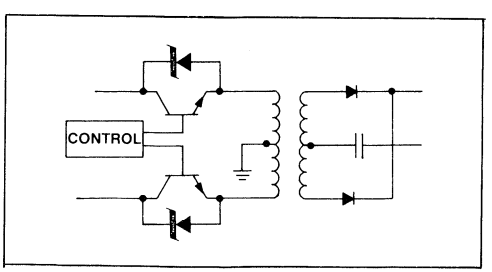


FIGURE 4—Protecting From High-Speed, Self-Induced Switching Transients

Self-Induced Switching Transients (Figure 4)

TransZorb TVS "clamp" placed across the collector-emitter of each of the switches provide a high degree of protection against transient voltages which occur when the transistor is switched to its "off" state. The use of appropriate collector-emitter reverse voltage clamps can completely eliminate any danger of the device ever switching through the energy sensitive $E_{S/B}$ region.

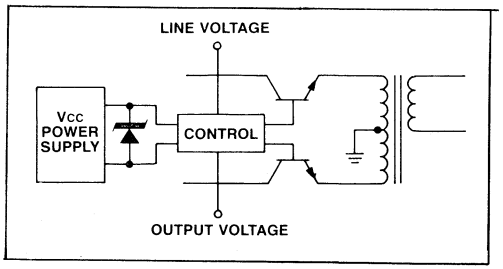


FIGURE 5—Protecting The Control Circuitry

Protecting The Control Circuitry (Figure 5)

Conclusion

Often the designer can overlook the effect of power supply transients, whether self induced or due to coupling paths from other system networks. A TransZorb TVS "clamp", placed across the supply terminals of sensitive control networks can avoid catastrophic failures due to line transients, supply glitches, or transients induced in the system due to unrelated system failures.

Conclusion

Performance and reliability should be the prime concern of the switching power supply design engineer. Transients have been around for a long time and they are not about to go away. What concerns us all is selecting the right device, for the right application, at the least possible cost to the end user.

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NEMP TRANSIENT SUPPRESSION USING THE TRANSZORB® TVS

by
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Summary

A nuclear device which is detonated above the atmosphere produces an extremely high power Electromagnetic Pulse (NEMP). Semiconductor devices are quite vulnerable to this fast rise-time pulse with destruct threshold values in the microjoule range.

TransZorb TVSs have been evaluated and found to be very effective in protecting sensitive electronic equipment from the harmful effects of NEMP. With high pulse power capability, low clamping voltage and subnanosecond response time, the TransZorb TVS has been used in many military systems to provide protection from both NEMP and normal system transient voltage.

Special insertion techniques for fast rise-time transients are required to optimize the protection offered by the TransZorb TVS. This includes minimizing the lead inductance between the protected circuit and ground. Inductance values as low as 10^{-8} henry can cause harmful effects.

In addition to the TransZorb TVS, several other device types have been evaluated for NEMP protection including zener diodes, metal oxide varistors and gas surge arrestors and are discussed in this report. Zener diodes have lower failure thresholds than TransZorb TVSs, and also significantly higher clamping voltages which may not provide adequate protection. Metal oxide varistors also have significantly higher clamping voltages and degrade in breakdown voltage and leakage current from successive simulated NEMP pulses. Gas surge arrestors have very high surge striking voltages, but turn on in less than 10 nanoseconds.

Applications using TransZorb TVSs and hybrid circuits using TransZorb TVSs and spark gaps are also reviewed and laboratory data is presented to illustrate the degree of protection provided by these components.

NEMP Transient Suppression Using The TransZorb TVS

The NEMP Threat

When an exoatmospheric nuclear detonation occurs, a significant amount of energy released is expressed as gamma radiation. This radiation expands outward in a relatively thin spherical shell. Upon striking the atmosphere, compton electrons are generated by the gamma rays impinging upon molecules of air and transferring energy to electrons, imparting a high velocity and subsequently separating them substantially from the heavier ionized atoms. This action forms an electric field. These high velocity electrons are subsequently influenced by the earth's magnetic field. As they spiral in along this magnetic field their collective energies are transformed into a broad wavefront of an extremely high magnitude, short duration radio frequency pulse called EMP or NEMP (Nuclear Electromagnetic Pulse). NEMP fields may be as high as 100,000V per meter having durations of 250 nanoseconds and rise-times of the order of 5kV per nanosecond.

Semiconductors are particularly vulnerable to NEMP. Some examples of burn-out energy include the following:[1]

Minimum NEMP Energy To Cause Burnout		
Device	Description	Minimum Enegy (Joules)
2N3528	Silicon Controlled Rectifier	3×10^{-3}
2N4420	GE PNP Switching Transistor	3×10^{-4}
2N4420	Field Effect Transistor	1×10^{-5}
MC715	IC Input Gate	8×10^{-5}

The SN55107 type line receivers subjected to 200 nanosecond duration pulses exhibit burn-out energies of 2.8 microjoules.[2] This illustrates the vulnerability of small geometry semiconductor devices to the fast rise-time, short duration NEMP.

Because of the NEMP threat to sensitive electronic equipment, effective methods must be employed to protect vulnerable systems. The following paragraphs discuss methods, techniques, and components which have demonstrated effectiveness in laboratory environments and may be used as guidelines in designing for NEMP protection in military electronics.

The TransZorb TVS

What It Is And How It Works

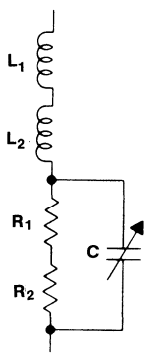
The TransZorb TVS is a silicon device designed specifically for transient suppression. It contains a large area pn junction having integral heat sinks and is capable of handling short duration high power pulses (1,500 watts for 1 millisecond and 100,000 watts for 100 nanoseconds). The TransZorb TVS protects by clamping transient voltages down to a safe level with subnanosecond reaction time. Small

size (DO-13) axial lead package) and available over a broad voltage spectrum, this device has found many applications in NEMP transient suppression.

TransZorb TVSs are presently being used on or designed into aircraft, missile systems, shipboard installation, various telecommunications programs and many other applications requiring NEMP protection or a combination of NEMP protection along with other severe transients environments.

Inductance Effects In Protection Circuitry

Fast rise-time voltage transients in protective circuitry wiring can produce substantial secondary effects due to what may appear to be negligible inductance in the circuit.



L_1 - External Inductance
L_2 - Internal Inductance
R_1 - Electrical Impedance
R_2 Self Heating Resistance
C - Capacitance

FIGURE 1
Equivalent Circuit Of A TransZorb TVS

These "inductors" are illustrated in Figure 1, which shows the equivalent circuit of the TransZorb TVS. Inductance in the wiring between the protected circuit and ground, excluding the TransZorb TVS, is represented by L_1. The very small amount of inductance, about 10^{-8}H, in the TransZorb TVS is represented by L^2. When a high transient voltage appears across the protected circuit, it is clamped to a very low value by the TransZorb TVS. The fast-rising high current in the inductance produces a "secondary" or overshoot voltage transient which is described by the equation:

$$V_{(t)} = L\ di/dt$$

where L = Inductance in henrys
I = Current in amperes
t = Time in seconds

Since NEMP is characterized by a fast rise-time, about 5kV/nsec, very high overshoot voltages can be generated. For the purpose of illustration, a 30V TransZorb TVS is used to represent varying degrees of protection afforded by the same component, but with different lead lengths between the protected circuit and ground. These lead lengths contribute a "negligible" amount of inductance; the effects of which become very profound under the fast rise-times of NEMP as shown in Figures 2-5. These overshoot voltages appear across the protected circuit.

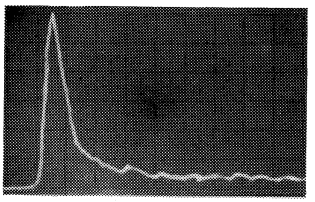


FIGURE 2
3 Inch Leads
Vertical Sensitivity: 200V/div.; Horizontal Sensitivity: 10nsec/div.

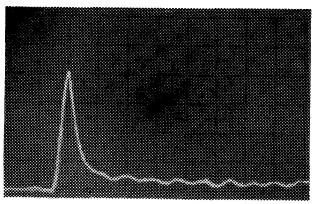


FIGURE 3
1.5 Inch Leads
Vertical Sensitivity: 200V/div.; Horizontal Sensitivity: 10nsec/div.

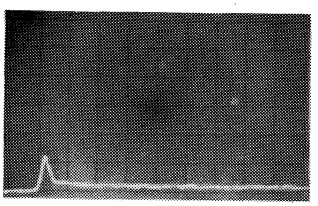


FIGURE 4
No Leads
Vertical Sensitivity: 200V/div.; Horizontal Sensitivity: 10nsec/div.

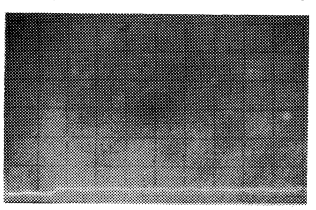


FIGURE 5
Disc Package
Vertical Sensitivity: 200V/div.; Horizontal Sensitivity: 10nsec/div.

The energy under the overshoot portion of the curve shown in Figure 2, which is due to inductance is calculated to be 150 microjoules. This is more than an order of magnitude above the threshold of destruction for SN55107 line recievers. This is also sufficient to destroy field effect transistors, IC input gates, and borderline for damging germanium pnp switching transistors. With 1 1/2 inch leads as shown in Figure 3, the energy due to lead inductance is 70 microjoules, still sufficient to destroy field effect transistors and IC input gates. With the leads removed, as depicted in Figure 4, and the input directly placed across the device case and insulated tubulation, there is a substantial reduction down to .67 microjoules. With the TransZorb TVS repackaged

into a disc form to yield minimum inductance and using low inductance insertion methods in the protective circuit, there is no overshoot observed, thus the intended protection is optimized as shown in Figure 5.[3]

Simulated NEMP Testing

A block diagram of the equiment used in performing tests for gathering data described in this report consists of the system as shown in Figure 6.

The circuit is relatively simple in its nature of operation, using a low current, high voltage dc supply to maintain a length of RG/217U cable under constant charge. A test pulse is produced by switching the charge line to the delay line using a high voltage vacuum switch. The pulse width is determined by the length of the charge line. The "delay line" filters out noise and helps to produce a reasonably smooth, square pulse. Rise-time of the pulse is 4kV/nsec. Modified GR type teminals were used at all connections to prevent arc-over of the high voltage, up to 10kV, used in this test equipment.

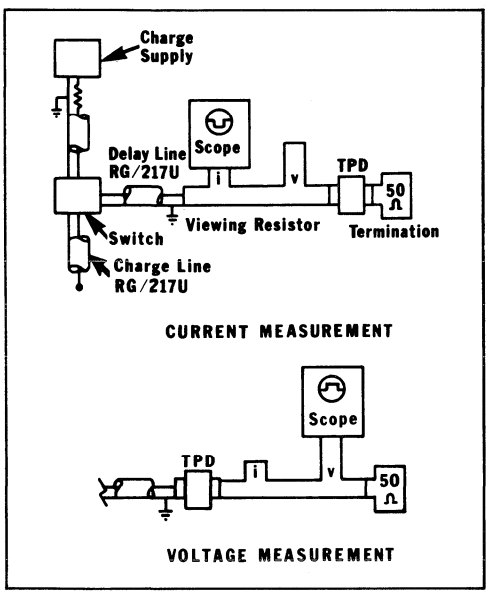
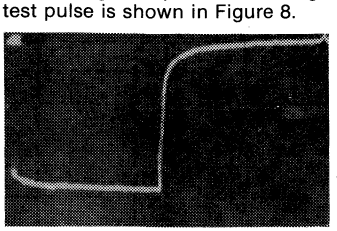


FIGURE 6
Instrumentation

Test Pulse

A typical example of a test pulse is shown in Figure 7, depicting the current through a TransZorb TVS inserted in a TPD (terminal protection device) under a 10kV charge line pulse. The voltage wave front of the test pulse is shown in Figure 8.



Vertical: 40A/div.
Horizontal: 50nsec/div.

FIGURE 7
Current Test Pulse

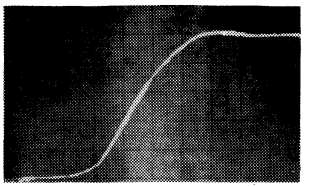


FIGURE 8
Test Pulse Wave Front
Vertical: 2,000V/div.; Horizontal: 1nsec/div.

TransZorb TVSs And Protection From NEMP

In 1971, a study was performed at Fort Belvoir to select devices particularly capable of offering protection against NEMP generated transients. The TransZorb TVS was found to be one of the best devices for this application. An outgrowth of this finding was a feasibility study contract with General Semiconductor Industries to evaluate TransZorb TVSs exposed to laboratory simulated NEMP transients. There were two specific results from this contract. The first was a development of an rf TPD (terminal protection device) for use in the Pershing Missile System for NEMP hardening. Figure 9 depicts the mechanical characteristics of this device.

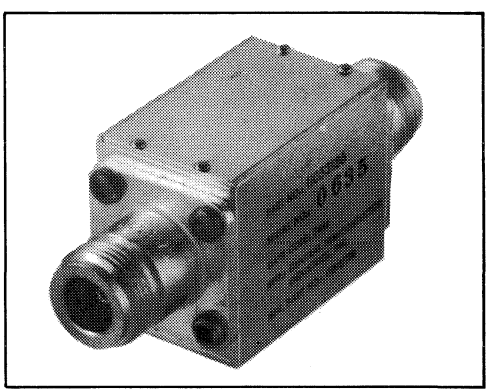


FIGURE 9—TPD 450

The oscillograms in Figures 10 through 13 depict protection levels of 6V, 30V, 90V and 180V, TransZorb TVSs having effectively zero shunt current path. The simulated NEMP transient has a peak current level of 200A.

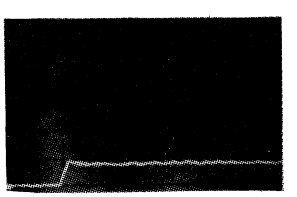


FIGURE 10
6V Low Impedance TPD

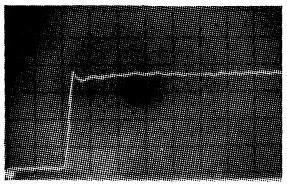


FIGURE 11
33V Low Inductance TPD

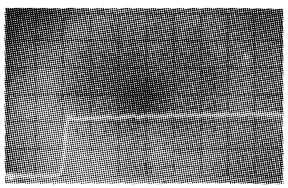


FIGURE 12
90V Low Inductance TPD

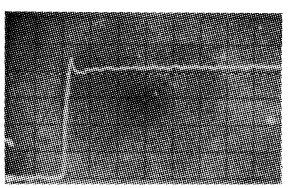


FIGURE 13
180V Low Inductance TPD

It is observed that the clamping voltages of the TransZorb TVS are higher than the breakdown voltages. This is normal as the breakdown voltage is measured at 1mA and the clamping voltage is measured at current levels several orders of magnitude higher. The difference being attributed to thermal and electrical impedance.

TransZorb TVS Capacitance

The TransZorb TVS is fabricated using a large area junction which is a basic requirement for a transient suppressor, hence an inherently higher capacitance than most silicon avalanche devices. Curves showing capacitance at zero bias and at reverse stand-off voltage are shown in Figure 14 for the 1.5kW types At stand-off (operating) voltage, the capacitance ranges from 70pF for the 200V type up to greater than 10,000pF for the 6.8V types.

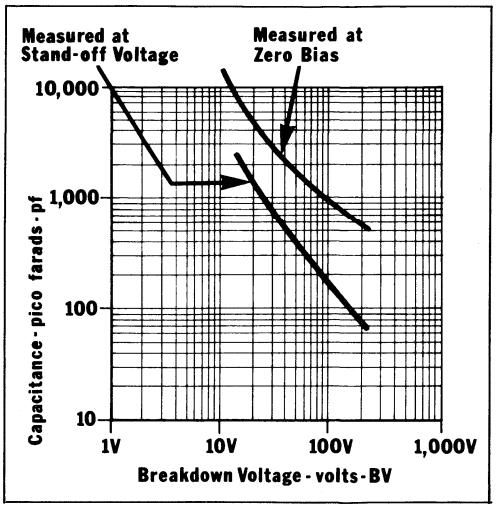


FIGURE 14
Capacitance vs. Breakdown Voltage

Signal attenuation for the low voltage types would make them unusable for rf applications without some method for effectively reducing the capacitance. This can be done by placing a low capacitance diode in series with the TransZorb TVS so that the low capacitance diode conducts only the direction of forward conduction as shown in Figure 15.

The four main requirements of the low capacitance diode include:

(a) adequate rating of the forward surge current parameter;
(b) minimum forward drop at high pulse currents;
(c) the reverse breakdown voltage of the diode must always exceed the TransZorb TVS with adequate margin; and
(d) the capacitance of the diode must be of such value to be compatible with the operational frequency of the circuit.

The LC, LCE and SAC TransZorb TVS series are offered for use in high frequency circuits to reduce signal attenuation. Insertion loss has been measured at less than -0.5db at 100MHz on some experimental devices. For most applications, the upper limit appears to be -1db at 30MHz.

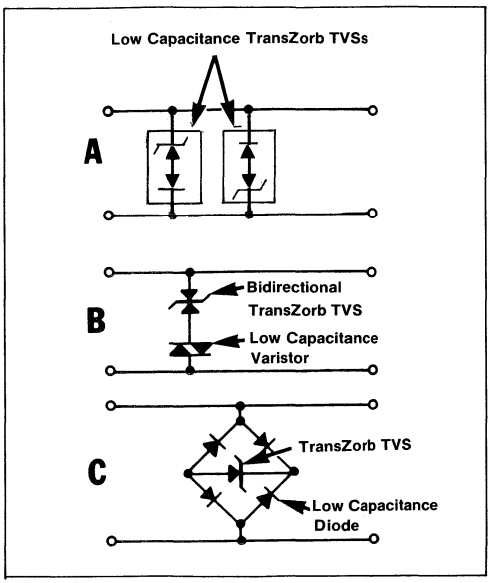


FIGURE 15
TransZorb TVS Capacitance Reduction

For pulses having fast rise-times, of the order of 5kV/nsec, the low capacitance diodes retard turn-on by 5-10nsec, hence an overshoot occurs. An example of this phenomenon is shown in Figure 16.

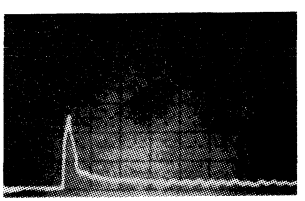


FIGURE 16
Forward Conduction Overshoot
Vertical: 100V/div.; Horizontal: 10nsec/div.

This is the response curve of a low capacitance 6V bidirectional TPD.

Clamping Voltage

Four standard DO-13 TransZorb TVS types ranging from 6.8V through 180V were inserted into low inductance fixtures and measured for clamping voltages under simulated NEMP pulses of 40A, 80A and 120A. Curves illustrating clamping voltages at 70 nsec for these devices are shown in Figure 17.[5]

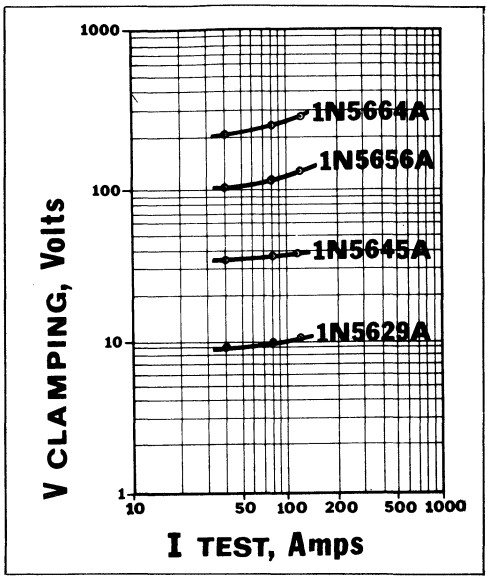


FIGURE 17
TransZorb TVS Clamping Voltage

Other Suppressor Devices

Gas Surge Suppressor

Although gas filled spark gaps were originally designed primarily for protecting telephone apparatus from induced lightning surges, these devices have been found to have relatively fast turn-on characteristics when exposed to laboratory simulated NEMP transients. Using leadless devices inserted in a low inductance housing to minimise inductance effects, several different device types were observed at peak current levels ranging from 50A to 200A in 50A increments. Response curves of the C.P. Clare CG75 device type are shown in Figures 18 through 21.

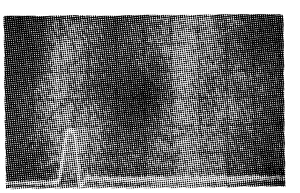


FIGURE 18—CG75 @ 50A
Vertical: 500V/div.; Horizontal: 10nsec/div.

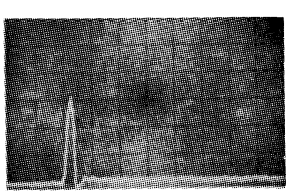


FIGURE 19—CG75 @ 100A
Vertical: 500V/div.; Horizontal: 10nsec/div.

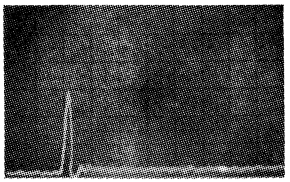


FIGURE 20 —CG75 @ 150A
Vertical: 500V/div.; Horizontal: 10nsec/div.

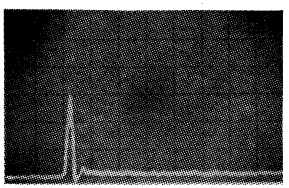


FIGURE 21 —CG75 @ 200A
Vertical: 500V/div.; Horizontal: 10nsec/div.

At levels of 100A through 200A, there appears to be no significant change in surge striking voltage; however, the turn-on time appears to decrease with increasing pulse current. The device turns to full-on condition in about 3 to 4 nanoseconds at 200A. Normal turn-on time for this gas tube device under typical induced lightning surges is in the microsecond range. Similar devices manufactured by Joslyn, Siemens, and Cerberus have also been pulsed and appear to display the same fast turn-on characteristics. Relatively small size spark gaps can offer protection in the multikiloampere range, particularly where protection must be provided against both lightning and NEMP. Under rf condition the arc conduction mode is self extinguishing in the range of 2MHz to 75Mhz for several device types.[6] The capacitance of spark gaps is relatively low, of the order of a few pf, which usually does not offer significant insertion loss below 100MHz. Turn-on time is relatively fast for primary NEMP wave fronts, which limits the leakage energy to a sufficiently low value which can be clamped by a lower energy rated secondary device. Because the voltage drop across the device in arc condition mode ranges from 20-40V, a series resistor or other device must be used to prevent the clamped voltage from going below the operating voltage in dc circuits. Series resistors may also be needed to limit follow-on current and assure arc extinguishing in some ac circuits.

Metal Oxide Varistor

The metal oxide varistor has been initially evaluated for NEMP applications. Response to laboratory simulated NEMP pulses have shown that the device does clamp fast rise-time pulses, but with a much higher clamping factor than silicon transient suppressors. Examples are shown for comparable rated devices in Figures 22 and 23. The pulse level is 60A and the devices are a 67V TransZorb TVS and a V56ZA2 GE-MOV®. Measurements were taken with devices in the low inductance TPD housing to elliminate inductance effects. Clamping factor, which is the ratio of the clamping voltage to measured breakdown voltage, is about 1.1 for the silicon device and 3 for the metal oxide varistor at 20nsec. Pulse energy for this test was 37.5 millijoules.

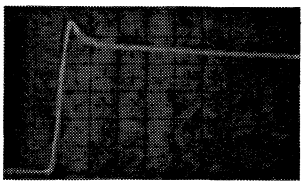


FIGURE 22—GE-MOV
Verical: 50V/div.; Horizontal: 20nsec/div.

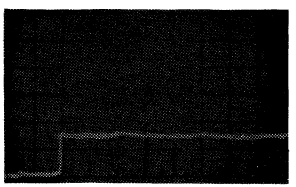


FIGURE 23—TransZorb TVS
Vertical: 50V/div.; Horizontal: 10nsec/div.

Upon multiple pulsing, the MOV appears to undergo degradation compared to the TransZorb. Components of each type were pulsed with simulated NEMP at levels of 20A, 40A, and 60A. Each device was measured for electrical parameters then administered 15 consecutive pulses at the 20A level with 15 second intervals. After post test electrical parameter measurement, the devices were pulsed at the next highest level. The MOV degraded 15% in breakdown voltage at 1mA and increased in leakage current by two orders of magnitude. The TransZorb had no significant change in parameters after pulse testing.

The metal oxide varistor is small in size for its relatively high energy rating and where cost is a major factor, these devices are more economical than spark gaps or silicon transient suppressors. However, clamping factors are high compared to silicon devices, hence less protection capability. The plastic construction of standard product and maximum case temperature of 115°C may make it undesirable for military applications. One manufacture of this product derates the 25°C working voltage down 50% at 85°C, this is probably because the metal oxide varistor has a negative temperature coefficient of voltage.

Zener Diode

Zener diodes have been pulsed under simulated NEMP conditions and shown to survive. When electrical parameters are tested before and after pulse testing with no significant change, it might be assumed that a zener diode would provide adequate protection. However, while observing the components under dynamic test conditions, a surprising observation is made. As the magnitude of the pulse is increased, the clamping voltage increases dramatically as shown in Figure 24[7]. This graph plots the clamping voltage vs pulse current for three 62V zener diodes and a 62V TransZorb TVS. At 200A, the TransZorb TVS is clamping below 90V while the zeners are clamping well over 200V! The oscillographs of the res-

GE-MOV® - Trademark of General Electric Company

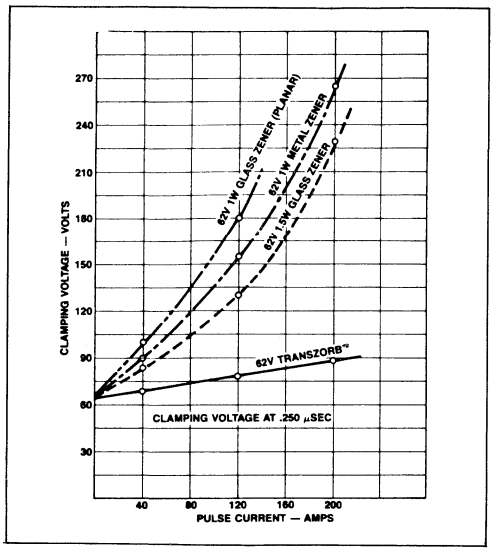


FIGURE 24
Clamping Voltage Of Zener Diodes And TransZorb TVSs

ponse curves as recorded on film for the 200A pulses are shown in Figures 25 through 27. For the zener diodes, the junction temperature increase is reflected in the increase in voltage of approximately 50V over the pulse duration. Note that the TransZorb TVS clamps far lower than the other devices although it is steady-state rated at 1 watt. The narrow spike at the left side of each trace is due to a very small amount of inductance of about 10^{-8} henrys within the device package.

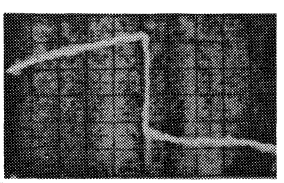


FIGURE 25 —62V 1W Metal Zener
Vertical: 50V/div.; Horizontal: 10nsec/div.

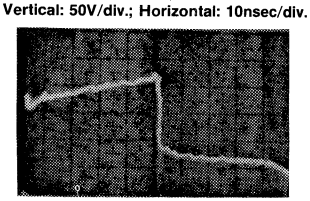


FIGURE 26—62V 1.5W Glass Zener
Vertical: 50V/div.; Horizontal: 10nsec/div.

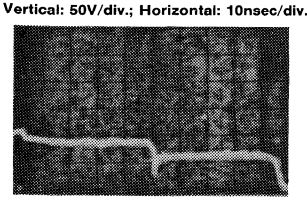


FIGURE 27 —62V TransZorb TVS
Vertical: 50V/div.; Horizontal: 10nsec/div.

Hybrid Circuitry Applications

Cable Isolation

Since the gas surge arrestors turn-on in less than 10nsec, a suitable separation by means of a coaxial cable between a spark gap and a TransZorb TVS has been found to fire the gap under simulated NEMP transients. The TransZorb TVS clamps the voltage spike of 1500V or more admitted by the gas arrestor. Figure 28 illustrates a typical circuit which may be suitable for some applications. The series low capacitance diode along with the silicon avalanche protector is used to effectively reduce circuit capacitance.

Using a CG90 C.P. Clare surge arrestor in a circuit similar to that shown in Figure 28, both 90V and 30V TransZorb TVS types were used as secondary protectors against 200A simulated NEMP pulses to absorb the gap leakage energy. The resultant response of the circuit protection is shown in Figures 29 and 30. In Figure 29, the "tailing off" of the trace below the clamping voltage is caused by the gas gap firing which drops the circuit voltage to between 30V-40V as observed in this oscillograph.

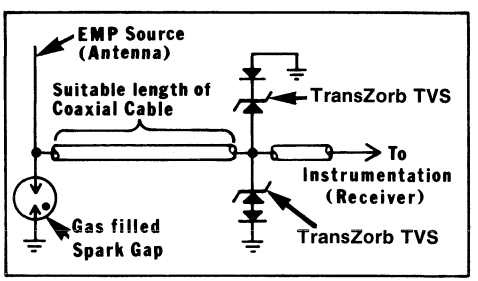


FIGURE 28
Cable Isolation Protection Circuit

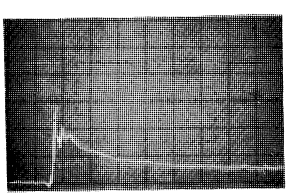


FIGURE 29—90V TransZorb TVS
Veritical: 50V/div.; Horizontal: 10nsec/div.

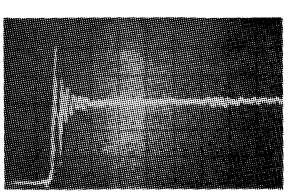


FIGURE 30—30V TransZorb TVS
Vertical: 50V/div.; Horizontal: 10nsec/div.

Standard DO-13 package TransZorb TVSs were used in this study. The internal inductance became less significant due to the slower rise-time of the incident pulse exiting the spark gap, hence an insignificant overshoot. The low energy leakage past the TransZorb TVS, in the .001-.010μj range is well below

the threshold of destruction for semiconductors. Separation of the 90V gap and 90V TransZorb TVS was reduced to about 5nsec with the system still functioning well, as shown in Figure 31. The energy leaking past the gas gap is observed slowly dissipating or "ringing down" as the pulse "reflects" between the gap and the TransZorb TVS.

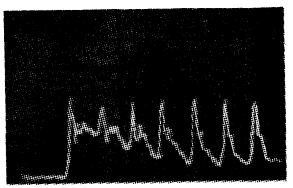


FIGURE 31 —5nsec Separation

At least ten oscillations are required to absorb the energy trapped between the gap and the TransZorb TVS, depending on the pulse amplitude. A two or three ohm resistor in the center conductor between the gap and the TransZorb TVS should be added for protection against induced lightning. All measurements were made with both the gap and the TransZorb TVS in a low inductance TPD housing which was described earlier.

Inductor Isolation

Another method for compatible use of gas surge arrestors and TransZorb TVSs for NEMP protection is to separate these components with an inductance of 5 to 10 microhenrys. A circuit using this technique is shown in Figure 32. The resistor develops a voltage drop to ground through the TransZorb TVS to insure firing of gap under the slower rise-times of induced lightning.

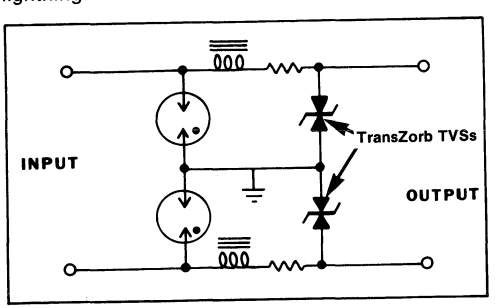


FIGURE 32
Inductor Isolation Protection Circuit (US Patent 3,934,175)

The inductor performs several functions, including reducing the voltage peak, reducing the slope of the wavefront and also delaying the pulse by several nonoseconds. This is illustrated in Figures 33 through 35 which are oscillograms of the pulse at progressive locations in the circuit. Figure 33 shows the 1900V pulse emerging from the spark gap; Figure 34 depicts the pulse which is stretched and reduced in amplitude to 600V as it exits the inductor and Figure 34 illustrates the effectiveness of the TransZorb TVS clamping the residual pulse to less than 200V. The incident simulated NEMP pulse was 200A. A 160V axial leaded TransZorb TVS was used in the circuit. Take special note that Figures 33 through 35 each have different vertical scales. It is of particular importance that the gap is observed to be down to a normal clamping voltage of about 30V in Figure 35, illustrating that the gap is firing and absorbing the bulk of the incident energy. This work was performed with components mounted in low inductance rf fittings of the type described earlier, to minimize inductance effects.

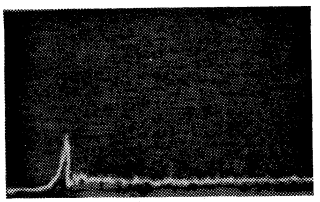


FIGURE 33—Pulse Emerging From Gap
Vertical: 1000V/div.; Horizontal: 10nsec/div.

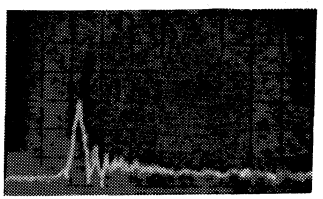


FIGURE 34—Pulse Emerging From Inductor
Vertical: 200V/div.; Horizontal: 10nsec/div.

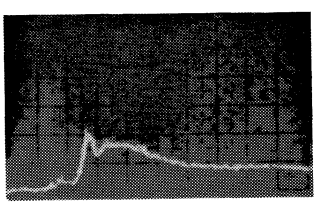


FIGURE 35—Pulse Emerging From TransZorb TVS
Vertical: 100V/div.; Horizontal: 10nsec/div.

Reducing this gas arrestor/TransZorb TVS combination to actual practice was effected for several military telecommunication applications. One configuration includes protection for eight line pairs mounted on a circuit board as shown in Figure 39. The signal line inputs are at the top, feeding into three element gas surge arrestors and subsequently to the inductors, resistors and then to the TransZorb TVSs. Inductance to ground is minimized with a broad grounding foil interconnecting all ground connections and also by providing individual grounding connection for each line pair.

The effectiveness of this arrangement is shown in oscillographs of the output under simulated NEMP pulses of 200A. Figure 40 depicts the output of a 30V protector. The overshoot above the clamping voltage is well below one microjoule with a peak of about 90V and a pulse width of less than 10nsec. The ringing is caused by the inductance in the circuit contributed by the short lead wires of the TransZorb TVS and also by rf noise generated by the arcing gas arrestor. Polaroid film type Polascope 410 having ASA speed equivalent to 10,000 was used for making the oscillographs.

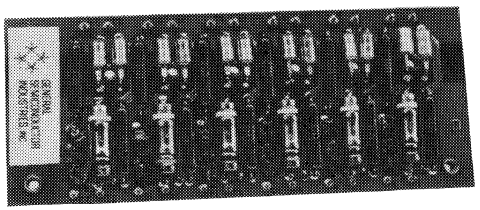


FIGURE 36
Telecommunications NEMP Protector

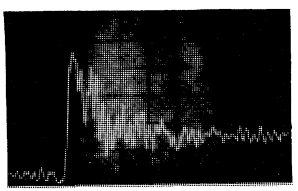


FIGURE 37—30V Protector
Vertical: 20V/div.; Horizontal: 10nsec/div.

Conclusion

The destructive transient voltages generated by induced NEMP presents a unique and sometimes difficult challenge to the design engineer. The fast rise-time induced NEMP transient voltages can generate high voltage spikes across the lead wires of a protector component, hence the requirement for maintaining the shortest possible connections.

TransZorb TVSs have subnanosecond response times and are capable of providing protection from NEMP if proper installation methods are used. Gas surge arrestors have been shown to perform compatibly with TransZorb TVSs to increase surge handling capability. Other devices used for protection, zeners, metal oxide varistors and gas surge arrestors, do provide some degree of protection but do not offer the low clamping voltage necessary to protect vulnerable components such as ICs.

TransZorb TVSs have been used for more than two decades and have a proven history of capability in NEMP protection applications. They have been designed into and are presently used in many military applications protecting both power and signal lines in aircraft, missile, telecommunication and other types of systems.

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LONG-TERM PULSE LIFE AND DESIGN CRITERIA FOR TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS

by
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Condensed from NASA Final Report "Surge Life of Transient Voltage Suppressors" performed under Contract No. NAS8-30811 and "Continuation of Surge Life of Transient Suppressors" performed under Contract No. NAS8-31547. Copies available to qualified users.

Introduction

The technical efforts, results, and conclusions described in this document are a condensation of work previously reported in NASA Contract Nos. NAS8-30811 and NAS8-31547. Due to the length and detail of the original form of these reports, it is desirable to have a short form version which briefly describes the effort and gives an accurate summary of the results. For more details of the information that is contained in this report, copies of the complete original document can be obtained from General Semiconductor Industries, Inc., 2001 West Tenth Place, Tempe, Arizona 85281.

Summary

This report summarizes the work efforts and conclusions as described in the final report for NASA Contract Nos. NAS8-30811 and NAS8-31547. This document also summarizes the efforts expended in testing, analyzing, and subsequent development of a meaningful definition of the Mean Number of Peak Pulses Before Failure (MP^2BF) levels of a family of transient voltage suppressor devices, the TransZorb® TVS. The period of this contract was in excess of two years, in which greater than 12,500,000 pulses were incurred by the devices under test. From the extensive data gathered in this study, meaningful reliability curves were developed to guide the engineer in optimizing component use for circuit protection and maximizing the long-term reliability criteria of the TransZorb TVS.

Test were performed over a very broad spectrum of stress starting at a low level of 25% of the maximum peak pulse current (I_{PP}) capability of the TransZorb TVS and increasing in increments of 25% up through 150% of the maximum I_{pp}. The device types used in this study were representative of the broad spectrum of voltage availability, including the 6.8V, 33V, 91V, and 190V types. A separate reliability curve for each device type was developed and is reported. The meaningfulness of the reliability curve (MP^2BF) has been extended to the maximum limit allowable under the number of pulses subjected to the components during the performance of these tests. In typical lightning environments, TransZorb TVSs will normally exhibit a life expectancy of grater than 20 years. The 50% peak current distribution ordinate for a lightning strike is 20kA while the 1% level, which is representative of worst case threat, is 140kA.[1] Failures at the 100% I_{PP} level were virtually total for all types in this study and subsequently, meaningful MP^2BF curves could be derived.

Test Efforts

Silicon avalanche suppressor devices have been on the market for many years; however, this is the first effort in the direction of gathering long-term reliability data under actual pulse test conditions. Since a TransZorb TVS normally operates in the standby mode conducting very little current, a meaningful measure of life expectancy for this type of device should simulate in-service conditions, which includes a reverse bias voltage upon which is superimposed a transient voltage waveform. The pulse waveform for this test had a ten microsecond virtual rise-time with a 1,000 microsecond exponential decay to one-half crest value. This is called a 10 x 1000 pulse. A sample of 50 devices from each voltage type were tested at each of six current levels, yielding a total of 300 devices for each of four voltage categories with a total of 1,200 parts. The components were mounted in a test rack equipped with a separate counter for each device which recorded the number of pulses incurred prior to failure. The peak pulse current test level for each of the TransZorb TVSs at the various test levels is shown in Table 1.

			Peak Pulse Current in Amperes			
Group	Sample Size	% Rated Ipp	1N5629A 6.8V	1N5645A 33V	1N5656A 91V	1N5665A 190V
1	50	25	35.75	8.25	3.0	1.45
2	50	50	71.5	16.5	6.0	2.9
3	50	75	107.2	24.75	9.0	4.35
4	50	100	143.0	33.0	12.0	5.8
5	50	125	178.7	41.25	15.0	7.25
6	50	150	214.5	49.5	18.0	8.70

TABLE 1
TransZorb TVS Pulse Exposure

Evaluation And Test Results

The tasks involved in the reduction of data, subsequent analysis, and development of the MP^2BF curves contained in this report were performed at the University of Arizona in Tucson, under the direction of Professor Edward B. Haugen.

The goal of this study was to obtain a meaningful analysis of each TransZorb type and also for the establishment of an MP^2BF curve for each voltage category and also to interpret the data as applicable for engineering use criteria.

An idealized curve plotting the percent of rated peak pulse current versus mean number of peak pulses before failure is shown in Figure 1. With a homogenous lot, a failure distribution curve could be obtained at each level, given a sufficient number of test pulses.

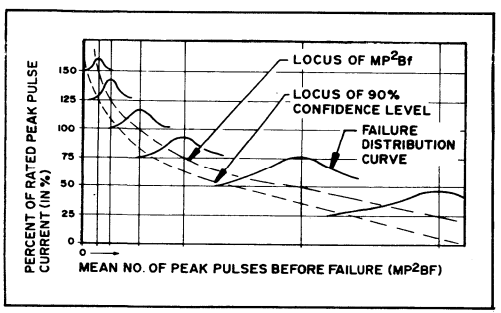

FIGURE 1
Loci of Mean Number of Peak Pulses to Failure and 90% Confidence Level for Ideal Case

For statistical purposes, there were insufficient failures in all lots with exception of the 100% I_{PP} and higher pulse current groups to be significant. Because of the insignificant failures at the 75% and lower peak pulse current levels, the MP^2BF curves shown in this report have a dotted line to represent the portion of the curve which is extrapolated and a solid line for the curve which is calculated.

Design Engineering Criteria

Results of data reduction for all pulse testing is shown in Figures 2 through 5. These four graphs depict the MP^2BF versus the percent of maximum rated I_{PP}. The device types 6.8V, 33V, 91V, and 190V are representative of the broad voltage spectrum in this device series. The curves were drawn to include the mean and 90% confidence levels for the types listed above. The solid line of the curves represents that which was derived from data while the dotted line was extrapolated and is based on more than 3,000,000 pulse tests for each curve, most of which did not result in device failure.

The TransZorb transient voltage suppressors were designed to protect voltage-sensitive elements from nonrepetitive transients. Since the TransZorb protector has been introduced, many requirements have been found for this protector device. Applications cover a broad spectrum of protection for electronic equipment containing sensitive electronic components.

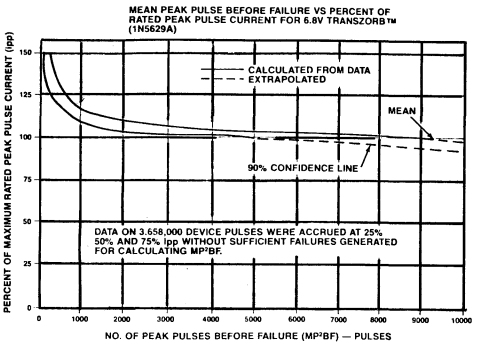

FIGURE 2
Summary For 6.8V TransZorb TVS (1N5629A)

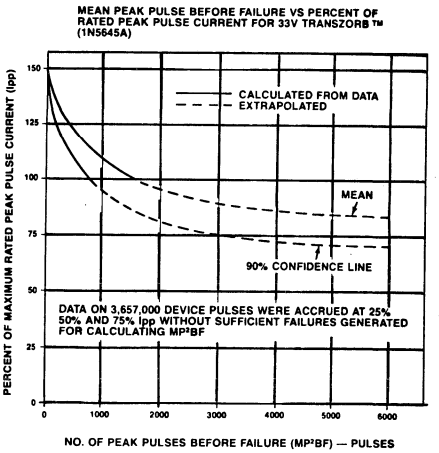

FIGURE 3
Summary For 33V TransZorb TVS (1N5645A)

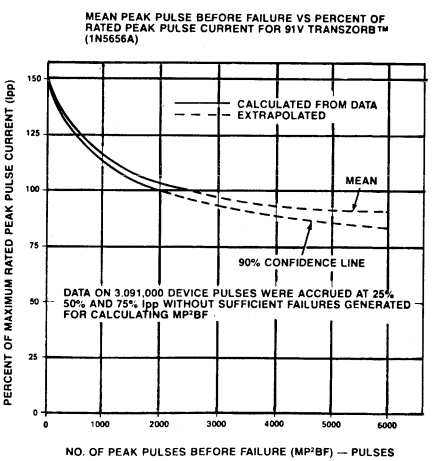

FIGURE 4
Summary For 90V TransZorb TVS (1N5656A)

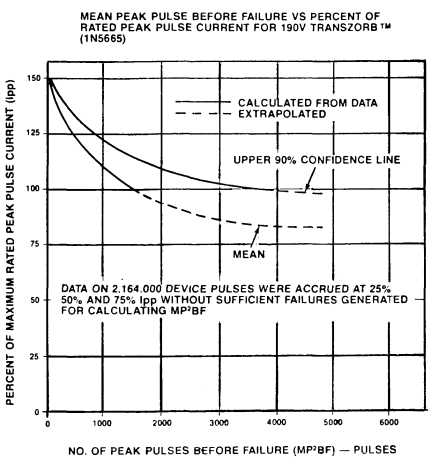

FIGURE 5
Summary For 190V TransZorb TVS (1N5665)

These vulnerable components include integrated circuits and MOS device types. Some ICs are destroyed by voltage spikes containing energies at the 100 microjoule level and some MOS devices are destroyed with transient energies less than 10 microjoules.[2][3] Most discrete semiconductors do not require the low-clamping voltage protection offered by solid state transient voltage suppressors because of their inherent hardness against some transient voltage. However, some power semiconductors, especially fast-switching transistors, can be quite vulnerable to fast rise time transient voltages, and these devices require transient voltage suppression in some circuits. The largest demand for transient voltage suppression is in the protection of microcircuits, which operate in the 6V, to 24V region. In observing the MP^2BF curves derived from this study, the lower voltage TransZorb TVSs appear to be more reliable, which is beneficial for microcircuit protection. The 6.8V TransZorb does offer some degree of protection at an I_{PP} level of 150% of the maximum rated value as shown in Figure 2.

Guidelines For TransZorb TVS Selection

The TransZorb TVS was initially designed for providing protection for telecommunication equipment from transient voltages resulting from induced lightning. Applications for TransZorb TVSs have substantially expanded to include many other areas of protection encompassing transient voltages generated by inductive switching, high-voltage disconnects, static discharge, and NEMP. In closed systems where voltage transients can be predicted and well defined, it is much easier to select a TransZorb TVS to protect the more sensitive elements of the system. General guidelines for selecting the right TransZorb TVS are listed below. Please refer to the data sheet in the back for optimum interpretation of these criteria.

dc Voltage Rating

- Determine the maximum dc or continuous operating voltage, which should be the nominal circuit voltage plus its tolerance on the high side. This should be the maximum voltage of the circuit.
- Select a TransZorb suppressor to have a reverse standoff voltage equal to or greater than the maximum circuit voltage, as defined in the paragraph immediately above. This selection will allow for operating over the temperature range of -65° to +175° C.

Pulse Rating

Define the waveshape or source of the transient and duration of the pulse. Determine the maximum peak pulse power of the transient. If the pulse decays exponentially, observe the pulse time for decay to 50% of the crest value.

- Check the peak pulse current on the data sheet to assure that the current of the pulse is within the maximum rating of the suppressor for a 10 x 1000 pulse. For example: 143A for the 1N5629A (6.8V), 100A for the 1N5633A (10V), and 19.5A for the 1N5651A (56V).
- If the pulse decays exponentially, but different than the 1 millisecond which is specified on the data sheet, check the chart entitled "Peak Pulse Power vs Pulse Time" for maximum Peak Power (P_P) for that particular pulse duration.
- If the pulse is a nonrepetitive square wave, derate the transient suppressor to 66% of the maximum value under exponential decay conditions. If the pulse is a nonrepetitive one-half sine wave, derate the suppressor peak pulse power to 75% of the maximum capability.
- If the pulse is a rapidly damped sine wave or rapidly damped square wave with one time constant of five cycles or less, rate the device the same as if it were subject to only one pulse, as defined in the paragraph above.

Stacking TransZorb TVSs For Higher Power

- If the incident P_P is greater than the rating of the TransZorb TVS, devices may be stacked in series to increase power rating for voltage levels usually above 20 volts. An example of this could be a 1.5kW, 100V TransZorb TVS, which is inadequate, and a 3kW peak power dissipation required. The most advantageous way to achieve this power level is to stack in series two each of a 50V±% TransZorb TVS. The total peak pulse power dissipation would then be twice that of a 1.5kW device, or 3kW. Stacking three each of a 33V±5% device would yield a 4.5 kW peak pulse power and stacking 4 each of the 25V±5% device would give a peak pulse power of 6kW. TransZorb TVSs can be stacked almost without limit.

  In practice, TransZorb TVSs have been stacked in excess of 180 devices with good reliability. However, 5% tolerance devices of the same voltage must be used to insure even loading of the devices. When the power rating is doubled, notice that the current rating is doubled also.

- If it is impossible to achieve the necessary power rating by stacking the devices in series, parallel stacking can be done effectively for voltages below 40V. Close matching, about 100mV or less between each device, is necessary to assure even loading of the transient power between the suppressors. This is usually done at the factory for optimum results.

Clamping Voltages

Observe that the maximum clamping voltage is 1.33 x the breakdown voltage. If this maximum clamping voltage exceeds the circuit limitations, devices can be derated to reduce the clamping factor. For example, two devices in series have a clamping factor of approximately 1.2 as compared to the clamping factor of 1.3 for a single device.

High Frequency Applications

If the suppressor is used on dc or low frequency signal lines, the capacitance of the suppressor will not attenuate or alter the circuit conditions. However, if the frequency is quite high, and insertion loss occurs, methods of effectively reducing capacitance by adding low capacitance diodes in series have been developed.

Static discharge has a rise time of the order of 1 to 2 kilovolts per nanosecond[4]. This fast rise-time voltage front presents some unique problems in providing adequate protection. What would seem to be a relatively short length of wire in the TransZorb circuit between the protected line and ground may produce a large secondary or overshoot voltage. Voltage produced by inductive effect is expressed as:

$$V_{(t)} = L\ di/dt$$

where L is inductance in Henrys
di/dt is time rate change of current

Conclusion

In excess of 12,500,000 total pulses were gathered on 1,200 TransZorbs to derive the MP^2BF curves shown in Figures 2 through 5. Each device was pulsed for a total of 25,760 pulses maximum or until failure occurred. This magnitude of testing appeared to be sufficient to describe the reliability of the device at 100% peak pulse current level and above. Additional testing would be required to define an accurate and meaningful reliability at lower peak pulse current levels in excess of 25,760 pulses.

From analyzing the devices which failed, it was observed that all components failed in a shorted mode, which was expected. There appears to be no method of predetermining device failure by some electrical parameter, such as reverse leakage current. All parameters remained quite stable throughout the duration of the test.

References

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(2) E. Van Keuren, "Effects of EMP Induced Evaluation on Integrated Circuits", IEEE EMC Symposium Record, 65CH1002-5EMC, October, 1975.

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(4) T. J. Tucker, "Spark Initiation Requirements of a Secondary Explosive", Annals of the New York Academy of Sciences, Vol. 152, Article I, P. 643-653, October, 1968.

LIGHTNING PROTECTION FOR COMPUTER DATA LINES

by
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Presented at the Electrical Overstress/Electrostatic Discharge Symposium. September 22-23, 1981, Las Vegas, Nevada.

Summary

Data terminals and computer main frames are failing with increasing frequency from lightning caused transient voltages on communication lines. This is directly related to a higher degree of IC miniaturization and increasing use of longer data lines. Even when acceptable shielding practices and grounding procedures are employed, lightning caused failures still occur.

A successful method of suppressing transient voltages has been developed by General Semiconductor Industries. Inc. This approach employs a gas surge arrestor to conduct the high current components and a specialized low clamping silicon transient voltage suppressor to clip the fast rising peak voltages, thus uitilizing the main advantages of each device type. This method is compatible with both 20mA loops and EIA STD RS232C. Suppression capability of this circuit is illustrated under severe transient voltage stress. Also, some case studies are reviewed in this paper.

Lightning Threat

Occurrence

Lightning, frequently present in rainstorms, has also been observed in dust storms, snow storms, and even on some occasions as a "bolt out of the blue". In the U.S., the greatest activity is in the southeast with up to 100 thunderstorm days per year occuring in southern Florida, as shown in Figure 1[1]. Activity decreases to about 50 per year in the midwest and tapers off to about 10 on the west coast. Bear in mind that this map represents a statistical average and may not necessarily reflect yearly activity. Also, lightning activity is not necessarily related only to thunderstorm days per year. Storms in Southern Florida and the southwest often consist of a few convective thunderstorm cells and last one to one and one-half hours, while most of the lightning activity in the midwest is caused by weather fronts and is likely to be more intense with storms lasting up to three hours.

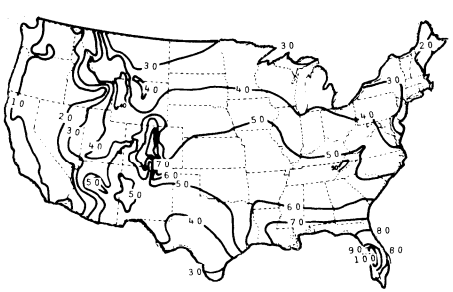

FIGURE 1
Mean Number Of Thunderstorm Days Per Year

Magnitude Of Lightning

The distribution of peak lightning currents reported by N. Cianos and E. T. Pierce[2], shown in Figure 2, ranges from a few kiloamperes to more than 150 kiloamperes with the mean value at about 20 kiloamperes. Although the probability of a direct strike is very low, electromagnetic coupling is real. with one of the primary factors being field strength. The radiated field strength[3], normalized to a distance of 10 kilometers, is shown in Figure 3. Lightning is complex, hence the broad range of frequencies. The peak level of 2-3 volt per meter for a strike at 10km distance can be in excess of 100V/m for a close proximity strike. A 100m communication cable interconnecting a terminal with a mainframe can incur lightning induced potential levels of several hundreds of volts, thus causing failure of line interfacing components.

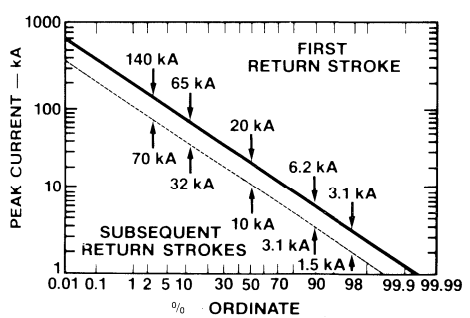

FIGURE 2
Distribution Of Peak Lightning Currents

4

APPLICATION NOTES

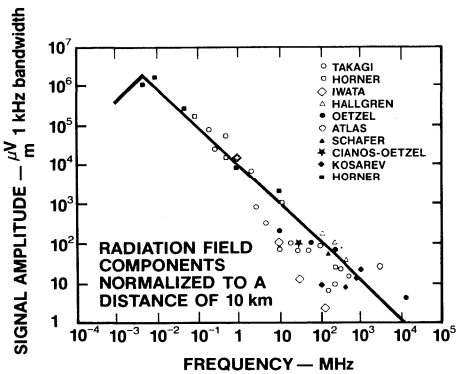

FIGURE 3
Radiated Field Strength Of Lightning

Component Failure

Failure Threshold Levels

The increasing complexity of integrated circuit chips has dictated that each component on that chip be smaller with the result that the failure threshold is also quite low. Most ICs fail at transient energies below 100 microjoules. Failure threshold voltage levels of some devices have been reported by Van Keuren[4] and are shown in Table 1.

TABLE 1
Minimum Failure Thresholds of CMOS and TTL

Device Type	Pulse Width					
	20*u*sec	2*u*sec	1*u*sec	0.2*u*sec	.1*u*sec	.025*u*sec
55107	22V	16V		22V		
55109	36V	38V		60V		
5404			30V		50V	120V
54L30			20V		50V	90V

Failure Mechanisms

The bipolar structured devices used for line drivers and line receivers have been observed to fail at levels between 40V and 100V from lightning transients, with the drivers being generally less susceptible than the receivers. Factors relating to failure, in addition to device type, can include manufacturer and lot. Micrographs of the failed area of a type SN1488 line driver is shown in Figure 4. The output resistor failed short and melted through to the metalized overlays. The failure area of a SN1489 line receiver is shown in Figure 5. Arc traces across the input resistor and the input transistor contacts can be seen as thin white lines. This device type must operate at levels of up to 25V on computer equipment per EIA STD RS232C; however it can fail at a level of only 40V. This leaves a relatively narrow window of 15V for protector standby and clamping operation.

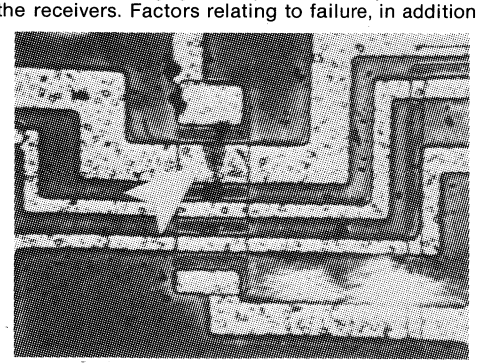

FIGURE 4 Shorted SN1488 Line Driver

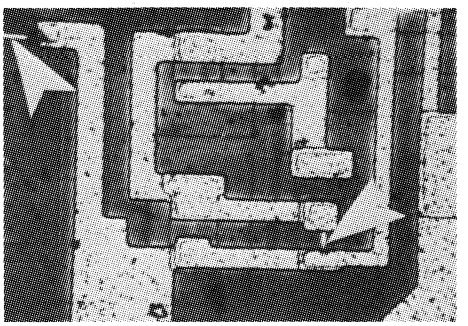

FIGURE 5
Shorted 1489 Line Receiver

Suppression Methods

Suppression Options

Components often used for reducing transient levels include LC and RC networks, thyrite units and metal oxide varistors. These are "soft" limiters in that there is no avalanche breakdown experienced. Hard limiters which include gas surge arrestors and silicon transient suppressors have lower dynamic resistance in the "On" or conduction stage. The gas arrestor requires an impulse voltage up to 1500V, depending on the wave front, to initiate conduction or "fire" the device. Silicon transient voltage suppressors go into conduction as soon as avalanche breakdown is attained. Zener diodes are unsuitable for this application because they are not designed for suppression and have not been tested for long term reliability as have silicon transient voltage suppressors[5].

As one peruses the list of options for protecting data lines, there appears to be no single part that has all the desired requirements which include:

Fast response time
High current conduction
Low clamping voltage

A combination of two devices, the gas surge arrestor and the silicon transient voltage suppressor, both being hard limiters, appears to provide these requirements based on laboratory tests and field experience. These are combined as shown in Figure 6.

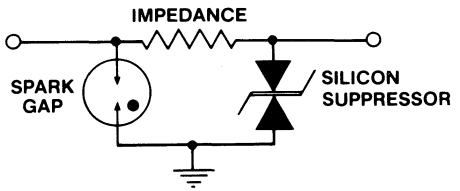

FIGURE 6
Data Line Protector Circuit

This approach may have been around for more than a quarter century, having been patented by David Bodle of Bell Telephone Laboratories in the mid '50's; however, careful selection and layout of components has been found necessary to enhance performance in providing protection and reliability as well as system compatibility. Installation is also very important.

Circuit Performance

For RS232C data line requirements, a low impulse striking voltage rating is desired in selecting the gas surge arrestor. The impedance element is selected for adequate power dissipation and with an IR drop high enough to develop the impulse striking voltage of the gas arrestor. The gas arrestor must fire to divert the large bulk of the surge current. A silicon transient votage suppressor, such as the Siemens TAZ™ or General Semiconductor's TransZorb® TVS, is selected for a 25V operating level with a maximum clamping level of 40V. In addition to appropriate selection of components, the mechanical layout must include factors such as shortest possible lead lengths of protector components and low impedance ground paths.

Protection capability of the protector circuit described above is illustrated in Figures 7, 8 and 9 below. An incident peak pulse current of 150A, 1.2 x 50μsec (1.2μsec rise, 50μsec decay to one-half crest value) having a peak voltage of 1200V was applied with a Keytek Model 424 surge generator. The pulse was clamped to a level of about 34V, well below the failure threshold of line receivers, as shown in Figure 7. A Tektronix 7834 scope was used for monitoring. With the same equipment, the clamping of a 500A, 1500V pulse to a level of about 37V is shown in Figure 8. The effectiveness of this circuit is further illustrated in the low 35V clamping of a 1000A, 1000V, 8 x 20μsec high energy pulse as shown in Figure 9.

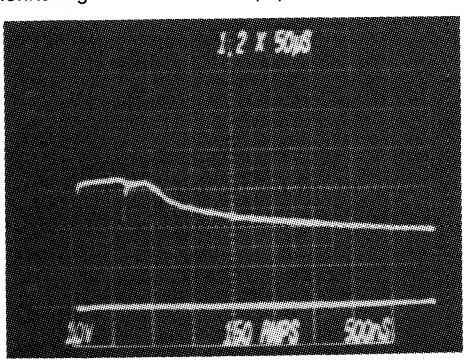

FIGURE 7
Clamping Voltage At 150A
Horizontal: 500nsec/div.; Vertical: 10V/div.

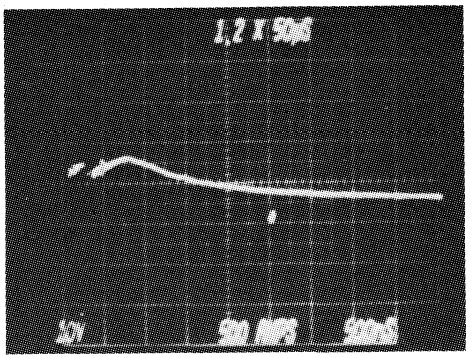

FIGURE 8
Clamping Voltage At 500A
Horizontal: 500nsec/div.; Vertical: 10V/div.

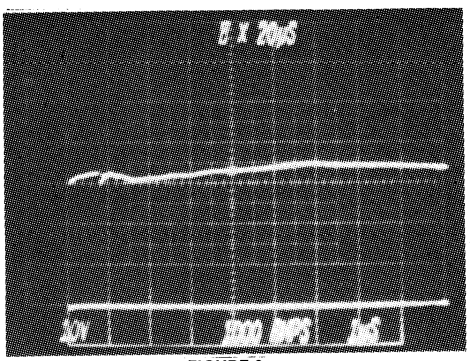

FIGURE 9
Clamping Voltage At 1000A
Horizontal: 1μsec/div.; Vertical: 10V/div.

The probability is very low that a single wire from a data line will incur a 1,000A transient; however, if this does occur, the suppressor is capable of providing adequate protection.

Protector Configurations

Most data lines have three or four individual wires to be protected for both differential and common mode lightning transients. As a minimum, these include transmit, receive and data ground. The protection components for these lines are mounted on a single circuit board. This provides short ground interconnections for effective differential mode protection which is achieved through the ground bus on each circuit board. A four wire data line protector is shown in Figure 10. This design was customized to provide for two unprotected lines. The wide low impedance ground bus can be seen through the laminate at the bottom of the card. These cards are usually mounted in groups of up to four or up to eight in a single housing with 25-pin RS232C connectors at both entry and exit. An eight line protector is shown in Figure 11. The box and cover are cast aluminum for rigidity, conductivity and shielding.

TransZorb® Trademark of General Semiconductor Industries, Inc. TAZ™ Trademark of Siemens Corporation.

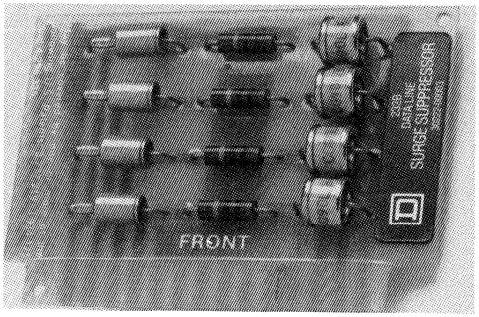

FIGURE 10
Data Line Protector

This enclosure is designed to be mounted at building entry points or in close proximity to the computer mainframe providing there is adequate shielding of incoming lines. The 25-pin sockets at both entry and exit of the box reduce installation time. A one-fourth inch threaded stud provides for ground wire attachment, which should be as short as possible to a low resistance earth ground. It is very important to have a good path for the lightning transient to earth ground, preferably with the protector mounted at the building entry.

Some installations have data terminals and line printers located at substantial distances from the entry protectors. This may result in lightning induced transients from close proximity strikes if the site is not well shielded, such as in older buildings or frame structures. A supplementary data terminal protector of the type shown in Figure 12 can be used to provide an extra margin of safety. This configuration contains 25-pin connectors at each end to interface between the data line and the terminal or line printer. In the plug, which attaches to the equipment, each of the lines are protected to a common point with a silicon transient suppressor. The common point is then tied to earth ground through a short 16 gauge stranded wire which is connected to the nearest suitable attachment.

FIGURE 11
An Eight Line Protector

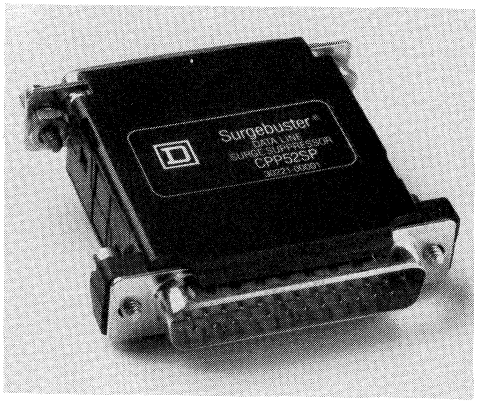

FIGURE 12
Data Terminal Protector

Installation

For optimum effectiveness, the protectors should be placed at the data line entry points. Transient voltages should be kept out of the building because they may inadvertently couple into vulnerable circuitry. If this is not feasible, magnetically shielded lines should be brought to the protector system. An example of an installation at the computer center in a relatively large installation is shown in Figure 13.

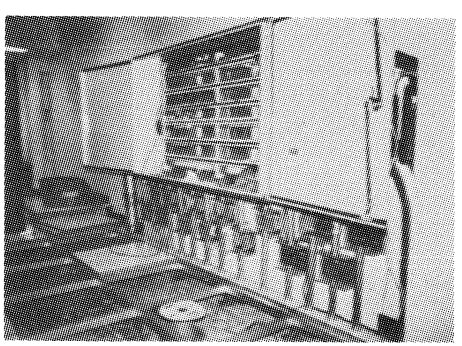

FIGURE 13
Computer Protector Installation

This protector system, in the process of being installed, contains more than 100 line protectors which interface with seven structures up to 500m distant. The large cabinet contains terminal posts and provides for flexibility in attachment of remote terminals. Eight position data line protectors are mounted below the entry cabinet. A closeup of this protector installation is shown in Figure 14.

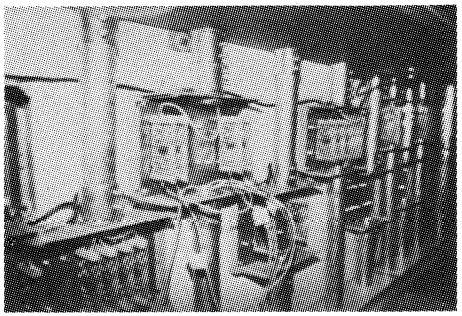

FIGURE 14
Protector Installation Closeup

The view shows the open protector boxes with individual line boards at various stages of installation. A one-fourth inch threaded stud provides a ground connection to each box. A stranded No. 6 AWG wire is daisy-chained to each box then attached to the computer common point ground rod.

Protectors for several remote terminals in a building located 60m away were installed within a large power distribution box as shown in Figure 15.

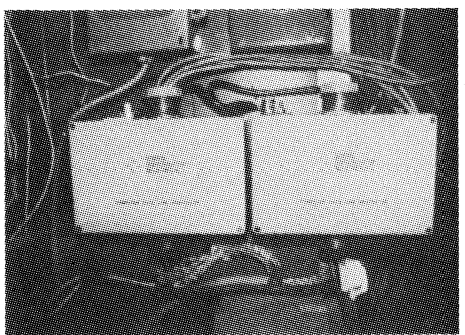

FIGURE 15
Remote Terminal Protector Installation

Entry from outside lines is at the bottom of the protector housing with exit lines (upper) feeding to the remote data terminals. The heavy guage ground wire is seen at the top.

Another protector installation for remote terminals is shown in Figure 16.

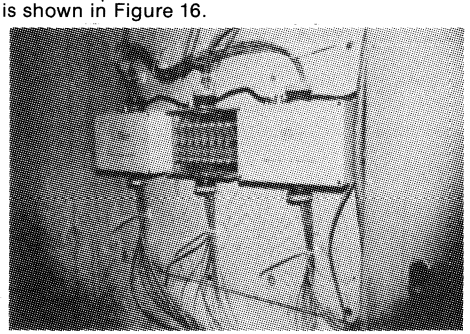

FIGURE 16
Remote Terminal And Line Printer Protection

This group of three units protects twenty-four terminals and line printers. Mounting location is in the building basement adjacent to the power service entrance. One of the box covers has been removed in this photo to illustrate mounting of the individual line protector circuit boards. Earth ground for this and other installations is achieved through both bonding to power ground and also to a separate driven ground rod.

The supplementary protection for remote equipment which interfaces the data line and the terminal (Ref. Figure 12) is illustrated in Figure 17. For neatness, the excess length of data line is coiled and tied at both the equipment and a nearby wall as shown in the lower right of the picture.

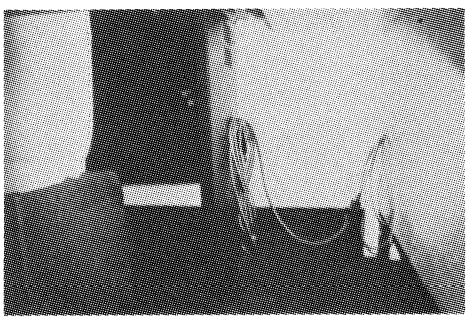

FIGURE 17
Data Terminal Protector

Case Histories

The history of three installations has been closely followed both before and after data line suppressors. A summary of the important details are reviewed in the following paragraphs.

Case I

This protector system was installed during an expansion program in which three new terminals were located in a building structure approximately 100m from the computer mainframe. One of the data line protectors (Ref. Figure 10) was installed at the building entry points on each of the three line terminations. Low impedance ground paths were provided by 2 to 3m of heavy guage wire to a driven ground. This was a new installation, hence, there is no previous failure history. After six weeks of service in which three severe thunderstorms occured, no failures were experienced.

Case II

Protectors were installed as a retrofit at this installation after frequent lightning caused outages on three remote terminals and the corresponding computer ports. The computer user was threatened with service contract cancellation because of high maintenance costs since failure occured with each thunderstrom if the equipment was not disconnected from the data line. It was a practice to "unplug" the remote lines when a thunderstorm appeared in the vicinity and at the end of the workday. Unfortunately, this was not always observed.

Data line protectors were mounted at entry points to both buildings and additional protection pro-

vided by installing data terminal protection plugs as illustrated in Figure 17. This site, located in the mid-south thunderstorm belt, was also provided with low impedance ground paths; 2m of heavy gauge wire to a driven ground at each entry point protector. After installation of the lightning protectors, a minimum of two thunderstorms per week have occurred over a 7 week period without lightning caused failures.

Case III *

This one is more complex that the previous two as it includes 120 data lines interconnecting 7 separate structures. During the previous three years of operation, an estimated annual cost of repairs caused by lightning was approximately $30,000. This excludes the inconvenience and work backlog buildup during the times when the equipment was inoperative.

During the first week of June, 1981, one building with 5 terminals was retrofitted and shortly thereafter weathered a very active storm with no resulting failures. With these encouraging results, full scale efforts were made on the balance of the installation. Six weeks later, two terminals out of three in the same location failed during a severe storm. An investigation showed that the ground path had a high impedance which could contribute to this failure. One week later, a storm in which direct strikes were apparently sustained by at least two structures, 9 out of 50 protected terminals failed and 3 computer input ports were damaged.

A close examination of the site revealed that the failure causes were in the following three categories:

1. Inadequate grounding
2. Insufficient bonding
3. Inductive coupling

Inadequate grounding is being corrected by reducing the length of ground wire runs and also bonding to convenient power grounds which will reduce the ground impedance of the protector boxes at building entry points. Differential and common mode protection was being provided to the remote terminal inputs; however, common mode with respect to the power ground was inadequate. This is being corrected by bonding the ac power ground to the protector ground with 3-5 ft. of 14 gauge wire. Entry cables which still contain transients are being routed away from the suppressed lines with separation of 1 ft. minimum to minimize inductive coupling onto vulnerable circuits.

After the corrective measures discussed are completed, and the system is back "on-line" during thunderstorms, the performance will be observed for lightning caused transient voltages.

*Note: There were no failures attributable to lightning during the five-year period following this retrofit.

Conclusion

Computer systems can now be reliably protected from lightning caused transients voltages with carefully selected and fabricated combinations of gas surge arrestors and silicon transient suppressors. To make these protectors effective, a few fundamental precautionary measures must be observed. These include short distance, low impedance paths to ground and physical separation of the protected data lines from the unprotected lines.

Some installations will present a greater challenge than others due to complexity and the difficulties associated with retrofitting a system while attempting to maintain normal computer operation. However, the protection methods described above have inherent flexible design characteristics which simplify both older and new systems installations.

Placement of protectors at cable-building entry points offers optimum protection in diverting transient currents to ground before communication lines enter the building. Short grounding wires of less than 3m to a low resistance driven ground or power ground are required to optimize low impedance to earth ground. For units protecting remote terminals and line printers, the protector ground must be tied to power ground at the protected terminal to minimize differential voltages between communication and power sections of the equipment.

Although a totally protected system may not provide complete protection from a direct strike, such events have a low probability of occurence. But for all other close by strikes, which would normally be disastrous to a computer system, the protection performs its function of diverting transient voltages harmlessly to ground.

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3. Cianos and Pierce, Page 105.
4. E. Van Keuren, "Effects of EMP Induced Transients on Integrated Circuits," IEEE Electromagnetic Compatibility Symposium Record, 75CH1002-5 EMC, 1975.
5. O. Melville Clark, "Surge Life of Transient Voltage Suppressor" (Final Report), Performed Under Contract No. NAS8-31547 for George C. Marshall Space Flight Center, May, 1977.

EFFECT OF LEAD WIRE LENGTHS ON PROTECTOR CLAMPING VOLTAGES

by
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Originally presented at the Federal Aviation Administration-Florida Institute of Technology Workshop on Grounding and Lightning Technology March, 1979—Melbourne, Florida

Abstract

Under high current pulse conditions, excessive lead lengths on suppressor components can be responsible for destruction of the protected circuit. This is caused by voltage build-up across the small but finite amount of inductance in the interconnecting leads of the protector. Some suppressor devices have been tested and observed to have more than twice the specified clamping voltage which was subsequently shown to be caused by inductive effects. Problems and corrective measures are illustrated and discussed in this paper.

SEMICONDUCTOR FAILURE THRESHOLDS

MOS and small area geometry semiconductors are particularly vulnerable to the effects of transient voltages. Unfortunately there has been very little information published on this subject. The work reported by Van Keuren[1] illustrates how fragile CMOS and TTL devices can be. Minimum failure pulse voltage thresholds are shown in Table I.

Electrostatic Discharge (ESD) failures of MOS microcircuits have been measured by Gallace and Pujol[2]. Comparisons among several suppliers indicate that failure levels can be a function of manufacturing technique. Repeated step stressing of a sample of 25 CD4011AF type devices shows that at a given stress level devices would eventually fail, as shown in Figure 1.

TABLE I
Minimum Failure Threseholds of CMOS and TTL

Device Type	Pulse Width					
	20μsec	2μsec	1μsec	0.2μsec	0.1μsec	.025μsec
55107	22V	16V		22V		
55109	36V	38V		60V		
5404			30V		50V	120V
54L30			20V		50V	90V

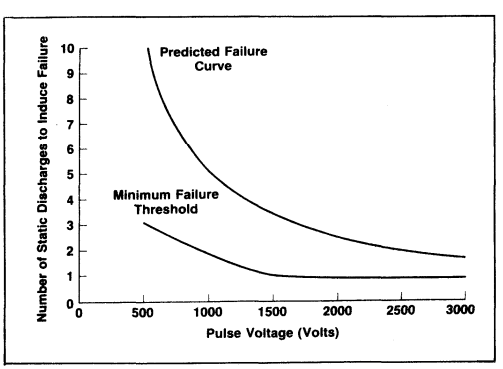


FIGURE 1—Stress Failure of CD4011F

EQUIVALENT CIRCUIT OF PROTECTOR

The eqivalent circuit of a silicon transient suppressor, such as the TransZorb® TVS which is manufactured by General Semiconductor Industries, is shown in Figure 2. All parameter values are fixed by manufacturing processes and device construction except L_1, the inductance resulting from the lead wires connecting the protector across the circuit for which protection is intended. Normal wiring practice results in lead lengths of the order of centimeters. In some power installations this has been observed to be of the order of feet.

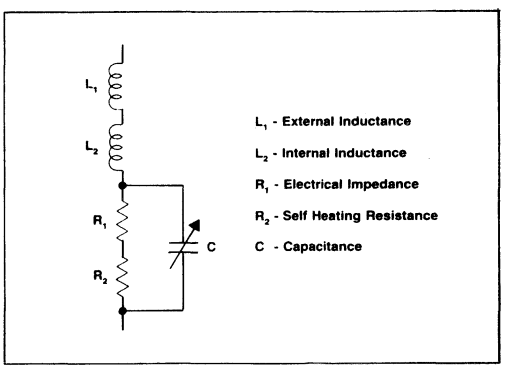


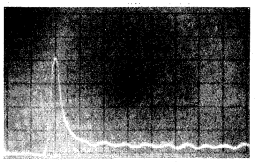
FIGURE 2—Equivalent Circuit of Protector

The inductance within an axial leaded part, as represented by L_2, is of the order of 10^{-8} henrys while the inductance within a modular assembly can be one to two orders of magnitude greater, depending on the design and the number of subcomponents. The capacitance of a silicon avalanche suppressor can vary over an order of magnitude, depending on the degree of reverse biasing.

TRANSIENT VOLTAGE RISE-TIMES

a. **EMP:** Voltage rise-times of EMP (Electromagnetic Pulse) transients, as generated by high altitude nuclear detonations, are 5kV/nsec. The presence of even a small amount of inductance in the protector

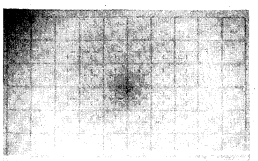
circuit can have very profound results on the effectiveness of a protector device. This is illustrated with the oscillographs in Figures 3 and 4.



Vert: 200V/div.

Horiz: 10nsec/div.

FIGURE 3— 7.5 cm Lead Wires



Vert: 200V/div.

Horiz: 10nsec/div.

FIGURE 4—Zero Length Lead Wires

In Figure 3, a 30V TransZorb TVS in the DO-13 package was pulsed with a 100A 4kV/nsec rise-time transient. With 7.5 cm leads on each end, at which current was injected and voltage measured, the overshoot voltage is slightly greater than 800V. The energy under this curve is calculated to be 70μjoules, sufficient energy to destroy most types of MOS and some TTL devices. By reducing the lead length to zero and repeating the pulsing, the overshoot voltage is reduced to about 200V. The energy under this curve is less than 1μjoule, below the destruct threshold of MOS and TTL devices.

b. **Lightning and Inductive Switching:** From measurements made on 120V ac power systems, Martzloff[3] has proposed a waveform with a frequency of 100kH. The lightning stroke, which is usually reported with current rise-times ranging from 1 to 3μsec has been more recently measured by Llewellyn[4] to be as low as 500nsec. Transients on shipboard ac power systems have been defined by MIL-STD-1339 as having transient rise-times of 1.5μsec.

Normal wiring practices are usually considered adequate for protection of electronic circuitry. "Normal" and "adequate" are relative terms and usually prevail under conditions in which equipment performance is acceptable. What is normal and adequate protection for vacuum tubes is not the same for power semiconductor devices. Protection for microcircuits is also quite different from power semiconductors. With increased usage of microprocessors and other small area geometry semiconductors, equipment is becoming more vulnerable to transient voltages, under both single pulse and repetitive pulse conditions.

INDUCTIVE EFFECTS IN COMPONENT LEADS

a. **Calculation:** The inductance in a straight wire appears, at first glance, to be very small and insignificant. Assuming a value of 1μH/m for a straight wire, most lead wires have inductance values in the nanohenry region. The voltage drop developed across an inductor under pulse conditions is expressed as:

$$V_{(t)} = L \frac{di}{dt}$$

where L is inductance in henrys

$\frac{di}{dt}$ is the rate change of current

For the fast rise-times of EMP as shown above, the associated problems are obvious; however, for the slower rise-time of switching and induced lightning the degree of exposure and protection required can be defined only after carefully studying all boundary conditions.

b. **Case Study:** In the following application, a silicon transient suppressor is being used to both regulate the voltage to power a telecommunications repeater and also provide transient suppression. The schematic is shown in Figure 5. This is one of two repeaters powered and protected by the same component.

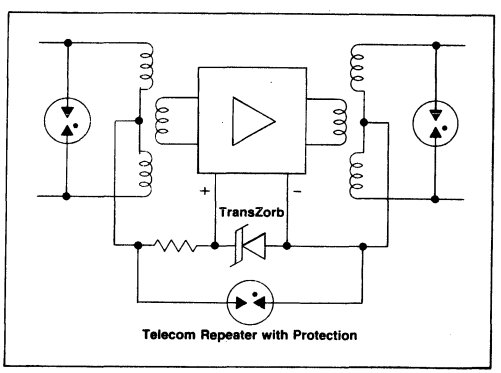


FIGURE 5—Telecom Repeater With Protection

The microcircuitry used in this equipment has some well defined failure levels; 20V in the positive direction and 6.5V in the negative direction. The suppressor has a well defined clamping voltage in the avalanche direction under a specified rise-time. The forward polarity measurements are specified at 100A with an 8.4 msec, ½ sine wave pulse. To determine higher current capability, pulse tests were made with a 1.2 x 50μsec waveform. During the process of taking data, small differences in lead length in the protection circuit were observed to have profound effects on the suppression capability of the device. Measurements extended over the range from 100A to 500A with lead lengths from the body of the device of zero, 1.0 cm and 2.0 cm. Tests were made on a molded 1.5kW TransZorb®. The peak clamping voltage was plotted against pulse current as shown in Figure 6.

After tests were made with zero, 1.0 cm and 2.0 cm lead lengths, the plastic body was carefully cut away leaving only the cell containing the junction and the leads. Voltage measurements were then made across

the cell, virtually eliminating inductance within the package. A lead length of 2 cm has a peak clamping voltage of 4V at 100A and 13.5V at 500A. By contrast, the cell only has a peak clamping voltage of 1.3V at 100A and 3V at 500A. Voltage probe placement for taking measurements is shown in Figure 7.

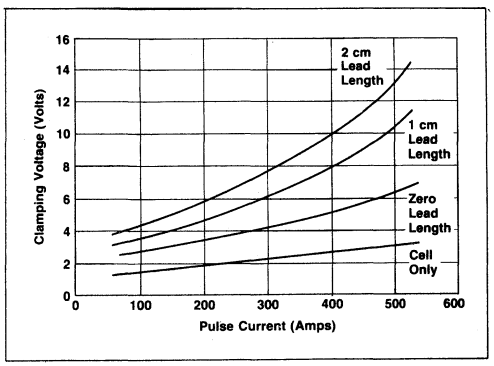


FIGURE 6—Clamping Voltage vs Pulse Current

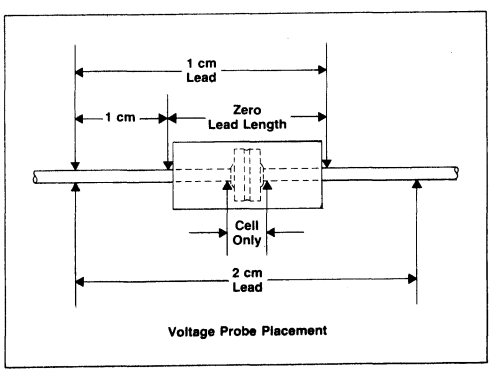


FIGURE 7—Voltage Probe Placement

Voltage drops across the lead wires contributing to peak clamping voltage can be attributed to both resistive and inductive components. Calculations were made for both resistive and inductive voltage drops for a 1.0 cm .040 in. dia. copper wire at pulse current levles from 100A to 500A. Rise-time is 1.2μsec. This data is shown in Table II.

TABLE II
Pulse Current Level and Voltage Drop

Pulse Current (Amps)	Measured Voltage Drop (Volts)	Calculated Resistive Voltage Drop (Volts)	Calculated Inductive Voltage Drop (Volts
100	.75	.019	0.83
200	1.3	.038	1.66
350	2.3	.066	2.91
500	3.3	.095	4.16

Note that the calculated inductive voltage drop compares favorably with the measured voltage drop while the resistive component contributes less than 10% of the total.

CLAMPING VOLTAGE OF AC PROTECTOR

In power systems, it is quite easy to place a modular assembly protector in a convenient mounting location rather than the most effective one, especially in retrofit applications. These components are sometimes bulky and do not always conveniently fit the desired location. To illustrate reduced effectiveness in an ac power transient suppressor, a module was measured for peak clamping voltage having lead lengths of 24 in., 48 in., and 72 in. Pulse currents were 100A, 200A, 300A and 400A with a waveform of 1.2 x 50μsec. Lead length vs additive peak clamping voltage plotted here is that value above the normal clamping voltage with zero lead length.

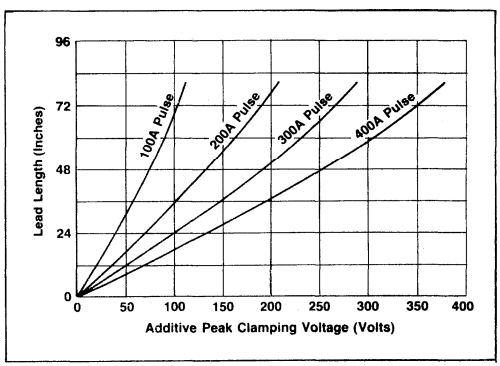
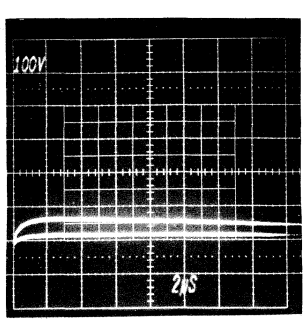


FIGURE 8—Lead Length vs Clamping Voltage

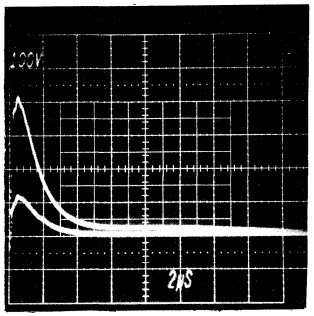
Note that the additive clamping voltage can be down in the range of 35V at 100A for 24 in. leads extending up to 350V at 400A for 72 in. leads. An oscillograph depicting optimum protection at 100A and 400A is shown in Figure 9. The 100A pulse is being clamped at about 215V and 400A pulse at 265V. The peak clamping voltage is substantially increased by the inductive effects of 72 in. leads as shown in Figure 10. In this oscillograph, the 100A pulse produced a peak of about 320V and 400A pulse produced a peak of about 615V. The inductive overshoot illustrated in Figure 10 is quite profound by comparison with Figure 9.



Vert: 100V/div.

Horiz: 2μsec/div.

FIGURE 9—AC Protector, Optimum Protection



Vert: 100V/div.

Horiz: 2μsec/div.

FIGURE 10—AC Protector, 72 in. Leads

CLAMPING VOLTAGE OF MICROCIRCUIT PROTECTOR

An ICT-5 type TransZorb TVS , designed for protecting low voltage logic circuits, was pulsed at levels of 100A, 200A, 300A, 400A and 500A with a 1.2 x 50μsec waveform. Voltage drop was measured across the leads at distances of zero, 1.0 cm and 2.0 cm from the body of the package, adding a total of 4.0 cm .030 dia. straight wire contributing to inductance and subsequently adding to the peak clamping voltage. A graph plotting total lead length vs. peak clamping voltage is shown in Figure 11.

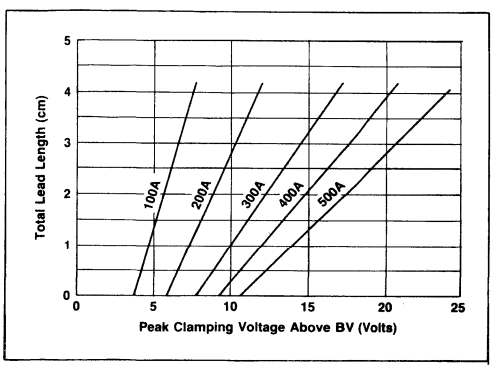


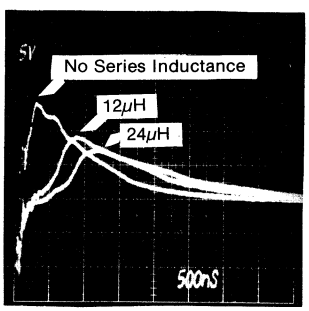
FIGURE 11—Lead Length vs. Peak Clamping Voltage

These curves are plotted as additive above the breakdown voltage (BV) at 1mA, which was 6.3V for the device tested. The clamping voltages increase with pulse current using zero lead length due both to the electrical impedance and thermal self-heating effect on the silicon pn junction. Observe that the clamping voltage covers a very broad range, from 3.6V above BV to 24V above BV depending on peak current and insertion method.

REDUCING INDUCTIVE EFFECTS

The most obvious method of reducing inductive effects and thus optimizing protector capability is to reduce lead wire lengths in the protector circuit. If it is not possible to reduce the conductor length, other options are available. Inductance in a given length of conductor can be reduced by replacing a small diameter wire with a wide strip conductor. On circuit boards, a ground plane on one or both sides of the board has been used by the author as a method for optimizing protector clamping.

Since voltage drop across the lead length is a function of the transient rise-time, it may be feasible to add series inductance between the transient source and the protector to reduce the rise-time and subsequently the peak clamping voltage. A TransZorb® used for 5V logic protection was tested with a 300A pulse having a 1.2 x 50μsec waveform with voltage measurements made at 2.0 cm from each end of the body of the device. This is shown in Figure 12, peaking at 24V. Placing a 12μH choke ahead of the suppressor to reduce the rise-time, reduced the peak to 19V and using 24μH reduced the peak to 17V. These curves are also shown in Figure 12.



Vert: 5V/div.

Horiz: 500nsec/div.

FIGURE 12—Comparitive Clamping Voltages

CONCLUSION

Inductive effects can be, and often are, a source of abnormally high peak clamping voltages compared to the inherent capability of a transient voltage suppressor. These high clamping voltages can cause failure of vulnerable electronic components; thus a suppressor capable of providing adequate protection can be rendered useless due to poor insertion methods. So it behooves the design engineers working on both mechanical layout and circuit design to be acutely aware of inductive effects and the problems which they can cause along with corrective measures in order to optimize transient voltage protector components.

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AC Power Line Protection For An IEEE 587 Class B Environment

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Tempe, Arizona

Abstract

The 587B series of protectors are unique low clamping voltage transient suppressors to protect ac powered equipment from the 6000V peak open circuit voltage and 3000A short circuit current as defined in IEEE Standard 587 for Category B transients. The devices, which incorporate multiple stage solid state protector components, have been specifically designed to operate under multiple exposures to maximum threat levels in this severe environment. The output voltage peaks are limited to 350V under maximum threat conditions for a 120V ac power line, thus providing adequate protection to vulnerable electronic equipment. The principle of operation and test performance data is discussed.

Introduction

As electronic systems become more sophisticated and make use of the newer higher density integrated circuits, their transient vulnerability increases. Equipment manufacturers are becoming increasingly aware that equipment must be designed to survive in a transient environment. Transient problems should not be left for the user to solve, but unfortunately, this has often been the case. The user is ill equipped for the task because he usually does not know system limitations or have the necessary test equipment to personally evaluate the plethora of protective devices available.

The IEEE 587-1980 Standard is a reasonable worst case definition of the transient environment[1]. By preceding equipment with a suppression network which reduces such transients to a specified maximum level, designers can insure that equipment malfunction or damage will rarely occur.

Topics to be discussed include the IEEE 587 Standard, suppressor design approaches, and test results of a suppressor module designed to protect equipment from the IEEE 587 transient environment.

The Transient Environment As Defined By The IEEE Standard 587

Several years of work by many people on IEEE committees has culminated in the publication of Standard 587-1980 which describes transient conditions occurring in low voltage (less than 600 volts) ac power circuits. It addresses transient voltages which exceed twice the peak operating voltage with durations ranging from a fraction of a microsecond to a millisecond, and originating primarily from system switching and lightning effects. The standard also proposes tests which approximate the real-world transient conditions for the purpose of evaluating the survival capability of equipment connected to power circuits.

Three location categories are defined: "A" and "B" for indoor applications, and "C" for outdoor applications. The location categories are further defined in Figure 1. They take into consideration the increase in source impedance from the outside to locations well within the building. Table 1 summarizes the test waveforms used for categories A and B, which are primarily for indoor residential, commercial and light industrial applications. The waveforms are detailed in Figure 2.

Location Categories

A. Outlets and Long Branch Circuits

All outlets at more than 10 m (30 ft) from Category B with wires #14—10

All outlets at more than 20 m (60 ft) from Category C with wires #14—10

B. Major Feeders and Short Branch Circuits

Distribution panel devices

Bus and feeder systems in industrial plants

Heavy appliance outlets with "short" connections to the service entrance

Lighting systems in commercial buildings

C. Outside and Service Entrance

Service drop from pole to building entrance

Run between meter and distribution panel

Overhead line to detached buildings

Underground lines to well pumps

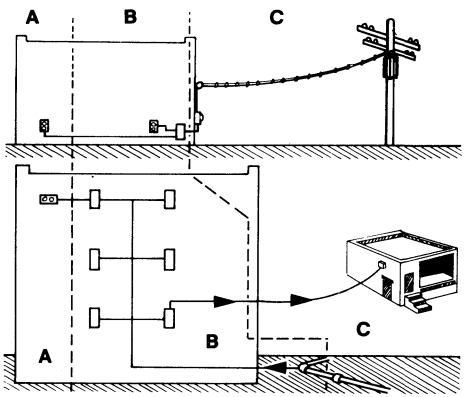


FIGURE 1
IEEE Std. 587-1980, Location Categories

LOCATION CATEGORY	WAVEFORM	OPEN CIRCUIT VOLTAGE	SHORT CIRCUIT CURRENT
A	0.5μs-100kHz Ring (Fig. 2A)	6000V	200A
B	0.5μs-100kHz Ring (Fig. 2A)	6000V	500A
	1.2 x 50μs Impulse (Fig. 2B)	6000V	---
	8 x 20μs Impulse (Fig. 2C)	---	3000A

TABLE 1 — Waveform Characteristics

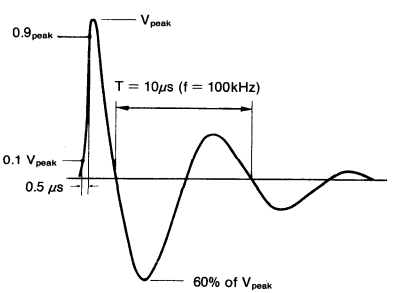
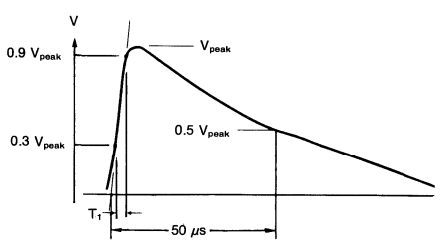
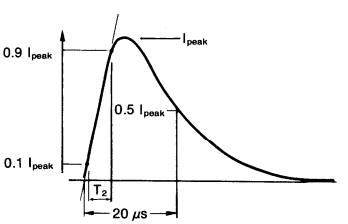


FIGURE 2A
0.5 μs — 100kHz Ring Wave



T_1 x 1.67 = 1.2 μs

FIGURE 2B
1.2 x 50 μsec Impulse



T_2 x 1.25 = 8 μs

FIGURE 2C
8 x 20 μsec Impulse

Another area worth summarizing from Standard 587-1980 is the rate of transient voltage occurrence. Transient occurrence varies over wide limits depending upon the power system, its loading and the amount of lightning activity.

Data collected from many sources have led to the plot shown in Figure 3. This prediction shows with certainty only a relative frequency of occurrence, while the absolute number of occurrences can be described only in terms of low, medium, or high exposure. These exposure levels are defined in general terms as follows:

(1) Low Exposure. Systems in geographical areas known for low lightning activity, with little load switching activity.

(2) Medium Exposure. Systems in geographical areas known for high lightning activity or frequent and severe switching transients.

(3) High Exposure. Rare but real systems powered by long overhead lines and subject to reflections at line ends, where the characteristics of the installation produce high sparkover levels of the clearances.

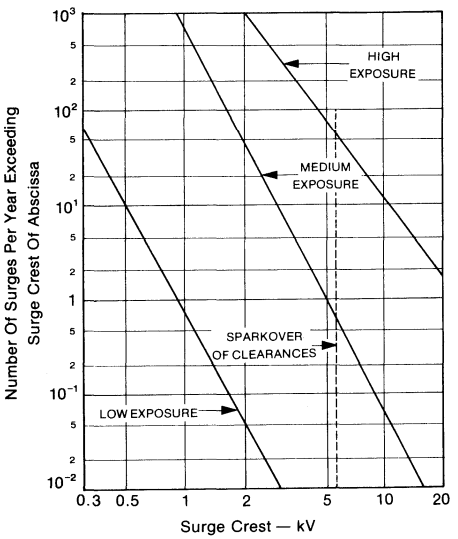


FIGURE 3
Yearly Rate Of Surge Occurrences At Unprotected Locations

A suppressor for use in most indoor location categories is adequately designed if it both protects and survives the occurrences shown on the medium exposure line. For example, it should survive a 6kV transient seven times, a 2kV transient 400 times, etc. for a 10 year life expectancy.

It should be emphasized that IEEE 587-1980 is not a test specification. It simply defines the open circuit voltages and short circuit currents which are most applicable to certain location categories. Protector performance is defined by the manufacturer. Transient voltage suppressors tested to the IEEE standard can be easily compared in terms of output voltage under identical input conditions.

Photos of output waveforms under different input conditions are useful when evaluating protector performance. It is desirable to have a slow rising output wave relatively free of spurious noise.

Other Line Transient Conditions

Fast rising transient wavefronts have also been observed on ac lines caused by switching transients generated close to the point of observation. As the distance between the points of origin and observation increases, line inductance and capacitance causes the wavefront risetime to decrease.

The possibility of a nuclear electromagnetic pulse (NEMP) on the power line should also be considered, particularly if essential military equipment is to be protected. Hard data describing the pulse is scant, but it is believed that, since its point of entry to the power lines is widespread, a fast rising pulse would appear in the power system. The pulse is usually described as having a rise in the kv/ns range and a decay of a few microseconds depending upon the altitude of the burst[2]. The spectrum extends roughly from 10KHz to 100MHz which easily excites the resonant frequencies of a system.

Development Of Suppressor Specifications

Based upon the preceding discussion of the transient environment on ac power lines, an intelligent spec can be composed. A decision must first be made whether the equipment location is best described by category A or B of IEEE 587-1980. Second, the maximum clamping voltage output must be selected. Since 400 volts is a standard voltage rating for economical semiconductors and capacitors, it is desirable to have the output level of the suppressor comfortably below 400 volts regardless of input waveforms. For a Category B location suppressor, Table 2 shows a suitable set of transient specffications.

PROTECTION MODE	MAXIMUM CLAMPING VOLTAGE	PEAK CIRCUIT VOLTAGE		PEAK CIRCUIT CURRENT	
		AMPLITUDE	WAVEFORM	AMPLITUDE	WAVEFORM
Differential (Line to Neutral)	350V	6kV	.5μs/100KHz	500A	.5μs/100KHz
		6kV	1.2 x 50μs	3000A	8 x 20μs
Common (Neutral to Ground)	500V	6kV	2 x 250ns	200A	2 x 250ns

TABLE 2—Transient Voltage Suppressor Specifications

The NEMP test (2x250ns) is based more on test capabilities rather than on an accurate representation of reality. The intent of the test is to insure that no overshoot occurs at the output, regardless of the rate of rise of the transient waveform.

Design Approaches

A general topology for transient protectors is shown in Figure 4 using the notations of Jacobus[3]. The diverter devices handle high currents but do not offer a precise control of voltage; gas tubes and MOV's are typical diverting elements. The clamp devices have low impedance and therefore offer

better voltage control but have lower current capabilities. A TransZorb voltage suppressor diode is a typical clamping device. The series impedances shown semi-isolate the various diverter and clamp stages by causing a voltage drop between them.

To meet the requirements of IEEE 587-1980, Category B, the topology of Figure 4 has proven to be quite cost effective. The series impedances are inductors. Depending upon the intended application, L sections could be added to or removed from the topology of Figure 4.

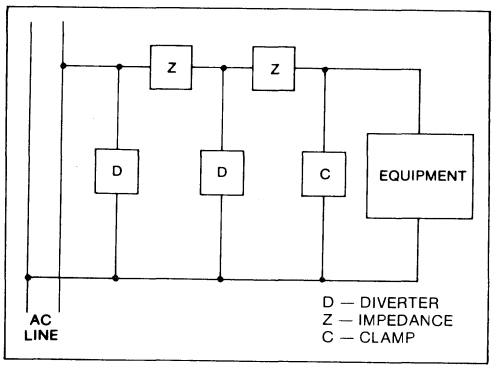


FIGURE 4
General Topology For A Protection Network

Capacitors can be added across the diverting and clamping elements to slow the rate of rise of fast pulses. Properly designed, the network of Figure 4 will provide rather precise voltage limiting, as well as slowing the rate of rise of fast switching transients or a NEMP. Methods of sizing the diverter, clamp, and inductive elements are discussed in the Jacobus paper. However, experience has taught that a practical design requires a good deal of attention to component selection and extensive testing.

Specifically, Jacobus suggests using the reactance of the series inductors at 100KHz to calculate network currents and voltages. For the 0.5μs/100KHz ring wave, using 100KHz reactance makes some sense; however, the highest stress is caused by the unidirectional impulse waves which have a much lower frequency content. Furthermore, the clipping action of the diverters creates a somewhat flat-topped wave with a width of about 50μs. In addition, the coils, and shunt capacitors if used for high frequency filtering, serve to stretch the pulse. Accordingly, a frequency of about 10KHz is more realistic to use for rough calculations; however, testing often indicates that inductors need to be much larger than calculated.

Shunt capacitors across the second diverter and the clamp element perform a valuable service in slowing the fast rise of incoming disturbances. The equivalent circuit of such a filter network is shown in Figure 5. The parasitic stray capacitances of the inductors, C_{S1} and C_{S2}, allow very fast pulse edges to shoot through the filter but they are attenuated by the shunt capacitances and clamped by the element C. A fast responding device, such as a TransZorb

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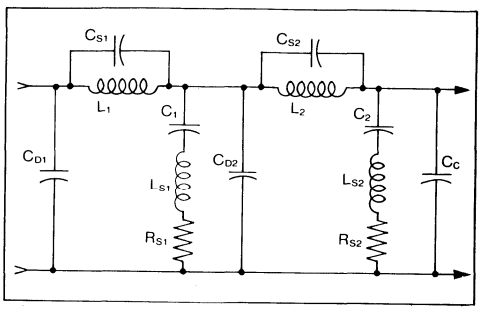

FIGURE 5
Filter Network Equivalent Circuit Showing Component Parasitics

Suppressor, is threrefore preferable for element C. The capacitances of the diverter, C_{D2}, and the clamp, C_C, usually provide a lower impedance shunt at very high frequencies than the discrete capacitors C_1 and C_2, which have more pronounced series parasitic inductance.

Note that the LC networks form series resonant circuits. To avoid large circulating currents, their resonant frequencies should be well removed from the 100KHz frequency typical of a lightning surge. Empirically, it was determined that having the resonant frequency of L_1 and C_1 considerably above 100KHz and that of L_2 and C_2 well below 100KHz provided the cleanest output.

Test Results Of The 587B Series Of Protective Modules

The General Semiconductor Industries' 587B family of ac power line protectors are designed to meet the specification of Table 2. Figure 6 shows the response to the unidirectional wave with open circuit voltage of 6000 volts and short circuit current of 3000 amperes. The top trace shows the voltage across a 12 ohm resistor which represents a 10A equipment load. The lower trace shows the dramatic reduction of the transient peak provided by the protector. Note

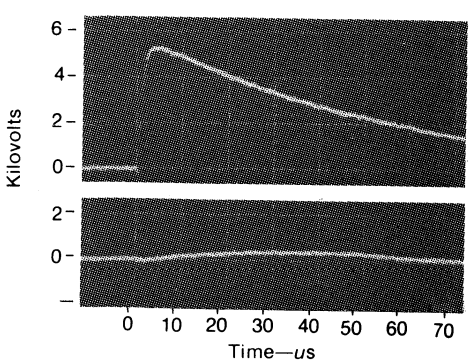

FIGURE 6—Transient Reduction
At Equipment Input Provided By Suppressor
Upper Trace: No Protection Lower Trace: Protector Output

the relatively slow rate of rise of the output pulse (25V/μs) and the peak level of 300 volts on the detailed photo of the output shown on Figure 7.

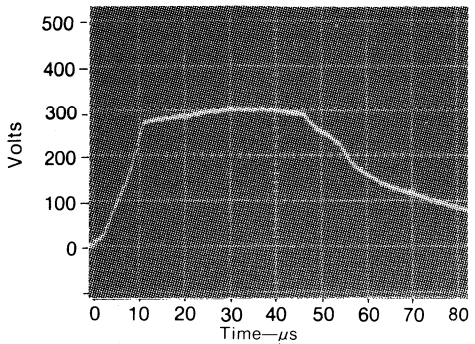

FIGURE 7.
Magnified View Of Protector Output

The output response with a ring wave input is shown in Figure 8. Figure 9 shows the output when a simulated NEMP is applied. The protector used is rated for 20 amperes ac current; the load simulates a 2 amp resistive load. The output noise is felt to be acceptable for most applications. The noise increases as the load current is reduced below 2A. Should the noise prove objectionable when the ac load is light, a high frequency load consisting of a 0.5μf capacitor in series with a 62 ohm resistor may be placed across the output.

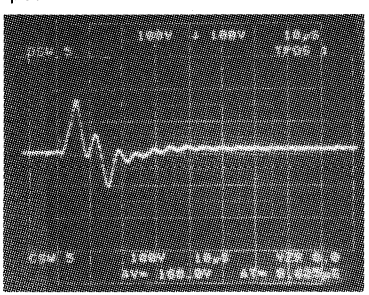

FIGURE 8—Protector Output With Ring Wave Input (6kV, 500A)

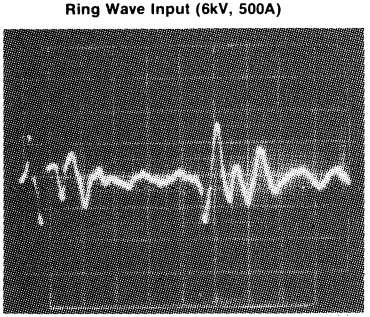

FIGURE 9—Protector Output With NEMP Input (6kV, 120A) 20V/Div.; 50ns/Div.

Applications And Installation

The 587B series of modules can handle the worst expected transients in an indoor environment. The modules are especially valuable when used in data processing and complex communications and instrumentation equipment.

Whenever a high voltage transient is present on the ac line, a large transient current will flow line to neutral and/or neutral to ground. It is important that the ac input to the module and the ground are distant from other wiring to prevent electromagnetic coupling. Should the transient current flow out the ground (green) lead, the impedance of the ground circuit causes conductive parts of the equipment cabinet or enclosure to rise—possibly several kilovolts—above the building earth ground. A potentially hazardous situation for personnel and equipment referenced to a different ground connection exists.

To reduce the undesirable potential difference between equipment, a practice called bonding is used. Bonding consists of connecting all conductive items together that are expected to conduct currents to earth. The bonding conductor must be sized properly for the high surge currents expected and must be solidly connected to each piece of equipment using the shortest possible path. All equipment is cross connected together to provide the lowest resistance that is practically achievable. Further information on grounding and bonding—vital to the equipment installer—is given in reference 3 and its references.

Summary

By placing a transient protection module between the ac power line and electronic equipment, failures caused by power line transients can be virtually eliminated, if the module handles the IEEE 587 environment under repeated surges, limits its output voltage to a safe defined maximum, and is installed properly.

Test results of a module fulfilling these requirements have been described. Peak output voltage has been shown to be under 350 volts regardless of the input waveform, provided that the stress levels of IEEE 587 are not exceeded. Also, it has been noted that proper grounding and bonding of equipment is essential for the protection of equipment and personnel.

References

(1) "IEEE Guide for Surge Voltages in Low-Voltage AC Power Circuits", IEEE Standard 587-1980, Institute of Electical and Electronic Engineers, 345 E. 47th St., New York, NY 10017.

(2) L. W. Pinkston, "Electromagnetic Pulse (EMP)", 1984 Interference Technology Engineers' Master. R&B Enterprises, P.O. Box 510, Plymouth Meeting, PA 19462.

(3) N. M. Jacobus, "Designing Power Line Transient Protection Circuits", Proceedings of Powercon 11, Power Concepts, Inc., April, 1984, D-4, pp. 1-11.

THE USE OF TRANSZORB® DIODES WITH POWER MOSFETS

by
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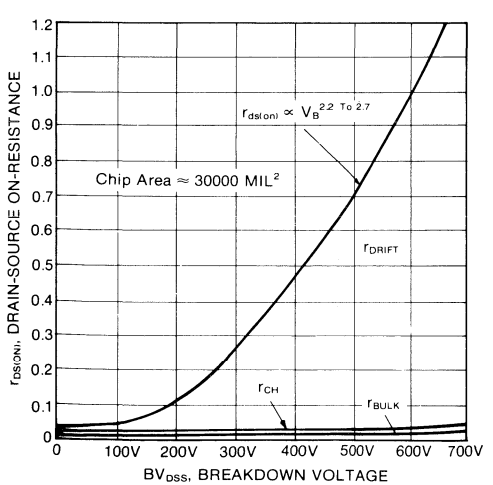
ABSTRACT

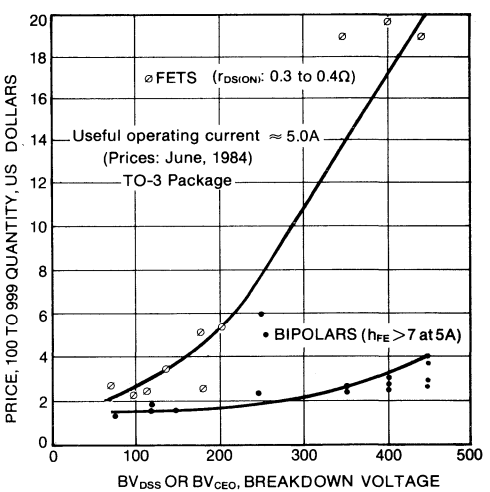
Power MOSFETs have a more rapid cost vs. breakdown voltage tradeoff than do bipolar devices. Transient Voltage Suppressor TransZorb® Diodes may be used to reduce the voltage stress on the MOSFET so that a considerably lower cost device may be used. The TransZorb diode serves a dual application; a transient protector and an ancillary snubber. A design approach is given and successful designs are described.

I. Need For Transient Protection

All off-line power electronic systems are subject to unwanted transient voltages. These originate from two sources: transients on the incoming ac line and transients generated in the system by the rapid switching of the power switch. The usual design procedure with bipolar switches calls for allowing generous voltage margins between the maximum anticipated circuit voltage and the breakdown rating of the transistor. The penalties are not too severe. Increasing a bipolar's breakdown rating causes a reduction in current gain and switching speed. The gain, however, can be restored and speed improved with a modest increase in die area.



Drain-Source On-Resistance vs Voltage Breakdown
FIGURE 1



Effect Of Voltage Rating On FET Price
FIGURE 2

The MOSFET displays several properties which cause protection requirements to differ from those of the bipolar junction transistor (BJT). Figure 1 shows the direct tradeoff in on-resistance with breakdown voltage, for a fixed die size. To maintain a constant on-resistance and current rating as voltage increases requires a rapidly increasing die size.

The price picture for BJT's and FET's is shown in Figure 2. It is evident that when using FET's, reduction of the required voltage specification is a critical and very cost effective task for the design engineer.

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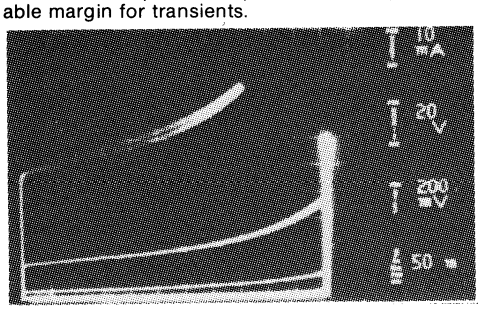
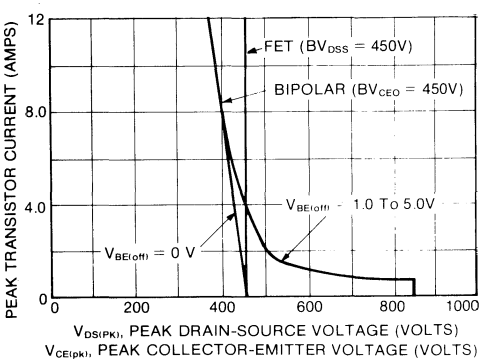
It should be noted that the mechanism of breakdown also markedly differs between the MOSFET and BJT. Figure 3 shows the Zener-like property of the FET. The high voltage drop across the device results in high dissipation and usually destruction, should operation occur even for nanosecond intervals in the avalanche breakdown region. Operation in avalanche breakdown is not advisable for a bipolar either, but it can usually sustain some energy in the $BV_{CEO(sus)}$ mode. Circuits are usually designed to limit peak voltage below BV_{CEO}. At low currents, however, most bipolars can handle voltages up to the BV_{CBO} limit which may approach two times the BV_{CEO} limit. The operating limits for a FET and a comparably rated bipolar device are shown in Figure 4. Properly snubbed, the bipolar can operate with a very comfortable margin for transients.



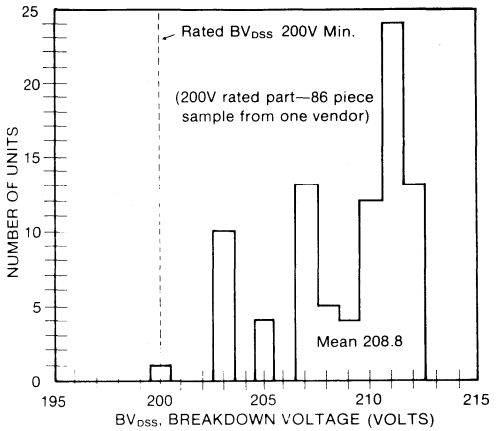
Typical FET Breakdown Characteristics
FIGURE 3



Maximum Reverse Bias (Turn-Off) Safe Operating Area
FIGURE 4

In addition, the FET breakdown voltage has a significant temperature coefficient—approximately 0.5V/° C for a 400V part—which must be considered in the design. The BV_{CEO} breakdown of a BJT is essentially independent of temperature.

The close tolerance of observed MOSFET breakdown voltage is shown in Figure 5. This is a histogram of a sample of 86 parts rated at 200V. Note the nonexistent margin for error due to the tight distribution of units just above the specification minimum. The mean of this sample is 208.8 volts, with a standard deviation of 3 volts. Experience with bipolars has indicated that a margin of 50 volts is not uncommon.



FET Avalanche Voltage Distribution
FIGURE 5

Summarizing the discussion, the need to protect FETs with some voltage limiting device is compelling because:

1. It is expensive to design in voltage margins.
2. FETs display a sharp breakdown characteristic of low energy capability.
3. The breakdown voltage can be expected to be very close to the specified voltage rating for most of the population.

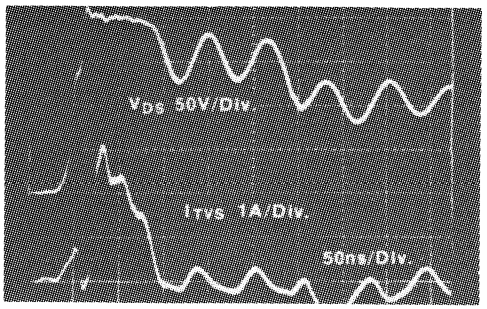
II. Need For Ancillary Snubber

A MOSFET circuit has somewhat more critical snubbing requirements than does a corresponding bipolar circuit. As discussed in the previous section, the FET cannot dependably withstand any transients if they exceed the FET breakdown voltage, whereas the bipolar is somewhat more forgiving.

The transient problem is intensified by the fast switching of the FET. The specified FET current rise time is several times faster than that of the bipolar (for example 30ns vs. 300ns) and in practice FET circuits usually switch faster than bipolar circuits. These fast rise times generate ringing in the stray wiring inductances between the snubber and the FET as well as in the residual inductance and resistance of the snubbing circuit causing the FET to suffer short duration (20-100ns) transients. These transients are observed by probing right at the FET package, rather than at the snubbing point. Figure 6 shows typical waveforms encountered in a MOSFET SMPS. The clamping effect of the protective device is evident on the V_{DS} waveform.

Using the protector in this fashion is termed an "ancillary snubber". It is an additional snubbing device intended to clamp any fast transients which remain after the application of the main snubber. By reducing peak voltage, a lower cost FET can then be used. Dissipation in the ancillary snubber should ordinarily be a small fraction, typically 10%, of the main snubbing power in order to remain within the protector steady state power ratings.

It is important that the protection device be mounted as close as possible to the FET drain and



Waveforms Of 450W SMPS
FIGURE 6

source leads to minimize the lead inductance (L_L). Doing this is critical because any package or lead inductance will cause the FET to suffer an additional transient voltage over that of the device clamp voltage (V_C). That is, the drain source voltage, V_{DS}, is given by:

$$V_{DS} = V_C + L_L \Delta I/\Delta t$$

For example, a 5 Amp pulse rising in 5ns will cause a 10V increase in V_{DS} over V_C for a lead inductance of only 10nH, about 1½" of AWG #18 wire. Thus the rating of the FET will have to be increased to accomodate this overshoot.

III. Choice Of Protective Device And Circuit

The ideal device to insure operation of the FET within its limits would have these properties:

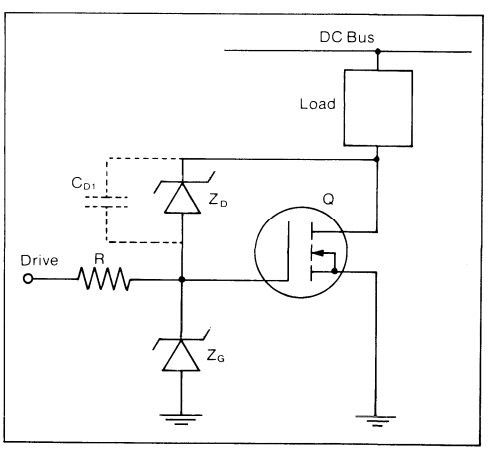
1. Low clamping ratio—to allow optimum utilization of the available FET safe operating area while abruptly limiting just below FET breakdown.
2. Low capacitance—to take best advantage of the inherently fast FET switching.
3. Low cost—to reduce overall systems cost by reducing FET cost without excessive protective device cost.
4. Sustantial steady-state power rating—to permit use of the transient protection device to "mop-up" any remaining repetitive voltage transients after application of snubbing techniques.
5. A variety of close tolerance breakdown voltages—to closely match the FET requirement.
6. Low inductance and fast switching—to clip short (30ns) spikes which can be FET-fatal!
7. Shorted catastrophic failure mode—to save the relatively expensive FET under extreme overload.

Table 1 compares the various protection devices available. The MOV is too soft in its clamp property and is specified in large voltage increments. The standard Zener is not rated for clamp properties and is not fail-safe. Gas tubes are unsuitable due to their arc conduction mode and wide breakdown variation. The Transient Voltage Suppressor (TVS) or Trans-Zorb Diode, if properly specified and selected, is the only device which can fulfill the requirement.

DEVICE	MOV	ZENER	TVS	GAS SURGE ARRESTOR
Range Of Voltages	12-4700	3-200	5-400	90-1,000
Voltage Spec Increments	10-25%	5-10%	10%	20%
Tolerance	10%	5%	5%	15%
***Clamp Ratio @ 10A**	1.85 (13 J)	1.65 No Spec	1.25 (15 J)	2.55
Capacitance (200V Device)	150pF	30pF	30pF	1.2pF
Price	Medium To Low	Low	Medium	Medium
Steady State Power Dissipation Capability	Very Low (¼W For 10 J Device)	Good To 50W	Good To 10W	Not Applicable
Failure Mode	Gradual Shift In Breakdown	Open Or Short Circuit	Short Circuit	Gradual Decrease In Protection
Polarity	Bipolar Only	Unipolar & Bipolar	Unipolar & Bipolar	Bipolar Only
Other Properties And Notes	Good For Mains Use, Not Suitable FET Protection	No Spec For Transient Use	Ideal For SMPS Switch	After Ignition Enters Arc Mode With Low Voltage Drop—Requires Zero Current To Extinguish

*Defined as V_C/V_{BR} measured for a particular unit.

Protective Device Comparison
TABLE 1.

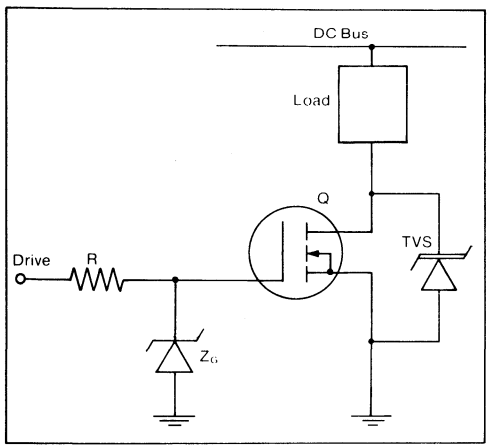


FET Protection Drain To Gate—Not Recommended
FIGURE 7

A suggested technique which has been proposed by FET manufacturers for protection is shown in Figure 7: A Zener rated below the FET breakdown (minus $V_{gs(on)}$) is placed from drain to gate. During a transient the FET is turned on and can handle a much higher current than the Zener diode alone. The configuration has some serious problems:

1. Limited Zener availability at high voltages.
2. Zener capacitance can induce an unwanted dv/dt turn-on of the FET which could be fatal.
3. Increased power dissipation in the FET.

Experience has taught that a protection diode from drain to source is better as shown in Figure 8. Note that a gate to source Zener is always advisable, regardless of the drain voltage breakdown protection scheme.



FET Protection Drain To Source—Preferred Circuit
FIGURE 8

IV. Selecting The Transient Voltage Suppressor

Selecting the rating of the protector is a non-trivial task. This is caused by the lack of correspondence between the manner in which the TVS diodes are specified versus the service conditions experienced in the application. The TVS must be selected on these criteria:

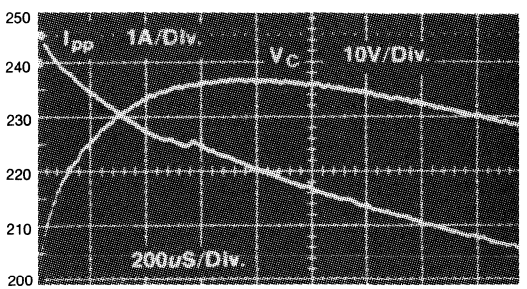
1. Minimum breakdown voltage must exceed maximum bus voltage under worst case conditions. The peak bus for a high line (135/270V) condition is 191/382 volts.

2. Maximum clamping voltage (V_C) at the peak applied TVS currents should be under the MOSFET minimum breakdown voltage. Peak TVS current will approximate peak switch current. For a supply with an 8 Amp switch current, TVS peaks of 3-5 Amp are typical. V_C must be determined for the TVS at its operating current at the extremes of the expected ambient temperature. The MOSFET temperature coefficient must also be considered.

3. The TVS continuous power dissipation must be sufficient to handle the average power experienced by the TVS because of the repetitive current pulse applied.

Specifications for Transient Voltage Suppressor Diodes are generally keyed toward suppressing a large single shot impulse. The format was developed years ago using standards devised by the telephone industry. The key specifications are the range of breakdown voltage (V_{BR}), usually specified at 1mA, and the maximum clamping voltage (V_C) usually specified at the rated power level of the diode. The clamping voltage is specified for a 10 x 1000μs impulse (10μs rise, 1000μs decay to the 50% point) developed by the U.S.A. Rural Electrification Agency (R.E.A.) to simulate lightning surges on telephone lines. The measured voltage is the sum of the breakdown voltage and a non-linear IR drop; both components are temperature sensitive. Since the specifications do not fit a snubber/clipper application, additional data and some data manipulation is necessary in order to determine if a diode will fit a particular requirement.

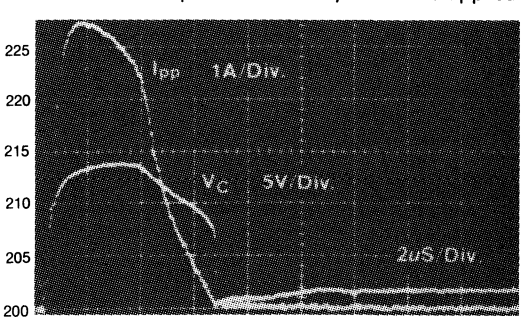
Figure 9 shows the voltage (V_C) and current (I_{PP}) waveforms for the 10 x 1000 impulse used for the standard clamping voltage test on a 200 volt breakdown device. The voltage wave shows the increase in voltage above the breakdown voltage of the diode at 25° C. The initial rise in voltage is the result of diode resistance. The slow rise to the peak value of 46V at about 800μs after pulse application is caused by the temperature rise of the junction. The major temperature dependent voltage change is caused by the temperature coefficient of the avalanche breakdown voltage.



Clamping Voltage Response For A 10 x 1000 Impulse

FIGURE 9

The waveforms of Figure 9 do not permit an accurate observation of the IR drop. A short test pulse is needed. Figure 10 shows the current and voltage waves when a pulse of about 5μs width is applied.



Clamping Voltage Response for a 5us Pulse

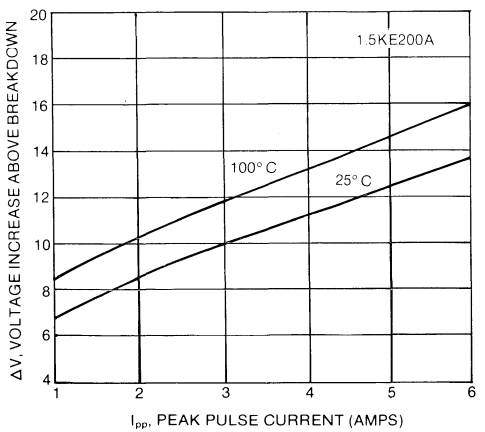
FIGURE 10

Some thermal effects are evident because the voltage does not track the fall in current; however, by reading the voltage at the peak of the current wave, the temperature contribution is small. Thus the IR drop is only 13 volts at the specified test condition of 5.5A.

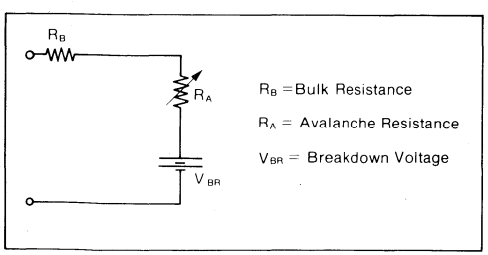
Note that the temperature contributed component of voltage rise is almost three fourths of the total. This proportion has been found to be roughly the same regardless of the TVS diode voltage. Therefore, a more reasonable estimate of the voltage rise (ΔV) above breakdown under short pulse conditions (i.e., negligible instantaneous heating) can be found from:

$$\Delta V = (V_{C(10 \times 1000)} - V_{BR(max)})/4 \qquad 1)$$

The voltage from Equation 1 is roughly correct for the test current I_{PP} specified for the clamping level V_C. Typical data supplied by the manufacturer is shown in Figure 11. It indicates a fairly constant resistance at currents above one ampere. At low currents the avalanche resistance increases rapidly with decreasing current. This behavior suggests a model as shown in Figure 12. At currents above one ampere, the resistor R_A may be replaced with a voltage taken from the y axis intercept of Figure 11. Also from Figure 11, the bulk resistance R_B may be read as approximately 0.9 ohms. At currents different from the specification, ΔV may be found by adding an IR drop correction term to the voltage from Equation 1.

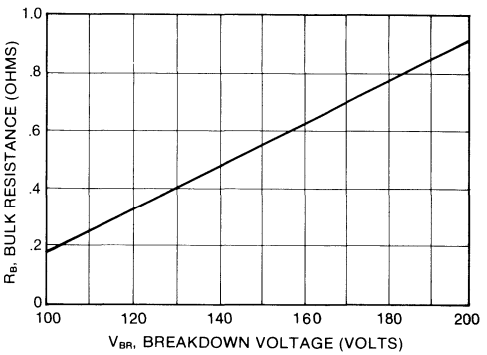


Clamping Voltage With A Fast Pulse
FIGURE 11



Model For A Transient Voltage Suppressor Diode
FIGURE 12

The resistance R_B varies somewhat proportionately with diode breakdown voltage as shown on Figure 13. This data can be used directly to estimate voltage levels for diodes in the 100 to 200 volt range. Note that R_B of a 200 volt diode is over twice that of a 100 volt part. Consequently, diodes with breakdowns over 200 volts are usually made by stacking die. For example, a 400 volt part is composed of two 200 volt diodes. The data of Figure 13 is therefore useful in estimating clamping levels for all diodes with breakdowns over 100 volts.



Relation Of Bulk Resistance To Breakdown Voltage
FIGURE 13

In a snubber/clipper application, some average power (P_{AV}) is dissipated and will cause an increase in breakdown voltage. The upper limit $\overline{V}_{BR}$ may be found from:

$$\overline{V}_{BR} = V_{BR(max)@25°C} + \Theta_V(T_J - 25°C) \qquad 2)$$

Where Θ_V = Temperature coefficient of breakdown voltage in volts per degree centigrade

T_J = Juntion temperature (° C)

The junction temperature (T_J) is calculated either from:

$$T_J = T_A + R_{\theta JA} P_{AV} \qquad 3a)$$

or

$$T_J = T_L + R_{\theta JL} P_{AV} \qquad 3b)$$

Where T_A = Ambient temperature (° C)
$R_{\theta JA}$ = Junction to ambient thermal resistance
P_{AV} = Average power
$R_{\theta JL}$ = Junction to lead thermal resistance
T_L = Lead temperature

The thermal resistance is not often specified but can be found by using the rated power dissipation (P_D) and temperature rating ($T_{J(max)}$), i.e.:

$$R_{\theta JA} = (T_{J(max)} - T_A)/P_T \text{ @ } T_A \qquad 4a)$$

or

$$R_{\theta JL} = (T_{J(max)} - T_L)/P_T @ T_L \qquad 4b)$$

The total voltage is the sum of V_{BR} from Equation 2 and ΔV from Equation 1, corrected for the actual current through the TVS.

An empirical procedure is a convenient way to select the TVS. We recommend starting with the breadboard circuit, using a passive snubber and the highest available voltage grade of FET. A variety of TVS diodes covering the range of interest should be available. These could be series combinations of lower voltage parts, say 50V, 100V, and 200V devices. Alternately, a TVS whose anode is returned to a variable power supply could be used for circuits where the FET source is grounded. The REA 10 x 1000 current rating should be comparable to the FET on-state current.

The snubbing current in the TVS is observed with a current probe around the TVS lead. The current and duration of the pulse is noted as the TVS (or variable supply) voltage is varied. For each TVS voltage grade, the TVS snubbing power may be found from:

$$P_{AV} = V_C I_{PP} t_p f_r \qquad 5)$$

Where P_{AV} = Average Power
V_C = Clamping Voltage of the TVS
I_{PP} = Peak Pulse Current
t_p = Average Pulse Width
f_r = Repetition Frequency

From this information, the tradeoff between TVS power dissipation and FET breakdown voltage (and hence cost) may be seen. Choosing the lowest voltage FET, consistent with a reasonably low cost appropriate TVS is easily done.

V. Finalizing The Design

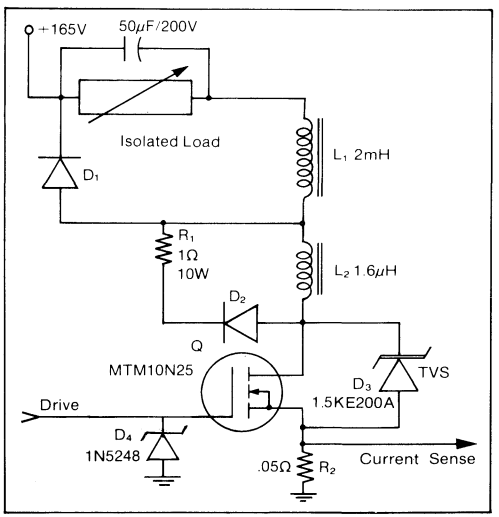
Use of the various procedures and equations discussed are illustrated in this section for three different applications. For convenience, Table 2 is presented. It summarizes the key specs for a popular series of TVS. ΔV for the 5μs pulse was calculated using Equation 1. V_C for the 5μs pulse was calculated by adding ΔV to the maximum breakdown voltage.

ELECTRICAL	PART NUMBER			
CHARACTERISTIC	1.5KE200A	1.5KE220A	1.5KE250A	1.5KE400A
Breakdown Voltage V_{BR} Volts Min/Max	190/210	209/231	237/263	380/420
Maximum Clamping Voltage 10 x 1000 V_C (Volts)	274	328	344	548
Maximum Peak Pulse Current I_{PP} (A)	5.5	4.6	5.0	4.0
Estimated Maximum 5us Volts Above V_{BR} ΔV (Volts)	16	24	21	32
Estimated Clamping Voltage 5us Pulse V_C (Volts)	226	255	284	452
Maximum Temp. Coefficient V_{BR} θ_V (V/°C)	.216	.214	.266	.432

TVS Specifications For Off-Line SMPS Use
TABLE 2

The first example is a constant current buck regulator operating from 120Vac, the most commonly used main in the U.S.A. The circuit of Figure 14 provides a constant 9 Amp output into a load which varies from 2 to 5 Ohms. The basic regulator is composed of choke L_1, FET switch Q and freewheeling fast recovery diode D_1. The switch current is sensed by R_2; the resulting feedback signal and the gate drive are referenced to ground. The repetition frequency is 33 KHz. The ambient operating temperature range is 0°C to 50°C.

This buck topology generates a current spike when the switch turns on, during the reverse recovery



8 Amp, 0V to 50V Constant Current Buck Regulator
FIGURE 14

interval of D_1. The small choke L_2 limits the magnitude of this current spike, but it stores energy and so is a source of voltage transients. Diode D_2 and resistor R_1 provide a path to dissipate this stored energy. The TVS diode D_3 snubs any remaining energy by clamping the drain-source voltage below the breakdown voltage of Q. Diode D_4 protects the gate.

The power switch has a rated BV_{DSS} of 250 volts. Since FETs are rated on the Absolute Maximum Rating System, this rating is only applicable at 25°C. The temperature coefficient of the FET is about 250mv/°C. Therefore, at 0°C, limit samples of the FET could breakdown at 243.8V, which sets the upper limit of the TVS clamping voltage at 0°C. The maximum junction temperature of the FET under worst case operating conditions will not exceed 100°C. Therefore 268.8 volts is the upper temperature limit of both FET breakdown and maximum TVS clamping voltage. The calculated FET breakdown voltages are listed in Table 3 along with other key data points for this example.

CHARACTERISTICS	WORST CASE LIMITS		
System Ambient Temp.	25°C	0°C	50°C
FET Breakdown Volts	250.0	243.8	268.0 @T_J = 100°C
TVS Breakdown (Vmin)	190.0	184.6	
TVS Breakdown (Vmax)	210.0		224.3 @ T_J = 91.2°C
Maximum Clamping Volts		215.0	240.2 @ T_J = 91.2°C

Key Voltages And Temperatures For Design Example 1
TABLE 3

The lower limit of the TVS should be above 184V to avoid conduction under the high line condition of 130Vac. The cold temperature limit is the worst case.

The waveshapes for this circuit using the best snubber/TVS combination were previously shown in Figure 6. Peak TVS current is approximately 3.2A; the current wave is modeled by a square wave having a 50ns pulse width. From Equation 5, the average power calculates as:

$$P_{AV} = (200)\ (3.2)\ (50 \times 10^{-9})\ (33 \times 10^{3}) = 1.06W$$

Looking at Table 2, it appears that a 1.5KE200A would be satisfactory but the worst case conditions need to be checked. The maximum temperature coefficient is 0.216 Volts/°C. At 0°C, the breakdown could be as low as 190-(.216)(25) = 184.6 volts which is just barely satisfactory.

The upper junction temperature limit of the TVS is more difficult to ascertain. To minimize inductance the TVS should be mounted as close as practical to the transistor drain-source leads which will transfer some heat from the transistor to the TVS. The TVS lead temperature in the buck regulator measures 45°C at room ambient of 25°C. At the 50°C upper operating temperature of the equipment, the lead temperature T_L is 70°C. The TVS has a 5W rating at T_L = 75°C. $T_{J(max)}$ is 175°C. Using Equation 4b:

$$R_{\theta JL} = (175 - 75)/5 = 20°C/W$$

Using Equation 3b, the junction temperature is found to be:

$$T_J = 70 + (20)(1.06) = 91.2°C$$

The maximum breakdown voltage is found from Table 2 and Equation 2 as:

$$\overline{V}_{BR} = 210 + .216\ (91.2 - 25) = 224.3$$

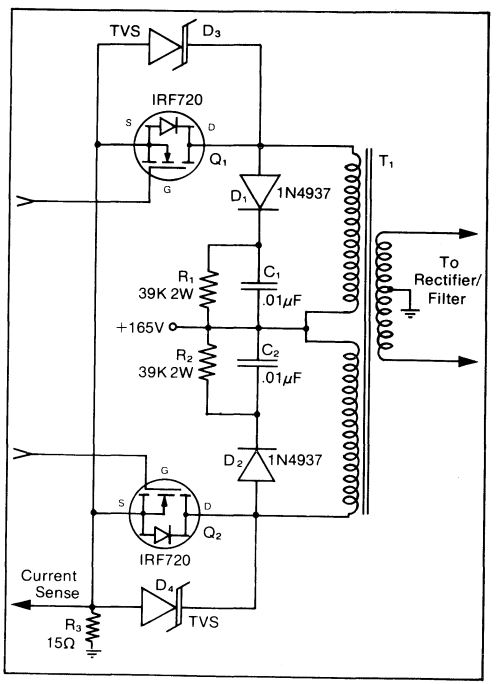
The IR drop (ΔV) in the TVS must now be determined. Data for the 1.5KE200A is shown in Figure 11. It indicates ΔV = 12 volts at 100°C and 10 volts at 25°C, typically. Another approach is to work from the 5.5A estimated ΔV limit of 16 volts. The current correction term is IR_B where R_B is shown in Figure 12 as 0.9 Ohms. Therefore the voltage correction for current is (3.2 - 5.5) (0.9) = -2.1V. Figure 11 indicates a +2 volt correction for T_J = 100°C. Finally:

$$V_{C(max)} = 224.3 + 16 - 2.1 + 2.0 = 240.2V$$

Thus the clamping voltage is well below the actual FET breakdown of 268 volts at T_J = 100°C.

The worst case situation at 0°C needs to be checked. With a high limit TVS and a conservative Θ_V of 0.2V/°C, the breakdown at 0°C is 210 + .2 (0 - 25) = 205V. At T_A = 0°C, the TVS junction will be at 20°C steady-state. Accordingly voltage ΔV at T_A = 0°C is less than the 10 volts shown in Figure 11, so that total V_C will not exceed 215 volts. The FET breakdown at 0°C was shown previously to be 243.8, well above the expected V_C.

The supply shown in Figure 15 is another example. It uses a pair of 400V FETs in a center-tapped push pull configuration. The dc bus is from a rectified 120Vac line (165Vdc). The push-pull topology subjects the FET to twice the bus voltage plus the overshoot due to leakage inductance. At high line the



A 100 Watt Push-Pull Converter

FIGURE 15

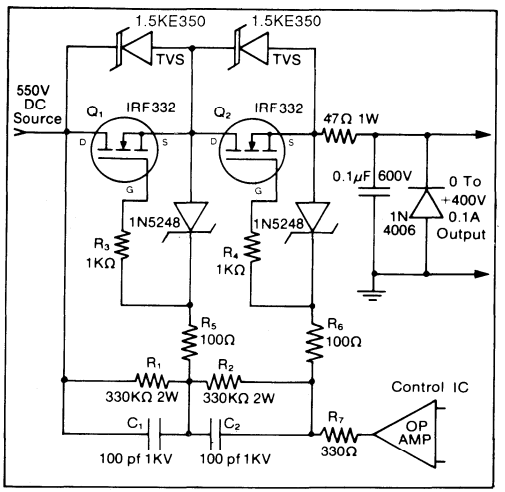
FET steady-state off-voltage is 368 volts.

The leakage was minimized by careful transformer design. The leakage energy is snubbed primarily by diode-resistor-capacitor networks D_1—R_1—C_1 and D_2—R_2—C_2. The small remaining transient is clamped by the transient suppressing diodes D_3 and D_4. Since the FET breakdown voltage rating is 400 volts, the voltage margins in this situation are quite tight. In order to use the lower cost 400V FET, it was necessary to use a tightly specified TVS, having a minimum breakdown voltage of 370V and a maximum of 390V.

The last circuit to be described is a linear regulator. The circuit provides a 0 to 400 volt output with low noise and precise regulation from a 550V ±50V source. See Figure 16.

Two FETs in series are used with 400 volt ratings. Resistors R_1 and R_2 divide the applied voltage by 2 and drive the gate of Q_1. C_1 and C_2 provide dynamic voltage sharing by swamping FET and stray capacitances. The gate of Q_2 is driven by the control IC op-amp. The control circuitry is referenced to the source of Q_2 (output of circuit). The gate resistors R_3 and R_4 are parasitic suppressors. Resistors R_5, R_6 and R_7 limit fault currents fed to the control circuit in case of drain to gate shorts in either FET.

Protection in this case is used simply for random transients and consists of a 1.5KE350 TVS across each FET plus an 18V gate Zener. The TVS diodes also pass reverse fault currents back to the 550V bus.



Linear Regulator Using Series MOSFETs
FIGURE 16

4

APPLICATION NOTES

VI. Summary

A method permitting use of lower voltage and hence lower cost FETs in switched-mode power supplies has been described. The technique involves using a carefully chosen Transient Voltage Suppressor (TVS) diode across the FET drain-source terminal to assure voltage spikes are within the FET rating. A method has been detailed for calculating the TVS performance from the data given on manufacturers data sheets. Its application to successful designs has been discussed.

GENERAL REFERENCES

1. General Semiconductor Industries, Inc. Diode and Transistor Product Catalog, 1983
2. General Electric Transient Voltage Suppression Manual, 4th Edition
3. International Rectifier Hexfet Data Book, 1982
4. Motorola Zener Diode Handbook, 1967
5. Motorola Rectifiers and Zener Diodes Data Book, 1982
6. Motorola Power Data Book, 1982

ACKNOWLEDGEMENT

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HARDENING POWER SUPPLIES TO LINE VOLTAGE TRANSIENTS

by
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Abstract

The power line transient environment is described. Transient voltages on the DC output of off-line rectifier/filter designs are shown. Protection schemes are discussed. An integrated rectifier/transient suppressor circuit is suggested as a cost-effective means of rendering the DC bus virtually immune to line transients.

INTRODUCTION

Unexpected line voltage transients are finally being recognized as a significant factor in the failure of Switching Mode Power Supplies (SMPS). As stated in a recent Navy publication[1]: "The most predominant power supply failure modes are caused by peak instantaneous transients and subtle factors within and external to the power supply. . . The following is a list of key points to consider when designing and evaluating a switching-mode power supply design: (1) Put voltage transient protection on the input power lines."

Until the publication of IEEE Standard 587-1980[2], the designer of off-line SMPS was unsure of the ac line transient environment. Now switching power supplies can be designed to meet this standard and pulse generators are available which produce the waveforms specified. The standard specifies that low impedances across the line in commercial and industrial environments should handle an 8/20 current waveshape (double exponential, 8μs rise time, 20μs decay to half of peak) having a peak amplitude of 3000A.

It should be understood that lightning induced transients propagate through a system as a current source looking for a low impedance path to ground. It is unlikely that most designers make provision for the rectifier and filter system to handle pulse currents up to 3000A, but a conservative design philosophy indicates that this should be done. The task is not easy, because component manufacturers do not generally consider this problem either.

A rectifier diode having a single-cycle 60Hz surge current rating exceeding 300A would most probably handle the 3000A, 8/20μs impulse specified in the standard, but the capability of rectifiers with lower ratings is questionable and needs to be verified. Rectifier diode surge capability will not be further addressed in this paper but clearly the rectifier must handle surge currents; the amount depends upon the protection scheme used.

In most off-line SMPS, the element which prevents excessive transient voltages from appearing across the DC bus and also bears the brunt of carrying the line to neutral transient pulse current is the filter capacitor. However, the charge delivered by the input transient and the voltage drop across the capacitor's ESL and ESR combine to develop a large overshoot voltage. This overshoot usually shorts the power switches connected to the DC output from the rectifier system.

Providing a network to limit voltage to a predetermined maximum rather than using higher voltage power switches offers a number of advantages to the power supply designer, independent of the choice of switching transistor (i.e., bipolar or FET). For a bipolar transistor of a given die area, lowering the breakdown voltage raises current gain and reduces all switching times. Reducing the breakdown voltage of a FET chip causes a marked decrease in on-state voltage—the principle determinant of power loss—because of the relationship $r_{DS(on)}$ of $V_B^{2.5}$. Alternately a smaller size power switch chip could be used to achieve the same performance while realizing a significant cost savings[3].

CONDITIONS IN AN UNPROTECTED SYSTEM

Most SMPS have an input network as shown in Figure 1. The impedance is used to limit start-up inrush current without causing excessive power loss. The series impedance may be a thermistor or a resistor which is often shunted by a triac to reduce power loss after start-up.

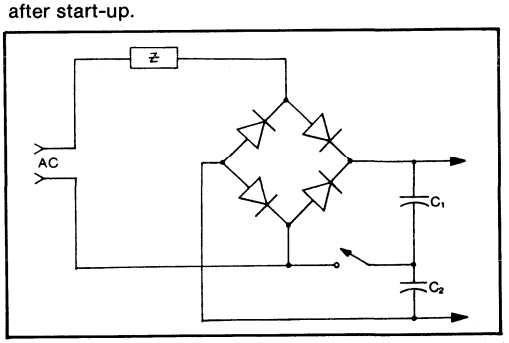

FIGURE 1—Basic line rectifier & filter for SMPS operating from 120/240V lines

It is not unusual to allow for a 20% tolerance on a 120/240V ac power line which puts the voltage crest at about 400 volts. Added to the dc level is the overshoot caused by the 3000A impulse. The usual switching power supply which operates from 120/240V inputs has two capacitors as part of the voltage doubler arrangement. The capacitors are connected in series when used on 240V. Thus, the total dc bus voltage spikes up to twice the individual capacitor transients when used on 240V.

The voltage waveform of Figure 2 reveals the presence of three components of overshoot: 1) a fast rising step caused by the di/dt of the wave flowing through the capacitors ESL, 2) an in-phase component caused by the current flow through capacitor ESL, and 3) a charge placed on the capacitor. Obviously, the transient voltage can be reduced by using a large

valued capacitor having low ESL and ESR. The relationship is given in Equation 1.

$$v_C = \frac{1}{C}\int i\,dt + iR_s + L_s\frac{di}{dt} \qquad (1)$$

where

C = input filter capacitance
i = pulse current
R_s = capacitor equivalent series resistance (ESR)
L_s = capacitor equivalent series inductance (ESL)
di/dt = rate of rise of transient current

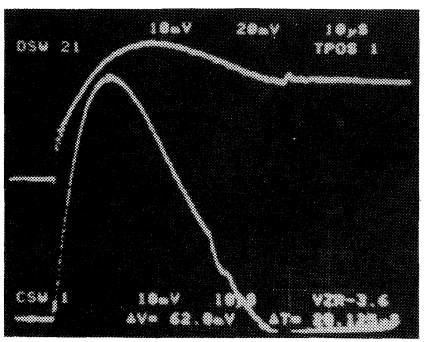

FIGURE 2—Capacitor waveform showing spike caused by current, and charge placed on capacitor
($C_1 = C_2 = 650\mu F$; Upper: 10V/div; Lower: 100A/div; Time: 10μs/div)

Measured voltage transients for some different capacitors when pulsed with 500A in the circuit of Figure 1 are shown in Table 1. With a 3000A pulse, overshoots of 6 times the values shown would occur. In all cases of 240V input, the transient voltage exceeds the typical 250V surge rating of a 200 volt capacitor. Even worse, the DC bus—possibly at about 400 volts because of high line, low load condition—is now up to at least 560 volts! No wonder power switch failures occur in seemingly well designed systems.

C_1, C_2	Type	Input	Peak Transient Voltage	Charge Voltage
540μF	Mepco/Electra 319DA541T250AMA1	120V	39V	30V
		240V	75V	58V
650μF	Mepco/Electra 3120EA651T200BHA1	120V	33V	23V
		240V	65V	46V
2100μF	General Electric 44A417052M21	120V	12V	7V
		240V	27V	16V

TABLE 1—Transient performance of the circuit of Figure 1
(Peak Pulse Current = 500A)

The spike could be clipped by a suitable TVS device but the charge voltage persists for too long and is not easily eliminated. The best solution is to minimize the amount of transient current being fed to the capacitor.

TRANSIENT PROTECTION TECHNIQUES

General principles of powerline transient protection have been described in a paper by Jacobus[4]. Almost concurrently, a specific module designed using these same principles which meets the 3000A specification of IEEE 587-1980 was described by Roehr and Clark[5]. Both papers deal with providing transient protection downstream from susceptible equipment. However, in a power supply, components which must be present for rectification and filtering may be used as part of the transient suppression network.

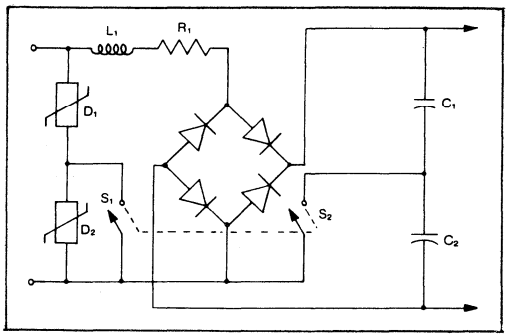

FIGURE 3—Basic circuit with MOV protection

When transient protection is used in a SMPS, it most often is nothing more than a single MOV across the line as shown in Figure 3. Table 2 shows test results taken in the circuit of Figure 3. Note that the worst transients occur in the 240V position when both switches are open. However, unless the MOV voltage is adjusted to fit the lower line voltage when used on 120V ac, (i.e., S_1 is closed), a very large capacitor current flows. For example, with only .5 ohm impedance the 77 volt spike appears across only one capacitor; with 3000A of input current the spike would increase to 115V which could exceed the surge voltage rating of the capacitor. The 106 volt transient increases to about 150 volts when 3000A is applied, bringing the bus voltage to 550 volts.

R_1 - L_1	Input	S_1	Peak Transient Voltage	Charge Voltage	Peak Capacitor Current
0.5Ω - 0μH	120V	Open	77V	54V	1080A
		Closed	24V	21V	440A
	240V	Open	106V	78V	780A
0.5Ω - 100μH	120V	Closed	18V	10V	190A
	240V	Open	74V	47V	440A
1.0Ω - 100μH	120V	Closed	12V	7V	130A
	240V	Open	53V	34V	300A

TABLE 2—Transient performance of the circuit of Figure 3
($R_1 = 0.5\Omega$, $C_1 = C_2 = 540\mu F$, Peak Pulse Current = 2000A)

To improve the transient suppression, the capacitor and/or the series impedance must be larger. The data in Table 2 taken with higher series impedances shows some improvement in lowering the transient levels but the transients are still higher than desired. For very low power supplies, the circuit of Figure 3 would be satisfactory if an appropriate series impedance and capacitor were chosen. For example, the data of Table 1 shows that the 2100μF capacitor allowed only 27V of overshoot with a 500A pulse. This capacitor would be satisfactory if used in Figure 3 with the 0.5 ohm-100μH input network.

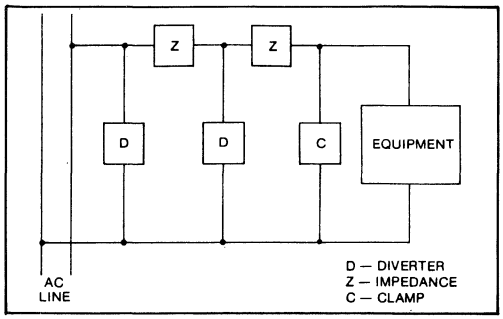

FIGURE 4—General topology for a protection network

A general topology for transient protectors is shown in Figure 4 using the notations of Jacobus. The diverter devices handle high currents but do not offer a precise control of voltage; gas tubes and metal oxide varistors (MOVs) are typical diverting elements. The clamp devices have lower impedance than the diverters but have lower energy handling capabilities. A TransZorb® Voltage Suppressor (TVS) Diode is a typical clamping device. The series impedances shown semi-isolate the various diverter and clamp stages by causing a voltage drop between them. To meet the requirements of IEEE 587-1980, Category B, and provide low output voltage clamping, the topology of Figure 4 has proven to be quite effective.

AN INTEGRATED RECTIFIER/SUPPRESSOR CIRCUIT

After some experimentation, the network of Figure 4 has been found to work quite well when the first diverter is a MOV, the first impedance is composed of the inrush current limiting resistance and an inductor, the second diverter is a silicon transient voltage suppressor and capacitor network, the second impedance is a series R-L circuit, and the clamping device is the filter capacitor.

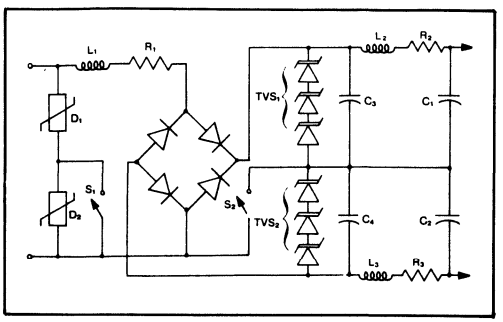

FIGURE 6—Circuit providing a high level of protection

Figure 5 (patent pending) shows a practical implementation of the circuit of Figure 4 which is virtually immune to transients. The resulting T filter network also attenuates high frequency noise in both directions, thus easing EMI filter requirements. Performance is shown in Table 3 when pulsed with 2500A. The resulting 25V peak transient appearing at the output is low enough to allow the use of 450V rated transistors in the power switching section.

Input	Peak Transient Voltage	Charge Voltage	Peak Capacitor Current
120V	9V	5V	103A
240V	25V	16V	163A

TABLE 3—Transient performance of the circuit of Figure 5
(Pulse Current ≈ 2500A, $L_1 = L_2 = L_3 = 100\mu H$, $R_1 = R_2 = R_3 = 0.5\Omega$ TVS Stack; 5KP60)

CONCLUSION

Only by ensuring a clean dc bus can a switching power supply be a reliable piece of equipment. Attention must be given to the lowly line rectifier and filter system to dramatically reduce line voltage transients. The circuit of Figure 5 provides a satisfactory clean dc level.

Reference

1. "Navy Power Supply Reliability—Design and Manufacturing Guidelines," NAVMAT P4855-1, Pg 27, NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
2. "IEEE Guide for Surge Voltages in Low-Voltage AC Power Circuits," IEEE Standard 587-1980, Institute of Electrical and Electronic Engineers, 345 E. 47th St., New York, NY 10017
3. Jon D. Paul and Bill Roehr, "The Use of Transient Voltage Suppressor Diodes With Power Mosfets," Official proceedings of the 9th International PCI '84 Conference, Intertec Communications, Inc. 2472 Eastman Ave., Unit 34, Ventura, CA 93003.
4. N.M. Jacobus, "Designing Power Line Transient Protection Circuits," Proceedings of Powercon 11, D-4 pp. 1-11., Power Concepts, Inc., P.O. Box 5226, Ventura, CA 93003.
5. William D. Roehr and O. Melville Clark, "AC Power Line Protection for an IEEE 587 Class B Environment," NASA Conference Publication 2356.

AN EFFECTIVE TRANSIENT AND NOISE BARRIER FOR SWITCHING POWER SUPPLIES

by
Bill Roehr
General Semiconductor Industries, Inc.

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Abstract

The power line transient environment and conduction emission requirements are described. Transient voltages on the DC output of off-line rectifier designs are shown. Various protection and filter schemes are discussed. An integrated rectifier/transient suppressor/EMI filter circuit is suggested as a cost effective means of rendering the DC bus virtually immune to power line (ac mains) transients as well as keeping EMI from the switching power supply out of the ac mains.

INTRODUCTION

Switching power supply designers are aware that the interface between the ac mains and the rectified DC bus must be designed to solve two problems:

1. Component failure caused by line voltage transients.
2. Excessive conducted noise into the mains.

Unexpected mains voltage transients are now being recognized as a significant factor in the failure of Switching Mode Power Supplies (SMPS). As stated in a recent United States Navy Publication[1]:

"The most predominant power supply failure modes are caused by peak instantaneous transients and subtle factors within and external to the power supply. . . The following is a list of key points to consider when designing and evaluating a switching-mode power supply design:

(1) Put voltage transient protection on the input power lines."

With the pulblication of IEEE Standard 587-1980[2], power supplies can be designed with assurance that failure caused by power line transients will be rare. The standard specifies that low impedances across the line in commercial and industrial environments should handle an 8/20 current waveshape (double exponential impulse, 8μs rise time, 20μs decay to half of peak) having a peak amplitude of 3000A. The reason for dealing with current is that lightning induced transients propagate through a system as a current source seeking a low impedance path to ground. Most designers presently do not make provision for the rectifier and filter system to handle pulse currents up to 3000A without producing excessive dc bus voltage, but a conservative design philosophy indicates that this should be done.

Since the emissions from switching power supplies can cause serious interference with broadcast and telecommunications services, governments have imposed conducted noise limits on equipment connected to the ac mains. Despite efforts to control the noise sources within the SMPS, filtering is needed at the power input terminals.

In an off-line switcher without transient voltage suppressor (TVS) devices, the ripple filter capacitor must handle the line to neutral transient pulse current. However, the charge delivered by the input transient and the voltage drop across the capacitor's ESL and ESR combine to develop an overshoot voltage. Given enough transient current, the overshoot is high enough to cause breakdown failures in the power switches connected to the DC output from the rectifier system.

The ripple filter capacitor also filters differential mode (line-to-line) noise to a degree. However, it is not adequate as a high frequency filter because of its ESL and ESR failing to allow equipment to meet the modern emission standards. In addition, the capacitor does nothing to reduce common mode noise which is usually the major EMI problem.

A common solution to the line transient problem is to add a transient voltage suppressor, usually a MOV, across the line and another MOV or two from neutral to ground and line to ground. However, to be effective, either an excessively large impedance must be placed between the MOV and the filter capacitor or an excessively large filter capacitor must be used.

The usual solution to the EMI problem is to add an ac mains filter to the power supply input. Often, on off-the-shelf item will permit compliance to the required agency regulations, but in some cases a custom design is required. Unfortunately, many filters cannot handle line transients without generating severe ringing or becoming damaged. The transient suppression and filtering requirements must be carefully coordinated if satisfactory results are to be obtained.

The material in the following sections will initially review the priciples of powerline transient suppression and filter circuits. Secondly, a way of integrating the two functions into a circuit which uses inductors to function both as current limiting impedances for transients and as filter reactors for EMI will be described.

REVIEW OF PROTECTION TECHNIQUES

The work in this paper is an extension of that reported in an earlier paper[3]. For completeness, the key findings and basic principles will be reviewed here and integrated into the newer material.

The voltage placed on the ripple filter capacitor by a transient consists of three components and is given approximately by Equation 1.

$$v_C = \frac{1}{C}\int i\,dt + iR_s + L_s\frac{di}{dt} \qquad (1)$$

where

C = input filter capacitance
i = pulse current
R_s = capacitor equivalent series resistance (ESR)
L_s = capacitor equivalent series inductance (ESL)
di/dt = rate of rise of transient current

Measured output voltage transients in the typical rectifier circuit of Figure 1 are shown in Table 1. The voltage components developed across R_S and L_S are essentially in phase with the current wave but the voltage caused by the charge persists for a relatively long time after the input transient has subsided. Both the peak voltage and the charge component are noted in the table.

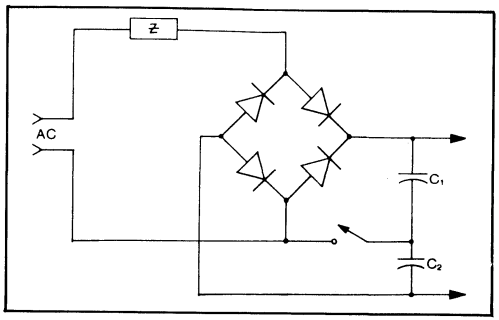


FIGURE 1—Basic line rectifier & filter for SMPS operating from 120/240 lines

Two values of impedance were used for Z. Z_1 consists of 10μH (from a circuit breaker) in series with a ½ ohm resistor while Z_2 consists only of a resistor. The small inductor caused a slight distortion of the 8/20 wave from the pulse generator as compared to the case when the ½ ohm resistor was used alone.

By studying the data in the table, several conclusions are evident:

1. The 240V input connection produces about twice the transient voltage than does the 120V connection. This is to be expected since the capacitors are connected in series.
2. What might appear to be minor differences in waveshape can produce significant differences in transient voltage. This also is not surprising; Equation 1 indicates that the rate of current rise and the area under the current waveform effect the peak transient voltage for a fixed level of peak current.
3. Even with a transient current of 500A, a commonly encountered value, the transients developed across the smaller filter capacitors could cause power switch failure, particularly if a high line condition were simultaneously encountered. At the 3000A level of the standard, the transient voltages would be 6 times the values in the table, spelling disaster for the power supply.
4. The larger the filter capacitor, the better the situation. This point is also obvious from Equation 1 and serves to explain why low-power personal computers and their peripherals have such a poor field service record.

C_1, C_2	Type	Input	Peak Transient Voltage		Charge Voltage	
			Z_1	Z_2	Z_1	Z_2
540μF	Mepco/Electra 319DA541T250AMA1	120V	39V	30V	30V	22V
		240V	75V	60V	58V	44V
650μF	Mepco/Electra 3120EA651T200BHA1	120V	33V	30V	23V	18V
		240V	65V	58V	46V	34V
2100μF	General Electric 44A417052M21	120V	12V	13V	7V	6V
		240V	27V	26V	16V	12V

TABLE 1—Transient performance of the circuit of Figure 1

($Z_1 = 10\mu H + 0.5\Omega, Z_2 = 0.5\Omega$)

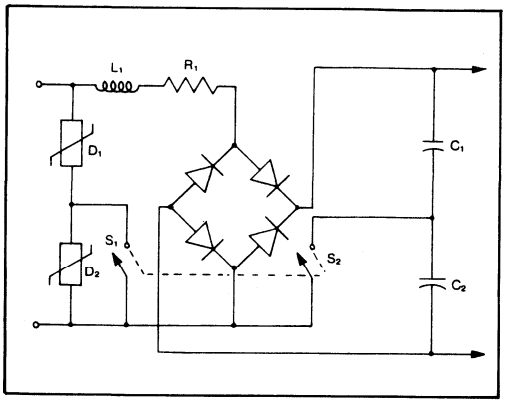


FIGURE 2—Basic circuit with MOV protection

Faced with this kind of evidence, many designers have concluded that transient voltage suppression devices are necessary. Quite often protection takes the form of little more than a single MOV across the line. Figure 2 shows another variation of the usual MOV protection circuit. In this circuit S1 provides a means to adjust the MOV voltage to fit the line voltage. If this is not done, a very large capacitor current flows when the input filter is configured for 120VAC operation. This is illustrated in Table 2 in the top row with S1 open and .5 ohm impedance. The large capacitor current produces a 77 volt spike across only one capacitor since the circuit operates as a voltage doubler; with 3000A of input current the spike would increase to 115V which could exceed the surge voltage rating of the capacitor. The 106 volt transient produced in the 240V circuit configuration increases to about 150 volts when 3000A is applied, bringing the bus voltage to 550 volts under a high line condition. A 550V bus is usually not acceptable.

To improve the transient suppression capability, the capacitor and/or the series impedance must be larger. Other data in Table 2 taken with higher series impedances shows some improvement in lowering the transient levels but the transients are still higher than desired. To obtain satisfactory transient performance with the circuit of Figure 2, it is necessary to further increase the series impedance and/or the filter capacitance. For example, the data of Table 1 shows that the 2100μF capacitor allowed only 27V of overshoot with a 500A pulse. This capacitor would be satisfactory if used in Figure 3 with a 0.5 ohm-100μH input network.

To improve transient suppression without using either excessively large series impedances or capacitors, a two-stage design proves to be cost effective. Further economies can be realized by placing the second stage TVS following the rectifier, because the output level is relatively constant regardless of whether 120V ac or 240V ac is applied to the input.

Figure 3 shows a practical circuit which is virtually immune to transients. The MOV TVS diverts most of the transient current back to the line. The series impedances limit the current available to the downstream devices. The TransZorb® avalanche diode TVS clamps at a low level which—together with the second inductor—prevents excessive transient current from entering the capacitor. When pulsed with 2500A, filter capacitor current measured 163A resulting in a 25V peak transient voltage appearing at the output. This level is low enough to safely allow the use of 450V rated transistors in the power switching section.

R1 - L1	input	S1	Peak Transient Voltage	Charge Voltage	Peak Capacitor Current
0.5Ω - 0μH	120V	Open	77V	54V	1080A
		Closed	24V	21V	440A
	240V	Open	106V	78V	780A
0.5Ω - 100μH	120V	Closed	18V	10V	190A
	240V	Open	74V	47V	440A
1.0Ω - 100μH	120V	Closed	12V	7V	130A
	240V	Open	53V	34V	300A

TABLE 2—Transient performance of the circuit of Figure 3

($R_1 = 0.5\Omega$, $C_1 = C_2 = 540\mu F$, Peak Pulse Current = 2000A)

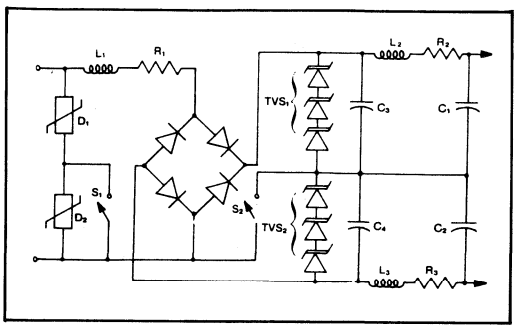


FIGURE 3—Circuit providing a high level of protection

LINE FILTER TOPOLOGIES

It is obvious that the network of Figure 3 also can serve as a high pass filter if capacitors are placed across the diverter and clamping devices. Under ideal matched conditions, rolloff is 24dB/octave, but should be at least 18dB/octave when working into powerline impedances. This type of filter characteristic has been shown to be usually adequate if common mode filtering is also provided.

A recent paper[4] has shown the frequency rejection characteristics of various filter connections when driven with a switching power supply. The circuit of Figure 4 with the common mode coil facing the power supply, proves to be the most useful topology for switchers, although it is not a commonly used configuration. In order for it to serve also as the topology for transient suppression, the common mode inductor must be designed to have a specific value or leakage inductance, or discrete inductors must be added in series with each coil as shown.

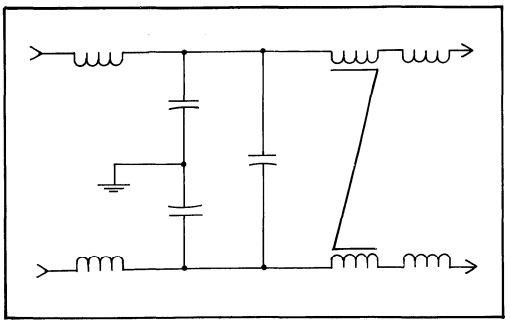


FIGURE 4—Useful filter topology for switchers

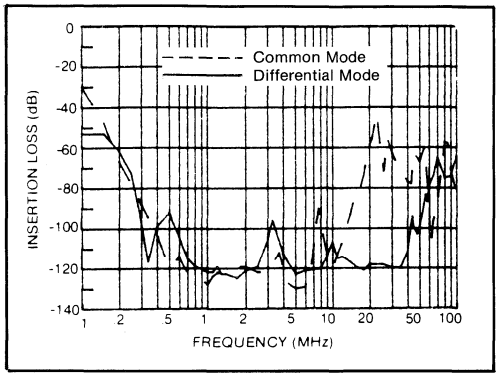


FIGURE 6—Insertion loss for circuit of Figure 5

TRANSIENT & NOISE BARRIER

Using the suppressor topology of Figure 3, and the filter topology of Figure 4, the circuit of Figure 5 results. It is a bi-directional noise and transient barrier for switchers. Although the values used are somewhat different from that described in the earlier paper, the transient performance is similar. With a 3000A, 8/20 pulse on the ac input, the transient output voltage on the filter capacitors was a mere 10 volts. Common mode voltage (i.e., 3000A input on both ac lines with respect to ground, output from dc plus voltage to ground) only exhibited a 3 volt transient.

Frequency response of the filter constructed on a lab breadboard is shown in Figure 6. For differential mode tests, the ac mains were terminated with 50 ohms. The input RF signal was applied to the dc (+) and the (-) terminals with the ripple filter capacitors removed. For common mode tests, the ac lines were connected together. Output voltage was read across 50 ohms connected between the ac inputs and ground. Attenuation exceeds 120dB over a wide frequency range. The design challenge in a filter is to have well designed broad-band coils. They must maintain their inductance into the low frequency range and be wound to minimize shunt capacitance. The cut-off frequencies can of course be easily altered by changing the values of the common mode capacitors C_1 and C_2, or the differential mode capacitors C_3 and C_4.

Parts	Values/Manufacturer's Part Number
C_1 - C_2	.005μF, 600V
C_3 - C_4	.1μF, 600V
L_1 - L_4	50μH - Dale
L_{cm}	1.2mH - Coilcraft E3495
M_1 - M_4	V130LA20 - G.E.
R_1 - R_4	0.5 Ohm, 2W
TZ_1 - TZ_2	3 - 1.5KE75A - General Semiconductor Ind.

TABLE 3—Parts list for circuit of Figure 5

CONCLUSION

Only by ensuring a clean dc bus can a switching power supply be a reliable piece of equipment. Attention must be given to the lowly line rectifier and filter system to dramatically reduce line voltage transients. To meet government imposed conducted noise requirements, powerline filtering is needed. Most cost effective transient and noise reduction can be achieved by a circuit which integrates the rectifier/filter, voltage limiting and high frequency filtering into a single circuit module.

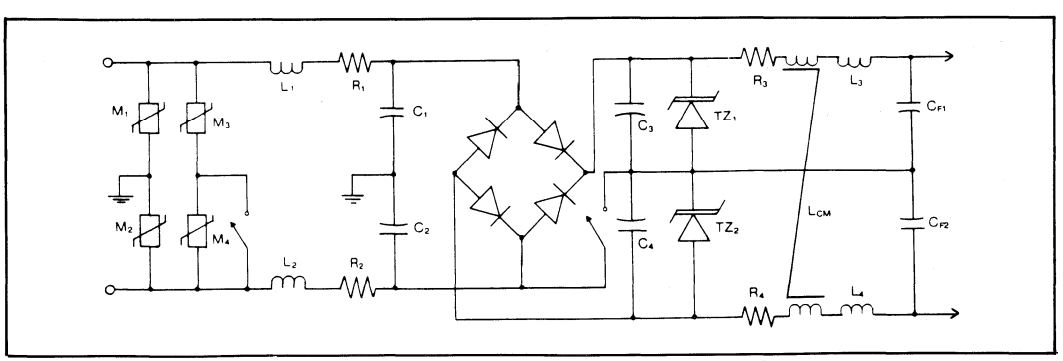


FIGURE 5—Complete circuit for a bidirectional transient and noise barrier integrated with the rectifier/filter system

References

1. "Navy Power Supply Reliability—Design and Manufacturing Guidelines" NAVMAT P4855-1, Pg 27, NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
2. "IEEE Guide for Surge Voltages in Low-Voltage AC Power Circuits," IEEE Standard 587-1980, Institute of Electrical and Electronic Engineers, 345 E. 47th St., New York, NY 10017.
3. Bill Roehr, "Hardening Power Supplies to Line Voltage Transients," Power Conversion & Intelligent Motion, June, 1986.
4. Ralph H. Queen, "Common or Differential Mode Noise? It Makes a Difference in Your Filter," EMC Technology, July-September, 1985.

A COMPARISON OF LOW VOLTAGE METAL OXIDE VARISTORS (MOVs) VS TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS

In 1975 General Semiconductor Industries, Inc., published the first comparison report of TransZorb TVSs versus metal oxide varistors. At that time the lowest voltage devices compared were rated at 33 volts.

Since then, as semiconductor memories and microprocessors have gained much wider acceptance in the marketplace, there have been many requests to compare the clamping voltage characteristics of 18 volt Metal Oxide Varistors to equivalent silicon avalanche devices.

The Metal Oxide Varistor cannot be directly cross-referenced to the TransZorb TVS. The purpose and function of both are identical. They can, in some applications, be placed in the same points for electronic circuit protection, but each product is specified differently — the application determines the actual product selection.

Metal Oxide Varistors originally developed by Matsushita Electric, are normally classified as a nonlinear resistor or a voltage dependent resistor. The product is a sintered ceramic material, consisting of zinc oxide as a primary ingredient along with several other metal oxide additives.

TransZorb TVSs are silicon PN junction transient voltage suppressors that are characterized by their sharp avalanche characteristics,phenomenal surge handling capabilities, ex-tremely fast response time (theoretically 1 x 10^{-12} second), and low resistance (R_{on}).

The most important electrical characteristic of a transient voltage suppressor is its clamping response, which includes both response time and clamping voltage.

A true comparison comes from the actual evaluation of both product types in a surge environment. Here the surge handling capability can be directly related to their response characteristics. Then and only then can one determine whether or not the product is adequate for protection of voltage sensitive circuitry, such as integrated circuits.

TEST PROCEDURE

To perform this comparison test, we selected a 1 Joule and a 3 Joule 18 volt Metal Oxide Varistor and compared it to three types of TransZorbs.

1. 18 Volt, 600 Watts
2. 18 Volt, 1500 Watts
3. 18Volt, 5000 Watts

The response curves for each device were recorded on a memory oscillograph. Figure 1 is a block diagram of our test equipment. Table 1 is a summary of the test results. Photographs depicting the actual response are shown on the following page.

Each device was energized with a 1 milliamp current. To obtain the expanded oscillograph, we used the actual breakdown voltage (BV) of the device under test as the base-line reference. The vertical sensitivity of the oscilloscope was 5 volts per division. We then superimposed a 20 μs surge pulse on the "device under test." The pulse amplitude was sequentially increased from 1 amp to 2 amps, 5

FIGURE 1—TEST DIAGRAM

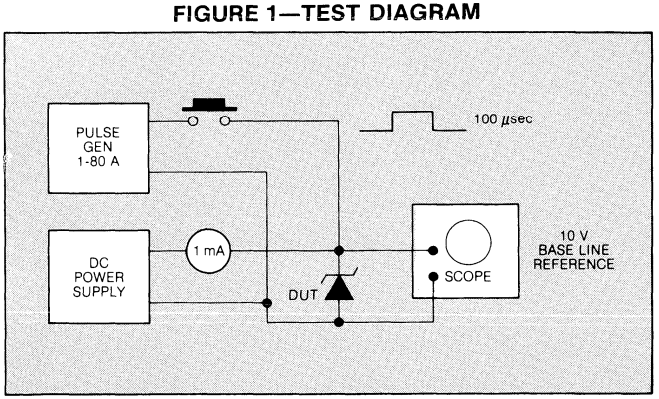


TABLE 1—SUMMARY OF TEST RESULTS

Type	Breakdown Voltage @ 1mA	Clamping Voltage @ Ipp in Amps							Δ Volts 1 mA to 80 Amps
		1	2	5	10	20	40	80	
18V 1 Joule MOV	16.79	29.8	32.0	35.8	39.8	45.1	51.8	Off Scale	>40V
18V 3 Joule MOV	17.30	31.3	33.8	36.1	38.6	41.3	45.3	48.3	31V
18V 600W TransZorb	17.60	17.9	17.95	18.10	18.25	18.60	19.25	20.0	2.4V
18V 1.5KW TransZorb	17.60	17.77	17.80	17.90	18.00	18.20	18.56	19.20	1.6V
18V 5KW TransZorb	21.0	21.28	21.33	21.41	21.50	21.61	21.80	22.03	1.03V

TransZorb® is a registered trademark of General Semiconductor Industries, Inc.

amps, 10 amps, 20 amps, 40 amps and 80 amps. The pulses were at 1 minute intervals.

A change in clamping voltage over the range of pulses is caused by both the resistance of the device and the thermal characteristics. Metal Oxide Varistors have negative thermal coefficients. TransZorb TVSs, on the other hand, have positive temperature coefficient.

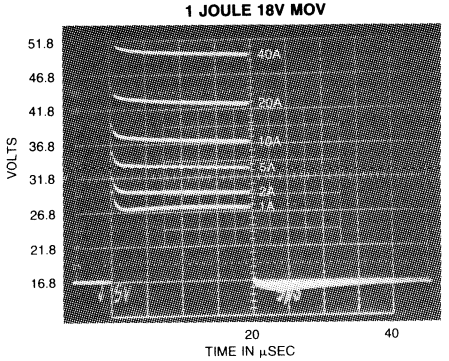
TEST RESULTS

The 1 Joule 18 Volt MOV device exhibited a breakdown voltage of 16.79 volts at 1 milliamp. At 1 amp, the device was clamping at 29.8 volts. At 4 amps, the device was in excess of 51.8 volts. At 80 amps, the response curve was beyond the range setting of the oscilloscope.

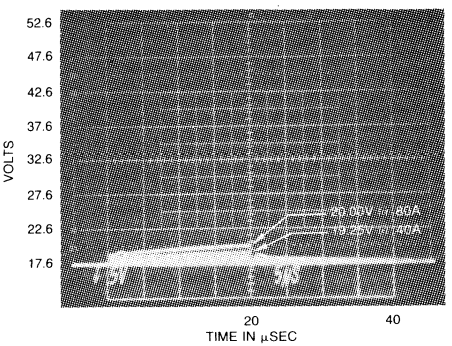
The 3 Joule, 18 Volt Metal Oxide Varistor had a breakdown of 17.3 volts at 1 milliamp and a clamping voltage of 31.3 volts at 1 amp, and 48.3 volts at 80 amps.

A picture is worth a thousand words. The photographs of the oscillograph of the response characteristics of the three types of TransZorb TVSs clearly speak for themselves. The most important parameter of transient voltage suppressors are the clamping characterisics. The true judgement value is the clamping voltage. Before you buy, COMPARE. . . Before you use, TEST.

1 JOULE 18V MOV

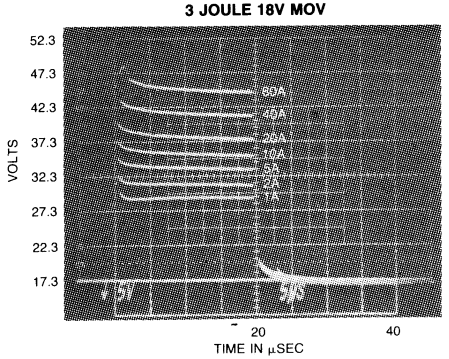


600W 18V TRANSZORB TVS

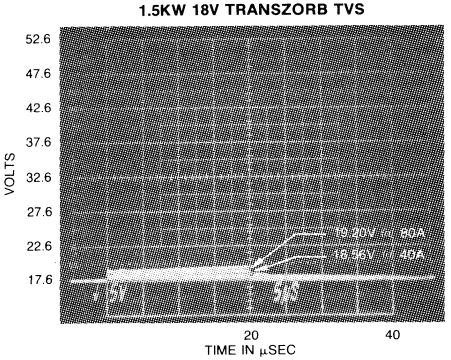


DEPICTS ALL 7 PULSES 1 AMP THRU 80 AMPS

3 JOULE 18V MOV

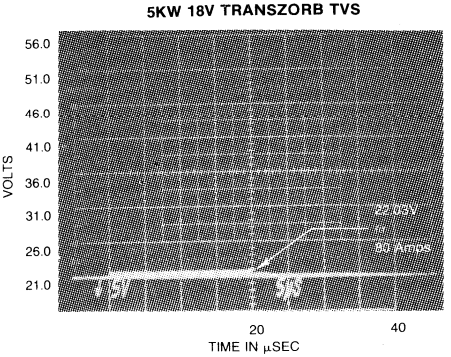


1.5KW 18V TRANSZORB TVS



DEPICTS ALL 7 PULSES 1 AMP THRU 80 AMPS

5KW 18V TRANSZORB TVS



DEPICTS ALL 7 PULSES 1 AMP THRU 80 AMPS

A COMPARISON OF ZENER DIODES VS TRANSZORB® TRANSIENT VOLTAGE SUPPRESSORS

(A New Approach)

TransZorb Transient Voltage Suppressors (TVS) are silicon P-N junction devices which have been *"designed, manufactured, specified, and tested"* as transient voltage suppressors. TransZorb TVSs are characterized by their surge handling capability, fast response time, and low clamping voltage vs their small physical size.

Zener diodes are *"designed, manufactured, specified and tested"* as voltage regulators.Zener diodes inherently have a certain amount of surge capability, however, in most instances, the surge handling capability is not a specified parameter, and in situations where it is, its capability is normally characterized as typical.

Different Zener diode manufacturers use different manufacturing techniques in the formation of the junction. Both the process and the junction size are directly related to the surge performance, therefore, a standard JEDEC device purchased from one manufacturer may not have the same surge performance as the original prototype.

If zener diodes are going to be used in surge applications, the surge should be a specified parameter and part of the vendor qualification procedure.

A true test of comparison comes from actual evaluation of both zener diodes and TransZorb TVSs in the surge environment. As stated earlier, zener diodes do have surge handling capabilities, but are their response characteristics sufficiently adequate to protect the voltage sensitive circuitry???

TEST PROCEDURE

To perform this comparison, we selected a series of zener diodes from various manufacturers and subjected them to a family of pulses. The response curves for each device were recorded on a memory oscilloscope. Figure 1 is a block diagram of our test setup. The following page contains the actual photographs.

Our test program consists of 5 types of 10 V zener diodes ranging from 400 mV to 10 W and a 10 V TransZorb in a 1 W axial lead package. Each 10 V zener was energized with a 1 milliamp current and the oscilloscope used this 10 V reference as the base line. The vertical sensitivity of the oscilloscope was 1 V per division. We then superimposed a 100μs pulse on the "diode under test." The test pulse was sequentially increased from 1 amp, 2 amp, 5 amp, 10 amp, 20 amp, 40 amp to 80 amps or until the device failed. The pulses were at one minute intervals.

FIGURE 1—TEST DIAGRAM

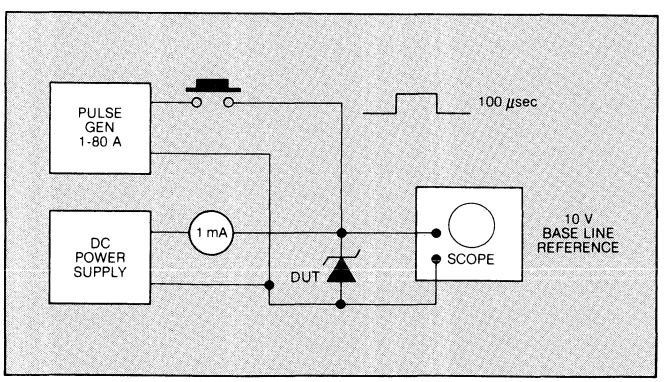
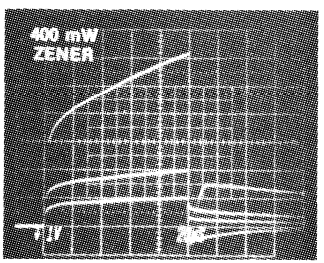


TABLE 1—SUMMARY OF TEST RESULTS

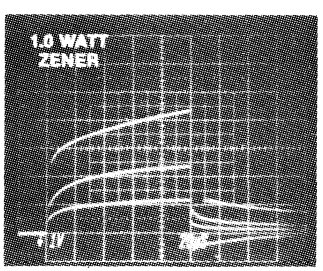
Type	Breakdown Voltage	Clamping Voltage @ Ipp in Amps							Mfg.
		1	2	5	10	20	40	80	
.4 W	10	11.0	12.0	16.2	*F	—	—	—	F
1.0 W	10	11.2	12.4	14.3	*F	—	—	—	I
2.0 W	10	11.6	12.2	13.3	15.3	F	—	—	T
5.0 W	10	10.4	10.5	11.0	11.9	13.9	F	—	U
10.0 W	10	10.3	10.4	10.6	10.9	11.6	12.9	F	I/
1.5 K 10 A 1.0 W	10	10.2	10.2	10.3	10.4	10.5	10.7	11.0	GSI

*F—Failed

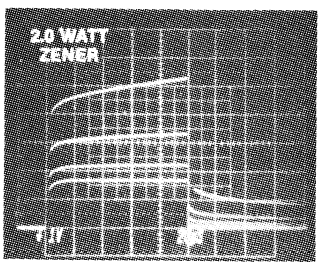
The change in clamping voltage is caused by both the resistance of the device and the thermal characteristics. The higher the slope, the higher the thermal performance.



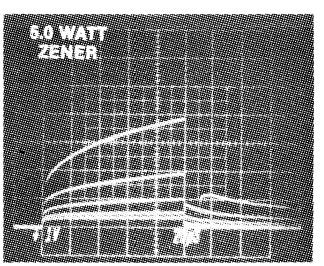
The 400mW, 10 V zener was subjected to a 1 amp, 2 amp and 5 amp pulse. The clamping voltage at the end of 100μs, 5 amp pulse was in excess of 16 V. Note the increase of the breakdown voltage caused by the thermal rise of the junction that occurs at the end of the 100μs pulse. This device failed when subjected to a 10 amp pulse.



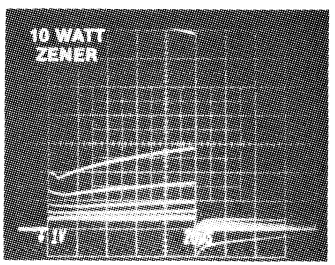
Depicts the 1 W, 10 V zener diode. There is a significant difference in the thermal slope of the clamping voltage due to the improved heat seeking capabilty of the 1 W package, however it is interesting to note that the dynamic resistance of this device is considerably higher than that of the 400mW zener indicating a smaller junction area. This device failed under the 10 amp pulse.



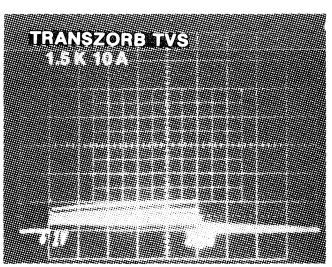
Depicts a 2 W, 10 V zener diode being subjected to 1 amp, 5 amp and 10 amp pulses. The unit failed at 20 amps. Again, it is interesting to note the difference of dynamic resistance and the thermal response curve which is appreciably different than the other two manufacturers. Packaging techniques do make a difference.



Depicts a 5 W "surge" rated zener diode. The clamping voltage at 20 amps was approximately 14 V. The device failed when subjected to a 40 amp pulse.



Depicts a 10 W zener diode. The discontinuity at the leading edge of the waveform is caused by package inductance where V is equal to $L_{di/dt}$. It is interesting again to compare the change caused by the thermal rise after the 100μs pulse. This device failed when subjected to 80 amps.



Depicts the 1.5K 10A TransZorb TVS over the entire family of pulse through 80 amps. The unit under test exhibited a clamping voltage of 11 V. The trailing curves also indicate the superb thermal characteristics of the package.

SUMMARY

Without a doubt, this series of tests graphically depict the differences between a zener diode and a TransZorb TVS. Transient surges caused by both the induced effects of lightning or by direct static discharge lie within the 40 to 80 amp spectrum, and therefore, the tests are applicable to actual environments.

DYNAMIC SATURATION
ITS CAUSE AND MEASUREMENT

by
William D. Roehr
General Semiconductor Industries, Inc., Tempe, Arizona

Published in May "Power Conversion International," P.O. Box 2889, Oxnard, California 93034. (Appendix added.)

As the name implies, quasi-saturation is a region of transistor operation in which the transistor is partially saturated. It appears on the conventional output characteristic as a transitional region (B) between the linear region (A) and the hard saturation region (C) as shown on Figure 1. Region B becomes more pronounced as the voltage capability of a transistor is increased. The region is characterized by a current gain (h_{FE}) and transition frequency (f_t) which are highly voltage dependent, and decrease rapidly as the voltage approaches the hard saturation region.

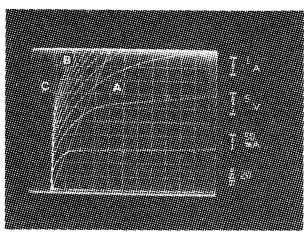


FIGURE 1

Transistor Output Characteristics. Showing three operating regions.

A: Linear
B: Quasi-saturation
C: Hard Saturation

Quasi-saturation is a natural but unwanted byproduct of the processes used to fabricate high voltage bipolar transistors. The collector region must be much wider than that of a low voltage device in order to contain the depletion region required by the high resistivity material used to obtain the desired breakdown voltage. In the on-state, this wide high resistivity collector region appears as a significant resistance; consequently evidence of saturation (the line between regions A & B on Figure 1) appears at voltages much higher than with low voltage transistors. However, as saturation begins, the collector region accumulates charge which effectively lowers the collector resistance, i.e. conductivity modulation occurs. As base drive is futher increased, the modulation process continues until the fully modulated condition of hard saturation is achieved (the line between regions B & C on Figure 1).

Because the gain-bandwidth product or transition frequency (f_t) decreases with decreasing voltage, the switching waveform of high voltage transistors noticeably departs from that observed with low voltage devices. One effect[1] is a change to lower slope on the turn-on waveform as the quasi-saturation region is traversed. Figure 2 dramatically illustrates this behavior.

In circuits where the current is close to the on-state value during this period of quasi-saturation, the power loss may be significant at high operating frequencies. A similar effect occurs at the time of turn-off where the waveform illustrates a slowly increasing slope prior to the point where rapid turn-off commences.

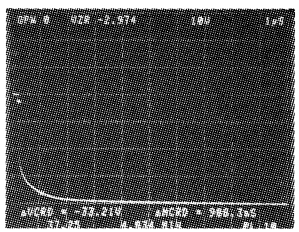


FIGURE 2

Rise Time: 90% to 10% in a 40 Volt Resistive Load Circuit. $I_c = 10A$

The response in region B is often referred to as dynamic saturation. When it needs to be controlled, it is sometimes specified as a maximum voltage level at a specified time from application of the input pulse. To avoid errors caused by scope preamp overload recovery and drift, however, it is better to specify the voltage indirectly by measuring time as in a conventional rise time test. The performance in the quasi-saturation region is emphasized by using a low collector supply voltage.

The waveform of Figure 2 was taken for a circuit having a collector supply of 40V. The time for the collector voltage to drop to 4 volts reads out at 0.908μs. The same waveform on a different time scale (Figure 3) indicates that an additional 8.1μs is required for the voltage to drop to 2% of the initial 40V level. At the 2% point, the saturation voltage is still 0.8 volts above the dc level of 0.735 volts. Steady state is not achieved until another 4.22μs has elapsed. Therefore, even for the very fast GSRU15040 transistor, it is evident that a dc $V_{CE(sat)}$ test is not very meaningful for applications where the repetition frequency exceeds 50KHz.

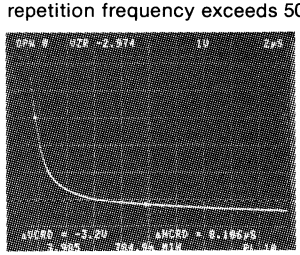


FIGURE 3

Rise Time: 10% to 2% in a 40 Volt Resistive Load Circuit. $I_c = 10A$

Data for several lots of GSRU15040 and some similar competitive transistors is shown in Table 1. It is evident that a fairly wide distribution occurs and that Brand X is

[1]Several deleterious effects occur with the high voltage structure, which are fully explained in an excellent paper by W. R. Skanadore: *"Toward an Understanding and Optimal Utilization of Third Generation Bipolar Switching Transistors"*, Proceedings of INTELEC 1982 pp196-203, IEEE, 445 Hoes Lane, Piscataway, NJ 08854. IEEE Catalog No. 82CH 1818-4.

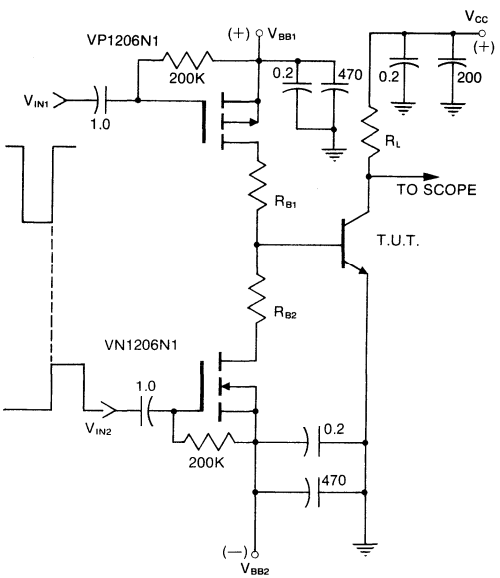
TABLE 1 Transistor Data					
Type	**T_c**	**Fastest**	**Average**	**Slowest**	**Unit**
GSRU15040	25° C 100° C	702 1246	937 1490	1195 1844	ns ns
Brand X	25° C 100° C	836 1406	1293 2082	1824 2940	ns ns

considerably slower than the GSRU15040. Higher temperatures also increases the time; 100° C readings are approximately 1.5 to 1.6 times higher than 25° C readings for the GSRU15040 and 1.6 to 1.7 times higher for Brand X.

During testing, it was observed that dynamic saturation is particularly sensitive to variations in base drive waveform and amplitude so that comparisons between transistors must be performed using the same circuits.

APPENDIX

DYNAMIC SATURATION TIME TEST CIRCUIT



NOTES:

1. Capacitance values in μFd.
2. For measurements shown in this note:
   $V_{CC} = 40V$, $R_L = 2.67\Omega$, $V_{BB1} = 12V$,
   $R_{B1} = 3.6\Omega$, ($I_{B1} \simeq 3A$), $V_{BB2} = 6V$,
   $R_{B2} = 1.8\Omega$, ($I_{B2} \simeq 3A$).
3. R_L is composed of two 5.6Ω Dale NH-50 (Non-inductive, 50W) resistors in parallel. The exact value is obtained by trimming with 2 watt carbon resistors.
4. Proper circuit performance is only achieved by a circuit layout which minimizes lead inductance. The emitter of the T.U.T. must be the ground focal point. To minimize stray coupling, a double sided P.C.B. is suggested for the driver stage.
5. View the voltage across power supply lines and adjust bypassing so that ringing is a small percentage of signal levels. Sprague Extralytic® and metalized stacked film capacitors are used for supply bypassing.
6. Base current should be viewed with a current probe. It may be necessary to bypass R_{B1} to achieve a flat topped current pulse.
7. Ground loops through the scope and pulse generator must be avoided. A differential amplifier scope input is often the best solution when a ground loop is encountered.

METHODS FOR UTILIZING HIGH-SPEED SWITCHING TRANSISTORS IN HIGH-ENERGY SWITCHING ENVIRONMENTS*

by William R. Skanadore, General Semiconductor Industries, Inc.

INTRODUCTION

The advent of switching power conversion has brought with it a whole new set of problems not usually encountered when dealing with linear power supplies. When it became obvious that smaller, lighter, and more efficient power conversion units would have to be made available to military and industrial markets, power conversion engineers set out to examine those aspects of reliability, performance and cost which had theretofore discouraged the development of competitive switching power supplies.

It became apparent at once that most of the inherent problems with such supplies could be attributed to inadequate or unavailable components and subsystems. These needs were communicated to the components industries, who, for the most part, have responded well. As of this writing, complete control subsystems on a single chip are available from several manufacturers, the quality and performance of passive components are constantly being improved, and the power semiconductors used in such supplies are more nearly compatible with the demands made of them than ever before.

Yet, there still seems to be much confusion with regard to transistor safe area of operation ratings. Much of this confusion stems from the fact that as yet, power transistor manufacturers have not produced a rating system suitable for use in the switching environment.

Upon scrutinizing the available information supplied with power transistors, it becomes apparent that there is even some disagreement with regard to existing definitions and testing methods.

The purpose of this work is *not* to present standards and definitions, for they do not as yet exist. Herein *will* be presented some current insights into the failure mechanisms associated with high-speed switching transistors and offer what *may* be useful countermeasures for those seeking to produce workable power systems with enhanced reliability.

RESISTIVE VS. INDUCTIVE SWITCHING — THE GROUND RULES

At the risk of appearing somewhat contrary, it will be necessary at the outset to present, for reference within, a brief recapitulation of switching waveforms.

Shown in Figure 1 is the standard time domain resistive switching waveforms which have been with us for many years and are well-defined. [1]

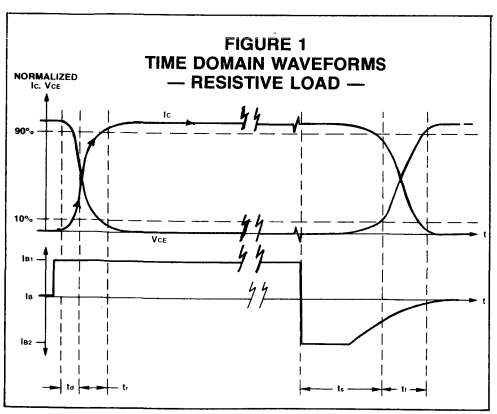


FIGURE 1
TIME DOMAIN WAVEFORMS
— RESISTIVE LOAD —

Somewhat less well-defined, as pointed out earlier, are the inductive switching waveforms shown in Figure 2. Here, it is assumed that operation of the NPN device is in a *clamped* inductive switching circuit similar to that shown in Figure 3, where V_{CE}, I_C, I_{B1}, I_{B2} and V_{BE} (off) can be varied.

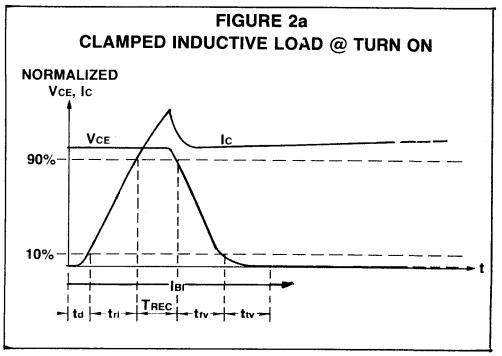


FIGURE 2a
CLAMPED INDUCTIVE LOAD @ TURN ON

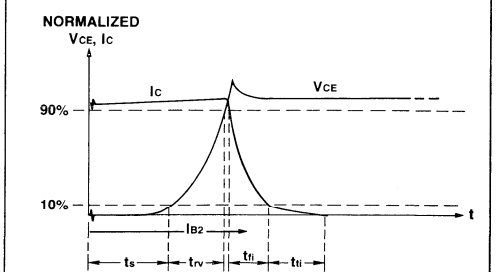


FIGURE 2b
CLAMPED INDUCTIVE LOAD @ TURN OFF

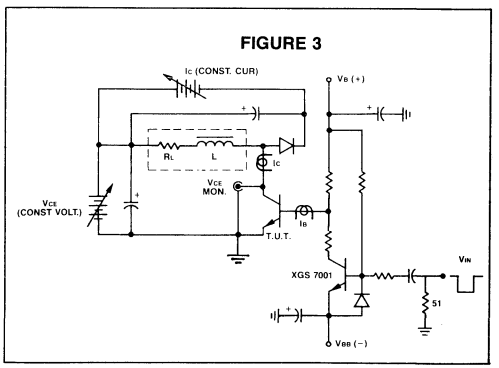


FIGURE 3

Table I gives a brief description of the various waveform components and the parameters with which they can be associated. Again, be advised that this nomenclature is *not* universal and the "ground rules" will have to be verified in any communicative situation for the time being.

*Originally presented at "Proceedings of Powercon 4," May 14, 1977

TABLE I

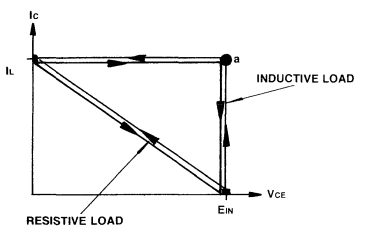
Symbol	Description	Asssociated with: Current	Voltage
t_d	Delay time	0 → 10%	
t_{ri}	Current Rise time	10 → 90%	
t_{fv}	Voltage Fall time		90 → 10%
t_{tv}	Voltage Tail-in time		10 → 2%*
t_s	Storage time		0 → 10%
t_{rv}	Voltage Rise time		10 → 90%
t_{fi}	Current Fall time	90 → 10%	
t_{ti}	Current Tail-out time	10 → 2%*	
T_{Rec}	Property of the environment	> 100%	100%

*A more stringent lower limit may be desirable in the case where ttv ≫ tfv and/or tti ≫ tfi as significant parcels of energy can be dissipated during ttv and tti.

THE SWITCHING LOAD LINE — A BRIEF ENCOUNTER

Shown in Figure 4 are the idealized switching load lines for both resistive and clamped inductive loads.

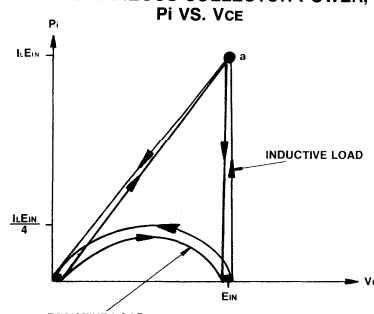
FIGURE 4
IDEALIZED SWITCHING LOAD LINES



Several general features of these load lines should be noted. The resistive load line transition allows for a very well-behaved, continuous transfer of power to and from the load, where the instantaneous collector power is a parabolic function of V_{CE} peaking at $E_{IN/2}$ and having a maximum value of $\frac{(E_{IN})(I_L)}{4}$.

On the other hand, the inductive load line presents an unforgiving set of switching conditions to the switching element and potentially to its environment. There exists at point "a" in Figure 4 simultaneously a maximum I_C and V_{CE} wherein instantaneous collector power is four times its resistive counterpart at twice the collector-emitter voltage! (Refer to Figure 5.)

FIGURE 5
INSTANTANEOUS COLLECTOR POWER, Pi VS. VCE



The problem at point "a" is further compounded in the case of the non-ideal environment where the unavoidable effects of stray inductance, leakage reactance, and circuit recovery phenomena may be magnified by the extremely fast response times of the high-speed switch.

Depicted in Figures 6–11 are six of the most popular types of switching regulators and regulator/converter circuits. Illustrated beneath these circuits are more pragmatic versions of the applicable switching load line which take into account some of the natural effects (shaded areas) discussed in the last paragraph.

FIGURE 6a
SERIES REGULATOR

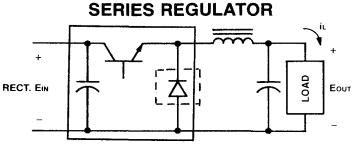


FIG. 6b

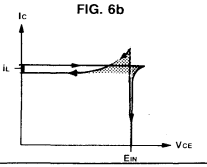


FIGURE 7a
FLYBACK REGULATOR

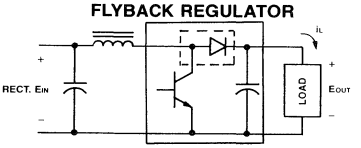


FIG. 7b

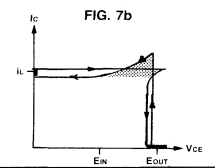


FIGURE 8a
HALF BRIDGE REGULATOR/CONVERTER

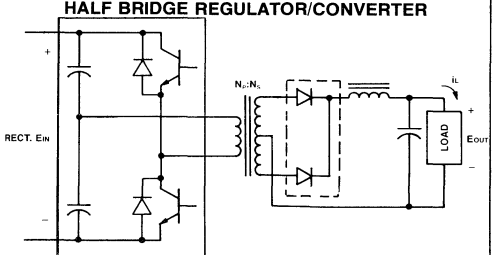


FIG. 8b

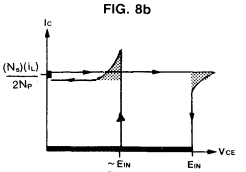


FIGURE 9a
FULL BRIDGE REGULATOR/CONVERTER

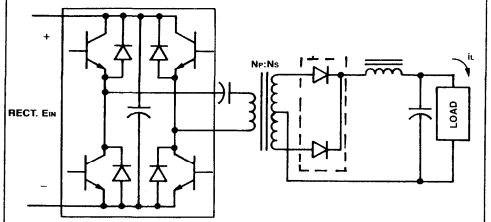


FIG. 9b

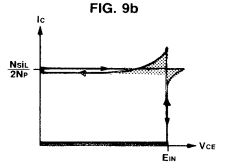


FIGURE 10a
ISOLATED FLYBACK REGULATOR

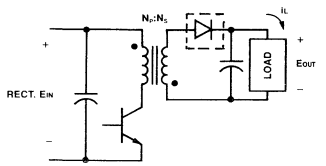


FIG. 10b

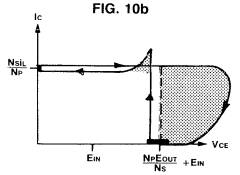


FIG. 11a
PUSH-PULL REGULATOR/CONVERTER

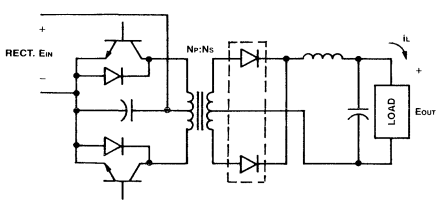
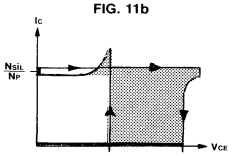


FIG. 11b



The bold black areas near the axis are representative of normal excursions of the switch while it is on (saturation) or off between switching events.

With regard to the switching load line, these six basic configurations can be segregated into *two* groups. The first group is characterized by a load line in which the "voltage spike" at *turn-off* due to the inductive nature of the environment can be effectively terminated by judicious layout and component selection within the solidly encircled areas of Figures 6-a through 9-a, inclusive.

The second group can be characterized as inherently difficult to control during turn-off due to the isolated nature of the terminating diode clamp and interposed transformer leakage reactance (see Figures 10 and 11).

TABLE II

DISPOSITION OF $LI^2/2$* (Magnetization Energy at Turn-Off)

Type I Regulators	**Type II Regulators**
Energy Efficiently returned to supply, E in:	*Energy Dissipated* in Switch or in "Energy-Snubber"
(forward regulators)	
Series	*Isolated Flyback*
Half Bridge	*Push-Pull*
Full Bridge	
Energy *Efficiently* sent on to Load, E out:	This type of dissipative and stressful power supply should be avoided whenever possible.
Flyback	
Series	

*L will include "stray" inductance (wiring and components) and leakage reactance (transformer circuits) as well.

Everything done to minimize L in the neighborhood of the switch will heighten the stress on this device at turn-on. If there *were* some residual inductance, the high-speed switch would tend to partially collapse V_{CE} during t_{ri}. This phenomenon is routinely observed at turn-on where di/dt will exceed 10^8A/sec. A quick tabulation using this number will show that sub-micro Henry inductance can have a profound effect at turn-on. The imperfect character of the freewheel diode (encircled by dashed lines in Figures 6-a through 11-a) can be held accountable for current overshoot during turn-on. In addition to the normal component of load current that must be assumed by the switch, a charge must effectively be removed from this diode in the vicinity of 0 bias before t_{fv} can commence.

This charge will be due to minority carrier effects in the fast recovery rectifier (high voltage applications) and majority carrier capacitive influences of the Schottky rectifier (low voltage applications). In general, the Schottky effects will be transformer-coupled to the switch and for most practical transformer designs, the natural leakage reactance will tend to allow for substantial voltage (V_{CE}) collapse, preventing the current overshoot from occurring at extreme values of V_{CE}. Those instances where fast recovery rectifiers are isolated by the transformer can be treated in much the same way.

With respect to the high-speed switch, the aforementioned charge removal process is, of course, influenced by the rate at which this charge can be removed. When a fast-rising current wavefront is presented to the rectifier, the peak current achieved in the reverse direction through such a device will be highly dependent upon the current rise time (di/dt) and the "recovery" properties of the rectifier, so that the "recovery time" can be shortened at the expense of higher peak currents. In actual practice, the current overshoot in the transistor may greatly exceed the normal load-related collector current!

We are, therefore, faced with what seems to be a bilateral problem. We would like to minimize the inductance in the vicinity of the transistor to eliminate the voltage overshoot at turn-off. Concurrently we would like to reduce the current spike at turn-on by selecting a commutating rectifier with minimum $T_{REC}(Q_{Rec})$. Having examined this, we can now proceed to characterize the remaining problem.

THE SWITCHING PROBLEM — SECOND BREAKDOWN

Second breakdown in bipolar transistors has undoubtedly received more attention in the past 10–15 years than any other single aspect of this device. The cause/effect relationships are still a matter for debate, yet there remains one undeniable precept. Practically everything done to maximize speed in the power switching transistor is deleterious to second breakdown capability. [2] Unfortunately, the concurrent requirement for high-speed and second breakdown immunity appears to be especially noticeable in the realm of inductive switching. Here we encounter perhaps the worst of all possible combinations: a load line which constrains the device to simultaneous high-current, high-voltage transients, and a demand for minimum transition times.

The phenomenon of "second breakdown" can be divided into three circumstantial areas: forward biased base-emitter ($I_C > 0$, $V_{CE} < BV_{ceo}$); reverse biased base emitter ($I_C > 0$, $V_{CE} < BV_{cex}$); and $E_{S/B}$ (avalanche breakdown.)

1. **Forward Biased Second Breakdown:**

This particular problem has long been associated with lateral thermal instabilities which initially develop as a result of an unavoidable electrical imbalance on the surface of the transistor chip. The effect of this electrical imbalance is to cause portions of the base-emitter junction to become somewhat more forward biased than others. This results in a distribution of collector current which favors the more heavily biased areas. More collector power is generated in these areas, raising local temperatures and further lowering local base-emitter voltages.

This will result in a positive feedback or runaway condition commonly referred to as a hot spot which may or may not stabilize [3]. Higher collector-emitter voltage has an accelerating effect upon this as it will elevate the ability to produce more local power and therefore higher local temperatures for a given amount of collector current.

The capability of the transistor to withstand this condition is related in part to the effective thickness of the collector region where a thin collector normally implies lower capacity for forward biased S.O.A.

2. **Turn-Off Second Breakdown:**

This characteristic is by far the most commonly encountered mode of failure in inductive switching applications. The device is normally operated in such a way that I_{B2}, the reverse base drive, is made quite large in order to improve storage and fall times. Figure 12-a shows a cross-sectional view of a portion of a switching transistor under the influence of forward bias. The base area has associated with it a distributed resistance which will be greatest directly beneath the emitter, owing to higher average resistivity in this area and the narrowness of the base channel.

Under the influence of applied base current, I_{B1}, there will appear a cumulative voltage drop proceeding toward the center of the junction, due to the resistive nature of the base. This will selectively forward bias those areas of the emitter-base junction nearest the base contacts. Figure 12-b models this peripheral crowding effect with discrete devices and resistors.

FIGURE 12a
FORWARD BIASED CURRENT CROWDING EFFECTS

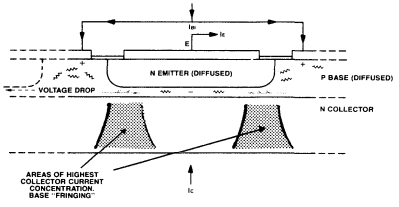
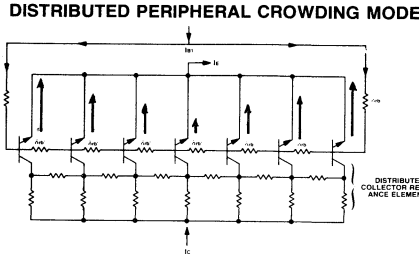


FIGURE 12b
DISTRIBUTED PERIPHERAL CROWDING MODEL



When this "device" is turned off by applying reverse base drive, I_{B2}, the resulting voltage drop in the base will tend to reverse itself with more positive values of voltage nearer the center of the base-emitter junction. (See Figure 13-a.) The turn-off of this junction will propagate inward toward the center until the remaining central regions cut off. The significant feature of this behavior is that at the final moments prior to cut-off, the current through the central regions rises sharply. Now when we allow the collector load to be essentially a constant current source up to some large value of V_{CE} (a typically "inductive" load) we can initiate the conditions necessary for avalanche injection.

FIGURE 13a
REVERSE BIASED CURRENT CROWDING EFFECTS

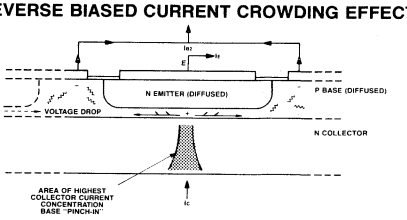
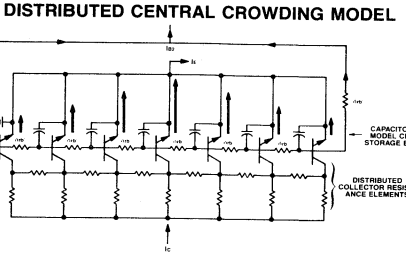


FIGURE 13b
DISTRIBUTED CENTRAL CROWDING MODEL



Simply stated, avalanche injection (or impact ionization) is a phenomenon which will occur in such a device when the electric field (volts/cm) in a portion of the collector exceeds some critical value beyond which the available carriers flowing in the collector will have sufficient energy under the influence of the large electric field to dislodge additional carriers from fixed locations in the collector, producing a veritable cascade of mobile charge in what may be a very small, highly conductive filament in the collector. Looking at this device from the outside world, we would notice at once an immediate drop in collector-emitter voltage to a value indicative of the size and conductivity of the "filament" (perhaps a few tens of volts) followed immediately by a total collapse of V_{CE} due to destructive heating effects in the vicinity of the filament.

This cause and effect relationship between avalanche initiated electrical breakdown and the ensuing thermal destruction of the device has only recently been established with any degree of certainty. Additionally, Hower et al [3] have recently proposed such a mechanism for the initiation of forward biased secondary breakdown.

Returning to our model of the transistor turning off the inductive load, we can establish a qualitative relationship, involving I_{B2}, which will serve to explain the existence of a very high electric field E_{CRIT} in the collector which cannot be explained in terms of V_{CE} alone. Normally, we would expect E to be much less than E_{CRIT} at the highest value of V_{CE} encountered in our application. However, when we constrict the collector current to a very small area at turn-off, we can actually cause the electric field to collapse in the vicinity of the collector base junction and rise sharply toward E_{CRIT} some distance away, deeper in the collector. In general, by increasing I_{B2}, we will achieve larger values of E, deep in the collector until we reach E_{CRIT}, at which time avalanche injection will occur. This phenomenon will occur in very thin collectors first and as collector width increases, the magnitude of I_{B2} required to initiate breakdown will also increase. "Rugged" transistors will avalanche, but at relatively high voltages and large values of I_{B2}. [5]

3. **$E_{S/B}$:**

The $E_{S/B}$ phenomenon is directly related to the above, where the requirements for high electric field are met in large part by high terminal voltages. This is a relatively useless parameter for circuit design as operating near the breakdown voltage BV_{cex} is generally considered risky at best.

Thus, we have seen that second breakdown capability and fast switching do not go hand in hand. Nevertheless, we can use the fast switching transistor if we treat the turn-off load line in such a way as to avoid simultaneous occurrence of high voltage and high current at turn-off.

For those interested in a quantitative study of avalanche injection, references [4, 6, 7, 8] will prove to be of value.

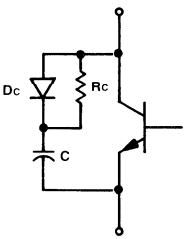
THREE SIMPLE SNUBBERS

1. **TURN-OFF: The Current Snubber** (Applies to Figures 6 and 7, and with modifications to Figures 8 and 9).

As stipulated earlier, the most critical portion of the switching cycle commences when reverse drive, I_{B2}, is applied at the base of the switch. In most *practical* applications, I_{B2} will have to be made quite large in order to minimize storage time and fall time under a wide variety of system conditions. The methods employed to provide this drive are anything but gentle. The results in many cases are predictably catastrophic.

In order to fully utilize the capability of the high-speed switch, we must eliminate at least one of the conditions conducive to avalanche injection. Ostensibly, there are two options: the transistor can be turned off into low values of V_{CE}, or the collector current can be diminished as the voltage rises. Reducing the collector current is undoubtedly the most realistic solution at turn-off, and will allow us the freedom to depress the turn-off load line excursion to any degree necessary for safety of operation. (See Figure 14.)

FIGURE 14
TURN-OFF (CURRENT) SNUBBER



A current "sink" will parallel the transistor and share current handling responsibility during the voltage rise period, t_{rv}. (See Figure 2-b.) An important result of this technique is that *efficiency will not be adversely impacted* since a fair portion of the power dissipated in the snubber would have otherwise been dissipated in the transistor. Additionally, this method will, in some cases, help to reduce RFI. [9]

Design Parameters:

$t_{rv(max)}$ and $t_{fi(max)}$ at

$I_{C(max)}$ and at

$V_{CE(max)}$ of Figures 6-b through 9-b (turn-off excursion)

f (frequency of operation)

$T_{on(min)}$ minimum switch *on* time

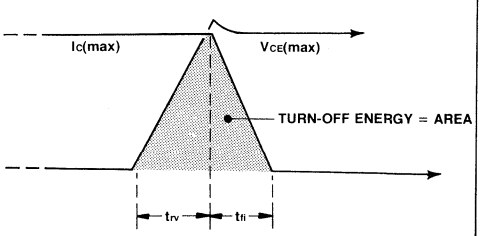
$$C_{(min)} = \frac{I_{c(max)}\,(t_{rv(max)} + t_{fi(max)})}{V_{CE(max)}} \qquad \text{A-1}$$

This is a quasi-empirical rule of thumb based upon the relationship:

$$E = \frac{CV_{ce(max)}^2}{2} \simeq \frac{I_{C(max)}\,V_{CE(max)}\,(t_{rv(max)} + t_{fi(max)})}{2} \qquad \text{A2}$$

(see Figure 15) and will guarantee that the current in the transistor will be reduced to near zero by the time V_{CE} has risen to $V_{CE(max)}$. ($I_{C(max)}$ is the maximum load related current.)

FIGURE 15
TURN-OFF ENERGY



In the limit as $t_{rv(max)} \gg t_{fi(max)}$, which is *not* unreasonable for high-speed devices driven off quite vigorously, it would seem that all of I_C could be channeled into the snubber capacitor. We might then state that since

$$i_{cap} = C \frac{dV_{CE}}{dt}$$

then:

$$C = \frac{I_{C(max)}\, t_{rv(max)}}{V_{CE(max)}}$$

$(t_{rv(max)} \gg t_{fi(max)})$

and the overall effect on efficiency would be negligible. However, due to the complex interdependence of I_C and V_{CE} during the turn-off transition, this may never be quite attainable.

In the limit as $t_{fi(max)} \gg t_{rv(max)}$ which is an inherent quality of "slower" transistors, then there exists the possibility of *improving* system efficiency by inserting a turn-off snubber as before. The transistor and snubber losses can be optimized at a level which will reduce turn-off power losses by 44% ($\alpha = \frac{2}{3}$) [10] while affording the power transistor some of the benefits of snubbing action. This analysis implies that:

$$C_{opt} = \frac{2\, I_{C(max)}\, t_{fi(max)}}{9\, V_{CE(max)}}$$

This is 78% smaller than the capacitor which would be used for the fast ($t_{fi} \simeq t_{rv}$) transistor and high current-high voltage conditions will prevail as V_{CE} will rise to $V_{CE(max)}$ before I_C has decayed to 0. However, with "slower" transistors, all of the *structural* conditions which fulfilled our initial requirement that $t_{fi} \gg t_{rv}$ will not be especially conducive to the onset of avalanche injection. So when slower devices are used, an attempt to improve switching efficiency will suffice.

Do not be misled by what seems to be a better alternative in using a slower device. In general, t_{fi} for these devices will be considerably longer than $t_{rv} + t_{fi}$ for the high-speed switch. This information was merely presented for those who cannot find a suitable high speed switch for their application or who would like to improve the efficiency of existing systems using the slow switch.

Returning from this digression, let us restate our empiricism:

$$C_{(min)} = \frac{I_{C(max)}\,(t_{rv(max)} + t_{fi(max)})}{V_{CE(max)}} \qquad \text{A-1}$$

We would prefer that the capacitor be essentially discharged (through R_C) at the end of $T_{on(min)}$.

$$R_{C(max)} = \frac{T_{on(min)}}{3C} \qquad \text{A-3}$$

$$[\text{from } V_{cap} = V_{CE(max)}\, \text{Exp}\, (-t_{on}/R_C C)] \qquad \text{A-4}$$

This will guarantee V_{cap} max prior to turn-off $\simeq 5\%$ of $V_{CE(max)}$.

Check that the turn-on current in the transistor due to the capacitor discharge, i_{dis}, is not a significant portion of $I_{C(max)}$.

$$i_{dis(max)} = \frac{V_{CE(max)}}{R_C} \qquad \text{A-5}$$

25% of $I_{C(max)}$ would be acceptable.*

If i_{dis} is too large, then R_C will have to be increased at the expense of snubber cut-in voltage. In other words, at the end of minimum T_{on}, the capacitor voltage (V_{cap}) will be higher and the capacitor will not sink current until V_{CE} rises to V_{cap} (see A-4). This will not severely impact operation of the snubber for reasonable changes in R_C.

Finally, the maximum dissipation of R_C is given by:

$$P_{R(max)} = \frac{C V_{CE(max)}^2\, f}{n} \qquad \text{A-6}$$

*Be aware that proportional base drive schemes may have to be treated separately.

n = 2: Figures 6 and 7.

n = 1: Figures 8 and 9. Actual values will lie between 1 and 2, depending upon the primary leakage inductance and duty factor where n = 1 is representative of most severe leakage reactance and lower duty cycle operation.

It is interesting to note that for duty cycles approaching 100% on the bridge convertors (Figures 8 and 9), n will be close to 2 regardless of leakage reactance. The preregulated convertor presented by Calkin ahd Hamilton [11] lends itself very well to this application. By operating a full bridge inverter at essentially 100% duty, they have also circumvented the troublesome problem of transistor turn-on current "spikes" due to the inactive snubbers of non-conducting transistor(s) elsewhere in the bridge and have used only two current snubbers for all four transistors.

Example:

$t_{rv(max)} = 60\text{ns}$ and $t_{fi(max)} = 140\text{ns}$ at

$I_{C(max)} = 5\text{A}$ ($T_c \simeq 110°\text{C}$) $V_{CE(max)} = 200\text{v}$

$f = 20\text{KHz}$ (series switching, Figure 6)

$$C_{(min)} = \frac{(5\text{A})\,(140\text{ns} + 60\text{ ns})}{200\text{v}}$$

$$= 5\text{nF}$$

Will use 6.6nF

$T_{on(min)} = 5\mu\text{sec}$ $\qquad R_{c(max)} = \frac{5\mu\text{sec}}{3\,(6.6\text{nF})} = 252\Omega$

Will use 220Ω

$$i_{dis(max)} = \frac{200\text{v}}{220\Omega} = 910\text{mA}$$

$$P_{R(max)} \simeq \frac{(6.6\text{nF})\,(200\text{v})^2}{2}(2 \times 10^4\ \text{sec}^{-1})$$

$$= 2.65\text{ watts}$$

Table 2 summarizes actual results using such a device and snubber.

2. **TURN-OFF: The Energy Snubbers** (Applies to Figures 10 and 11).

The nature of the push-pull regulator/converter and the isolated fly back regulator is such that a substantial amount of energy is available at the transformer primary due to leakage inductance which can drive the transistor(s) into avalanche breakdown. There is no "hard" clamp at the collector to return this energy to the supply or pass it on to the load.

Therefore, a snubber must be provided that can sink all of this energy without allowing the transistor to exceed maximum voltage ratings.

One method uses the current snubber of the previous section in conjunction with a zener diode "clamp" across the collector-emitter terminals. The diode will presumably have to absorb most of the energy (given by $\ell I_{C(max)}/2$) and will probably have to be heat sunk. A problem with this method arises as a result of the variability of the clamping voltage of the zener diode. More recent designs using this type of clamp now incorporate silicon transient voltage suppressors (such as the TransZorb™, a General Semiconductor Industries, Inc. product). These rugged devices are specifically characterized for transient environments wherein maximum clamping voltages at maximum pulse currents are tested and guaranteed parameters. The transient suppressor therefore represents the preferred alternative to zener diodes in such applications.

A second method employs the current snubber configuration adapted to absorb all of the energy. Here again a resistor may dissipate a considerable amount of energy and may have to be heat sunk.

TABLE III

CURRENT SNUBBER RESULTS

	Without Snubber	$C = \frac{2}{3} C_{(min)}$	$C = C_{(min)}$	$C = \frac{4}{3} C_{(min)}$
Transistor Turn-Off Power Dissipation:	1.6W	540mW	450mW	350mW
Snubber Dissipation:	—	1.32W	1.6W	2.6W
Total Additional Dissipation:	—	260mW	450mW	1.35W
Peak Collector Power @ Turn-Off:	1KW	143W	110W	83W
V_{CE} @ Peak Collector Power:	200V	156V	50V	20V

I_C = 5A, I_{B2} = 1A, $t_{rv} + t_{fi}$ = 160ns

V_{CC} = 200V, f = 20KHz

Design Parameters:

$t_{rv(max)}$ and $t_{fi(max)}$

@ $I_{C(max)}$

$BV_{ce(max)}$ — A property of the switch

f (frequency of operation)

ℓ transformer leakage reactance

$V_{CE(max)}$:

$$- E_{in(max)} + \frac{N_p}{N_s} E_{out(max)} \quad \text{(Figure 10-b)}$$

$$= 2E_{in(max)} \quad \text{(Figure 11-b)}$$

Compute $C_{(min)}$ as in A-1 above.

Let us assume that the end of t_{rv} (when $V_{CE} = V_{CE(max)}$) the transistor will be completely off and all of the current will be flowing in the current snubber. At this point, energy will be available in the form of $\ell I_{C^2(max)}/2$ at the transformer primary.

This energy will continue to transfer to the snubber until depleted and will show up as an increased voltage, ΔV over and above $V_{CE(max)}$.

If this $\Delta V + V_{CE(max)}$ exceeds the BV_{CE} of the transistor, avalanche breakdown may occur, destroying the switch.

A good margin of safety can be provided by selecting the capacitor such that:

$$V_{CE(max)} + 2\Delta V < BV_{CE} \quad \text{B-1}$$

$$\Delta E = \tfrac{1}{2}\ell I_{c^2(max)} \leq \tfrac{1}{2}C\left[(V_{CE(max)} + \Delta V)^2 - V_{CE(max)^2}\right] \quad \text{B-2}$$

$$C \geq \frac{\ell I^2_{c(max)}}{(\Delta V^2 + 2V_{CE(max)}\Delta V)} \quad \text{B-3}$$

Compare C calculated in this fashion with that computed using A-1 and use the larger of the two. We can now proceed to find Rc (A-3) and $i_{dis(max)}$ (A-5). (Substitute $E_{in(max)}$ in push-pull configuration and $N_pE_{out(max)}/N_s + E_{in(max)}$ in isolated flyback.) A straightforward consideration of worst-case conditions for these two converters indicates a resistor power dissipation of:

$$P_{R(max)} = \left[2\,CE_{in^2} + (2CE_{in})\,(\Delta V) + \frac{C\Delta V^2}{2}\right] f \quad \text{B-4}$$

(Push/Pull)

$$P_{R(max)} = \frac{C}{2}\left(E_{in(max)} + \frac{N_p E_{out(max)}}{N_s} + \Delta V\right)^2 f \quad \text{B-5}$$

(Isolated Flyback)

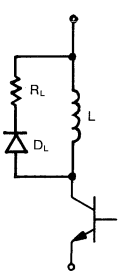
3. TURN-ON: The Voltage Snubber

For most applications, the need for device protection at device turn-on (t_{ri}, t_{fv}, T_{Rec}), from simultaneous high-voltage, high-current transients will not be required, owing mainly to the fact that the high-speed switch is far more capable of sustaining this energy pulse in the forward biased mode than during turn-off. Nevertheless, the presence of such a power pulse may present long-term difficulties and will in any event lead to higher average junction temperatures by way of dissipation in the switch. These higher temperatures will in turn degrade V_{CE} (SAT) and turn-off transition times leading to still higher temperatures and more dissipation. This resembles an insidious form of thermal runaway which may or may not equilibrate prior to device failure. Even in the event that current snubbers are employed, the ramifications of this effect are such that the benefits of turn-off load line shaping will gradually be lost as the junction temperature rises.

The probability that this switching thermal runaway (STR) phenomenon will *not* equilibrate at reasonable safe levels is, in the most cases, quite low. However, *any* excursion upward in temperature because of it will detract from overall efficiency and device reliability.

The current snubber of the previous section strikes a balance between device protection and transferred turn-off power. The voltage (turn-on) snubber (refer to Figure 16) can lead indirectly to improved efficiency by allowing for a lower average junction temperature. Additionally, it may serve as a protective device in those situations where forward biased safe operating area may be jeopardized by an extremely severe turn-on load line. For useful and interesting variations of this concept in both bridge and series regulators, the reader is referred to Calkin and Hamilton [11] and Gottlieb [12] respectively.

FIGURE 16
TURN-ON (VOLTAGE) SNUBBER



The present guidelines will assume the energy exchange format as before where the effects of current rise time, voltage fall time and T_{Rec}, the recovery properties of the system will be taken into account.

Design Parameters:

$t_{ri(max)}$, $t_{fv(max)}$, and T_{Rec} at:

$I_{C(max)}$ and *

$V_{CE(max)}$ *

$T_{OFF(min)}$ minimum switch off time

$BV_{CE(max)}$ — A property of the switch

f (frequency of operation)

*Same as those used in current snubber analysis.

In order to carry this analysis out, we will make an assumption about the recovery parameter, T_{Rec}. In the course of application of what follows, the reader is urged to examine the nature of this parameter for possible modification.

The following method is seen to apply approximately to the series switching regulator (Figure 6) and the flyback regulator (Figure 7) where fast recovery rectifiers are used as commutating elements. These devices can be characterized by a "reverse recovery time," T_{Rec}. This parameter reflect s a tendency for the rectifier to remain close to forward bias during an active turn-off period wherein current will be caused to reverse from the normal direction until a charge, Q_R, can be removed from the device. This charge is primarily due to minority carrier lifetime effects brought about by normal (rectifying) current flow in the device. "Fast" recovery times noted in such devices are brought about by reducing the effective minority carrier lifetime.

In general, for the time periods with which we will deal, we can state that:

$$T_{Rec} \simeq \frac{Q_R}{\langle I_{Rec} \rangle} \qquad \text{C-1}$$

$\langle I_{Rec} \rangle$ is the time-average reverse current withdrawn during T_{Rec}. Q_R is effective recovered charge and will be considered constant for a constant I_F (forward Current) at worst-case thermal conditions. As I_F increases, Q_R will increase. We will, therefore, use $I_{C(max)}$ as the worst-case condition. ($I_{C(max)}$ is the maximum load-related current.)

$$L_{min} = \frac{V_{CE(max)}\,(t_{ri} + t_{fv} + 2T_{Rec})}{I_{C(max)}} + \frac{2V_{ce(max)}\,Q_R}{I_{c(max)^2}} \qquad \text{C-2}$$

This, as before, is based upon energy equivalence:

$$E = \frac{LI_{C(max)}^2}{2} \simeq \frac{I_{C(max)}\,V_{CE(max)}\,(t_{ri} + t_{fv})}{2} +$$

$$V_{ce(max)}\,(I_{C(max)} + \langle I_{Rec} \rangle)\,T_{Rec} \qquad \text{C-3}$$

where I_{Rec} has been replaced by $\frac{Q_R}{T_{Rec}}$

(See Figure 17.)

FIGURE 17
TURN-ON ENERGY

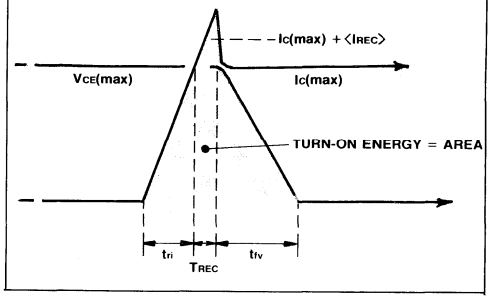


Figure 18 shows the approximate shape of this recovery current overshoot in a flyback regulator where the voltage snubber has been used. Note that the recovery current maximum, I_R, is twice $\langle I_{Rec} \rangle$.

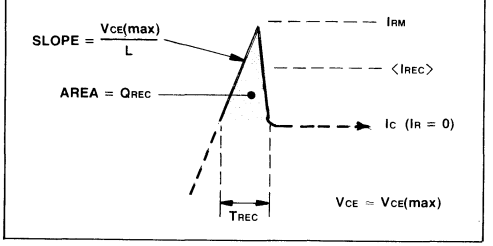
We may then state that:

$$I_{RM} \simeq \frac{2Q_R}{T_{Rec}} \qquad \text{C-4}$$

Suppose that we wish to limit this overshoot to $1/\gamma$ of $I_{C(max)}$. Then:

$$I_{RM} = \frac{I_{C(max)}}{\gamma} \qquad \text{C-5}$$

FIGURE 18
RECTIFIER RECOVERY CURRENT WAVESHAPE USING VOLTAGE SNUBBER (AT TURN-ON)



Substituting this into C-4, and solving for T_{Rec}:

$$T_{REC} = \frac{2\gamma Q_R}{I_{C(max)}} \qquad \text{C-6}$$

Substituting this into C-2:

$$L_{min} = \frac{V_{CE(max)}\,(t_{ri} + t_{fv})}{I_{C(max)}} + \frac{2V_{CE(max)}\,Q_R\,(2\gamma + 1)}{I_{C(max)^2}} \qquad \text{C-7}$$

In this form, we can estimate the value of L, based not only on the transistor switching speeds and rectifier properties but also on the allowable current overshoot due to the rectifier. We can therefore be assured that under normal conditions, the peak currents seen by the transistor and the diode can be controlled.

The next consideration involves selection of R_L. We would like for the current that will circulate through L, D_L and R_L to decay to near 0 at the end of T_{OFF} inasmuch as the transistor will have to assume this current and any reverse recovery effects due to this residual current on D_L upon turning on. Initially, let:

$$R_L = \frac{4L}{T_{OFF(min)}} \qquad \text{C-8}$$

$$\text{from } I_{L(max)} = (I_{RM} + I_{C(max)}) \text{ Exp } (-R_L T_{OFF}/L) \qquad \text{C-9}$$

This will guarantee that I_L will be $< 2\%$ of $I_{C(max)} + I_{RM}$ when the transistor turns back on. We next check that the voltage overshoot on the collector due to the network is within safe limits for worst-case conditions ($I_L = I_{C(max)} + I_{RM}$ at turn-off).

$$V_{CE(max)} + V_L = V_{CE(max)} + (I_{C(max)} + I_{RM}) R_L < BV_{CE(max)} \qquad \text{C-10}$$

If this overshoot approaches $BV_{CE(max)}$ the transistor may incur avalanche breakdown and fail.

If this overshoot is too large, then R will have to be made smaller at the expense of increased residual freewheel current, I_L.

Finally, the maximum power consumed by this network is given by:

$$P_{R(max)} = \frac{L(I_{C(max)} + I_{RM})^2 f}{2} \qquad \text{C-11}$$

Substituting for I_{RM} from C-5:

$$P_{R(max)} = \frac{LI_{C(max)}^2 (1 + \frac{1}{\gamma})^2 f}{2} \qquad \text{C-12}$$

It is interesting to note that in the case where dissipation due to the presence of the rectifier greatly outweighs that due to the transistor turn-on transients, t_{ri} and t_{fv}, an optimum value of γ exists that will minimize dissipated power at turn-on. This condition can be met for vigorous initial turn-on drive, I_B, such as that which is obtained by bypass or "speedup" techniques. Substituting C-7 into C-12 for L and neglecting the term involving t_{ri} and t_{fv} we obtain:

$$P_{R(max)} = V_{CE(max)} Q_R f (1 + \frac{1}{\gamma})^2 (2\gamma + 1)$$

$$= V_{CE(max)} Q_R f (2\gamma + 5 + \frac{4}{\gamma} + \frac{1}{\gamma^2}) \qquad \text{C-13}$$

By setting $dP_{R(max)}/d\gamma$ equal to 0 and solving the resulting cubic equation, we obtain one positive minimum at $\gamma = 1.62$. As γ approaches 0, dissipation rises because of increased peak current through the inductor. As γ increases from the minimum, dissipation rises due to increasing values of inductance. A few computations will show that for values of γ between about 1 and 2.5, the power dissipation will not rise significantly above the minimum, and these numbers should represent design limits. Figure 19 shows how both the current and voltage snubbers might be used concurrently.

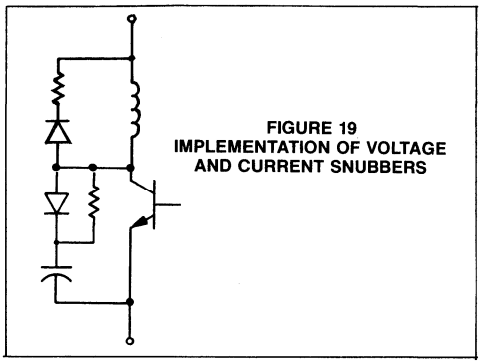


FIGURE 19
IMPLEMENTATION OF VOLTAGE AND CURRENT SNUBBERS

In designing an appropriate inductor for the voltage snubber, and keeping in mind that this inductor is in most instances going to be only a few microhenries, air core inductors should be considered for their low cost and non-saturating characteristics. The obvious disadvantage here may be the magnetic field generated by such a choke, but owing to the low values of inductance, this may be an innocuous side effect for many applications. However, care should be exercised in placing this inductor so that flux lines do not adversely affect the base drive leads and associated circuitry. As a convenience, a design sheet for such inductors has been included where values of κ have been excerpted from Corson and Lorrain [13] (Figure 20). One feature of this approach to voltage snubbing should be mentioned lest it go unnoticed. At the instant that V_{CE} falls toward saturation, there will be a voltage reversal across the snubber inductor given by:

$$V_L = I_{RM} R_L \qquad \text{C-14}$$

due to the fact that the additional energy acquired by the inductor while clearing charge from the rectifier must immediately commence to dissipate in R_L. After this has occurred, I_L will have decayed to I_C and V_L will be 0. The effect is to observe a minor voltage peak at the beginning of T_{ON}.

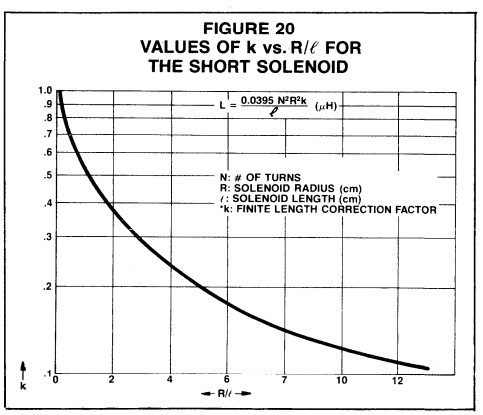


FIGURE 20
VALUES OF k vs. R/ℓ FOR THE SHORT SOLENOID

THE R-C SNUBBER

A discussion of simple load-line shaping techniques would not be complete without mentioning the R-C Snubber.

Briefly, the R-C Snubber in most cases is used across the primary of converter type regulators and consists simply of a series-connected resistor and capacitor which will act as a current-type snubber at turn-off.

This type of snubber does not have the inherent capability to sink the total current throughout the turn-off load line as does the previously mentioned current snubber. However, it does not suffer from the uncontrolled turn-on current spike which can be a problem with the "current snubber" in converter applications. It may then offer an acceptable alternative in some applications. The selection of values for R and C would proceed in much the same way as with the current snubber. In the limit as $t_f \ll T_{ON(min)}$, the turn-off load line can be made to look almost resistive. A starting point for selecting R would be $V_{primary(max)}/I_{C(max)}$. C could be selected then using the $T_{ON(min)}$ criteria of the current snubber section. The current overshoot at turn-on would then be approximately equal to $I_{C(max)}$ under most conditions except for high duty where this overshoot would be seen to decrease. This approach might be used in the bridge-type converters and an "energy sink" approach might be used in the push/pull converter.

SUMMARY:

The problems associated with using power switching transistors are well-known to the experienced power supply designer. This paper was not necessarily prepared to offer hard and fast rules and regulations for fail-safe application. The material and presentation was directed at a multi-faceted area in broad, general terms, and the two basic snubbing configurations examined were chosen for their inherent simplicity. The *resulting benefits* of this class of protective devices are to be considered far more important than the techniques used to achieve them. There are more elegant techniques available to those who are willing to trade simplicity for greater efficiency and protection.

One area that should be emphasized at this point regards base drive. The severity which was noted as common in turn-off drive configurations will enhance t_{rv} and t_{fi}. Given that a current snubber is used, increasing I_{B2} will actually serve to decrease the turn-off power dissipated in the transistor while concurrently reducing V_{CE} at which peak collector power occurs. So by making I_{B2} larger, we can use smaller snubber capacitors and improve upon power losses. This is a favorable approach, but one which would meet with disaster in the absence of a snubber. The same rationale can be applied to turn-on, where very large initial values of I_{B1} will serve to reduce switching losses and bring the transistor much closer to $V_{CE(SAT)}$. A reduction in I_{B1} after turn-on will maintain $V_{CE(SAT)}$ and allow for a reduction in storage time and therefore will improve turn-off efficiency in the base drive circuit.

Component selection for the passive elements of the two snubber configurations involve a consideration of transient performance in addition to the normal voltage, current, and power constraints. For most applications, D_C can be a simple rectifier since recovery time is not terribly important. D_L, on the other hand, may require some attention in this area, depending upon the magnitude of the maximum residual current freewheeling through it when the transistor is turning on. If the design constraints outlined above can be met, then there will probably be no reason to select a fast recovery rectifier for this job. R_C need not be a low inductance resistor since the RcC time constant is not very critical. R_L is involved in the over-voltage turn-off transient and self-inductance should be kept at an absolute minimum. Carbon is a good choice. C is potentially a troublesome component in that it must pass large currents when the transistor turns off. The choice here should clearly be a very low-loss, quality capacitor, such as polycarbonate or polypropylene.

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REDUCING CONDUCTED EMI WITH THE ULTRA-LOW CAPACITANCE ISOLATED TO-3 SWITCHING TRANSISTOR

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Abstract

A brief review of the various sources of EMI in the switching power supply is presented. Capacitive coupling of the transistor collector (case) to ground is shown to be a major cause of conducted EMI.

Conventional solutions (e.g., "screened heatsinks") are examinded and shown to be much less than optimal. The isolated TO-3 is presented as an effective solution to this problem. Electrical, thermal, and mechanical properties are compared to "standard" configurations. Data showing the comparative reduction in conducted EMI (obtained by an independent testing facility) is provided.

Introduction

Some years ago, at POWERCON 3, several individuals expressed an interest in procuring a power transistor for widespread commercial application wherein the active terminals were completerly isolated from the case. The benefits associated with such configurations were, even then, well established. However, the only available devices were of the stud-mounted variety commonly used by the military. Owing to the large packaging investment, these devices are, of necessity, two to three times more expensive than their electrical counterparts packaged in the industry standard TO-3. This cost deficiency has been, to this point, the major obstacle in the path of extensive utilization of isolated package power devices.

Following POWERCON 3, an industry-wide survey was conducted by mail to determine the level of interest in a cost-effective version of the isolated power transistor resembling a TO-3. Response to the survey was extremely favorable. An unprecedented 33% reply rate, in which 88% of those responding, favored such an endeavor clearly demonstrated industry awareness of those problems addressed by an isolated TO-3.

What follows is a brief examination of what many consider to be the primary advantage of an isolated structure, the reduction of conducted EMI. Concurrently, however, certain thermal and mechanical properties will surface as an outgrowth of this approach, and these characteristics will be examined as they further enhance the desirability of such a device.

Electromagnetic Interference (EMI)

Electromagnetic interference can be described as any undesired electromagnetic energy which may find its way into or out of electronic equipment. A fundamental requisite for the generation of EMI is that the time rate-of-change of current in the generator" be other than zero:[1]

$$di/dt \neq 0 \qquad (1)$$

If this condition is met, then the generation of EMI is inescapable. In actual point of fact, the probability that this condition will *not* be met somewhere, even in the most stable of direct current systems, is vanishingly small. On an atomic scale, certainly, the discrete nature of current flow would suggest that electromagnetic interference is generated by what we might regard as steady state flux.

However, EMI production, to be meaningful will be considered only as it might have a deleterious effect upon perfromance of an electronic system. Certain levels have been established by many organizations as limits beyond which susceptability to interference may present functional problems for another link in the equipment chain. These specifications generally pertain to the two different methods by which interfering signals may be propagated, conduction and radiation.

Although the means of transmission may be self-explanatory, the internal mechanisms by which such signals are generated and sustained are sometimes subtle. More engineering time is being expended in EMI management in the design stages than ever before, and many of the subtleties are being put to rest.

EMI vs Power Conversion

There are few areas more demanding of the design engineer from an interference standpoint than that of solid state power conversion.

The central principle embodying the present state of the art of power supply design is the switching concept. Two fundamental requirements have necessitated this approach: (1) efficiency, and (2) compactness. Efficiency is achieved in the switching process as the switching elements approach the ideal. That is, infinite off-state impedance (both steady state and transitional), zero on-state impe-

dance, and zero transition times. Compactness is achieved as a result of rising efficiency which allows for smaller dissipative surfaces. Compactness is also brought about by an increase in the switching rate allowing for proportionally smaller energy storage and transformation elements, capacitors, inductors, and transformers.

Unfortunately, the switching approach, while leading to the aforementioned goals, will introduce the necessary conditions for the generation of EMI on a large scale (Figure 1). Radiated interference, which will generally occur because of rapidly varying current within the supply can, in most cases, be adequately controlled by employing shielding technology[2]. However, if the input and output are improperly terminated or the ground connection on the shielded enclosure has any appreciable impedance associated with it, radiated emissions may increase.

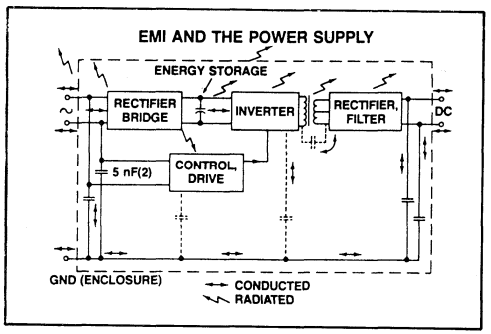


FIGURE 1

Conducted emissions will be apparent at the input and output terminals as well as the "ground" terminal (third wire conduction). Filter techniques are commonly employed to reduce emissions at the input and output terminals. However, as the energy content of high frequency interference rises (high speed, high frequency switching), conventional filtration may fall short of the desired results.

Many times, conventional high frequency bypass techniques will incorporate the ground plane as a conduction path. Such an approach may well reduce emissions on the input/output lines at the expense of increasing conducted emissions injected into the ground. This can lead to common mode interference where common "ground" conditions are less than ideal.[3][4]

In addition to the reconizable sources of interference by conduction, there exists within any such system a multitude of mutual nonconductive impedances, either capacitive or inductive in nature which will transmit and receive energy from the input/output lines and ground plane.[5] (A few such capacitive paths are shown in Figure 1—dashed lines.) These coupled interference paths can contribute a significant component of high frequency interference.

Primary Conducted Interference—Principal Causes

Figure 2 is a simplified schematic representation of the primary-side switching elements (the input rectifiers and power switching transistors) of a half-bridge configuration.

The frequency domain analysis which follows will make use of the interference envelope approximation method.[6] This method will yield worst case levels to within ~ 3dB.

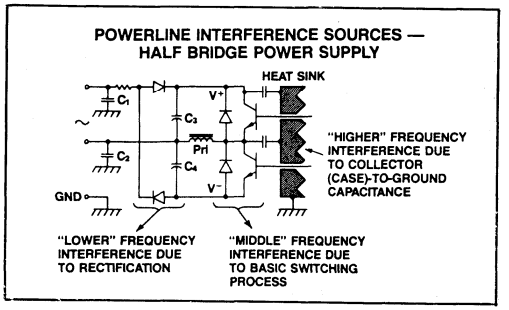


FIGURE 2

Mains Rectification

The interference envelope generated by the mains rectifiers of Figure 2 will, in general, depend upon the duration of the conduction cycle of each rectifier. If we require that the power delivered to the system remains constant, then the conduction cycle duration will depend upon the magnitude of C_3 and C_4. The amplitude of rectified current, together with conduction cycle duration, will determine the interference level at frequencies less than $1/\pi d$, where d is conduction cycle duration (Fig. 3). Beyond $1/\pi d$, the interference contribution of the mains rectifier will drop at a rate of approximately 40dB/decade. The rectifiers themselves will contribute a higher frequency component due to nonlinearities caused by forward and reverse recovery transients. In most cases, however, the level of interference produced by these transients will be considerably beneath those levels produced by the high frequency switching elements.[7] Reducing capacitor size will have the effect of lengthening d, the conduction period, and reducing the amplitude such that the interference level at low frequencies will remain approximately the same. The frequency at which roll-off commences will shift down, implying lower high frequency interference levels. C^3 and C_4 must remain large enough to gurarantee proper circuit operation under all conditions.

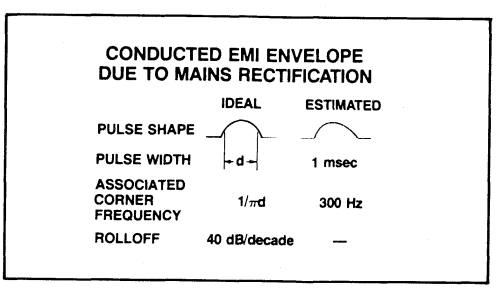


FIGURE 3

Transistor Switching Action

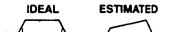
This particular source of EMI provides a substantial portion of conducted interference directly, and as the active switching element of the system, could be held indirectly accountable for most of the interference generating responses associated with the transformer and secondary network. (Fig. 4)

As before, the low frequency interference level is proportional to pulse amplitude (I_C) times the conduction period $T_{(ON)}$. This level remains unchanged out to $1/\pi T_{(ON)}$, at which point, the level will drop at a rate of 20dB/decade.

The relatively large input capacitors, C_3 and C_4, will provide some attenuation of this high level signal at the low frequencies, but will gradually loose effectiveness at hgher frequencies due to ESL.

The current rise and fall times of the switching transistor will establish the second "corner" frequency of the interference envelope. The present state of the art implies a practical expectation of current transition on the order of 100nS. This speed places the second corner at about 3MHz beyond which the envelope will roll off at about 40dB/decade. This frequency may be well beyond the self-resonant frequencies of C_3 and C_4 as mentioned above and most of the burden of attenuation may fall in C_1 and C_2. These capacitors, generally on the order of a few thousand pF, are by themselves fully capable of providing the necessary attenuation. However, their physical location within the power supply may allow for enough series inductance (due to lead-length) to provide a significant resonance point within the switching envelope. In fact, the ESL of C_3 and C_4 may provide this inductance in parallel fashion.

CONDUCTED EMI ENVELOPE DUE TO TRANSISTOR SWITCHING ACTION

	IDEAL	ESTIMATED
PULSE SHAPE		
PULSE WIDTH	T_{ON}	15 μsec
ASSOCIATED CORNER FREQUENCY (1ST)	$1/\pi T_{ON}$	20 kHz
ROLLOFF	20 dB/decade	—
RISE TIME	t_i*	100 nsec
ASSOCIATED CORNER FREQUENCY (2ND)	$1/\pi t_i$	3 MHz
ROLLOFF	40 dB/decade	—

*t_i = CURRENT RISE, FALL TIMES

FIGURE 4

The treatment of this major source of EMI could proceed in two directions, depending upon the desired result. One method which might be employed to reduce interference below $f = 1/\pi T_{ON}$ would be to elevate the basic operating frequency. Since I_C would remain the same and the conduction period would decrease as the inverse of operating frequency, then the low frequency portion of the interference envelope (below $1/\pi T^*$, where T^* would be reduced conduction period) could be reduced. It is worthwhile to note that this solution is consistent with the requirement for physical size reduction mentioned earlier.

The second area which might be considered for alteration is associated with a reduction in the second "corner" frequency, that associated with current transition times, t_{ri} and t_{fi}. In order to reduce this frequency, we might adjust the drive levels to the transistor to lengthen rise and fall times. Although this would achieve the desired result with regard to EMI, power consumption would rise in the switching transistor, thus violating our requirement for efficient operation. Artificially slowing current rise time by inserting some small valued inductor in series with the transformer primary would efficiently reduce current rise time, but would introduce additional high frequency interference during current fall time. Certain techniques related to nondissipative load-line shaping may at least partially solve this problem. Usually, however, when such circuit methods are applied during current rise, the voltage transsition time will improve. This may sound favorable, but any reduction of voltage transition times will further enhance high frequency EMI by virtue of capacitive coupling.

Capacitive Coupling

The third major source of conducted EMI on the primary side is a capcitively coupled generator which incorporates the ground plane as a conduction link. In so doing, it plays a major role in common mode (third wire) conducted interference as well as adding to high frequency powerline interference.

This capacitive coupling is a result of the proximity of a grounded heatsink to the transistor collector (here assumed to be a TO-3 package). Interposed between the transistor and its heatsink is a thin (.002) mica ($\varepsilon_r = 7.5$) dielectric insulator. This structure yields a calculated collector to ground capacitance in excess of 800pF for perfectly flat sufaces and no thermal compound. Typical measured values for this capacitance fall in the range from 200 to 250pF. The large difference between measured and calculated capacitance arises mainly as a result of imperfect surface-flatness and the presence of thermal compound.

This configuration is capable of generating significant parcels of EMI which will only begin to roll off at frequencies approaching 3MHz (Figure 5). This "first corner" frequency is in excess of two orders of magnitude greater than that associated with the basic switching frequency. This basic relationship in this first corner of the interference envelope bears the same relationship as does T_{ON} to t_v, the voltage transition time.

The current generated by capacitive coupling to ground would resemble a trapezoidal pulse in the absence of significant inductance. Generally speaking, there will be enough inductance in the collector return to alter the shape of this current pulse. However, the effective pulse duration will not change significantly, with the result that the first "corner" frequency on the coupling envelope will be essentially unchanged.

It is worth mentioning at this point that the only devices which will generate such a large amplitude pulse are those in which the collector voltage is undergoing large amplitude rapid transitions with respect to ground. Referring back to Figure 2, we find that the lower transistor in the half bridge satisfies this condition while the upper transitor is operating at a fixed voltage with respect to ground, or at worst oscillating at power-line frequency where coupling capacitance would contribute virtually

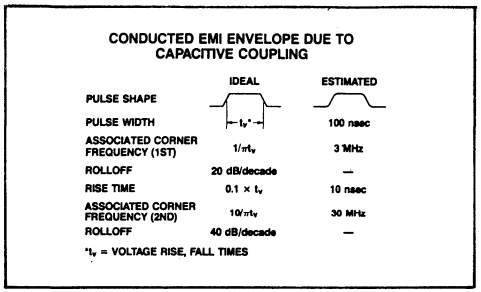


FIGURE 5

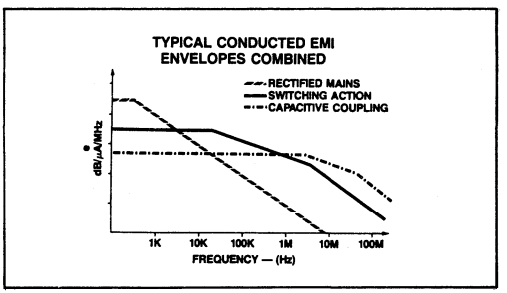


FIGURE 6

nothing in the way of current.

Above, we discussed the reduction of magnitude due to the transistor conduction period by increasing the basic switching frequency (decreasing the conduction time, T_{ON}). This would allow for a reduction in $I_C T_{ON}$ which, as we pointed out earlier, is proportional to the magnitude of the interference envelope below $1/\pi T_{ON}$. Let us examine the possibility of a magnitude reduction for the coupled current pulse.

We know that: $M \propto I_p t_v$ (2)

where M is the magnitude of interference below $1/\pi t_v$, I_p is the amplitude of the current pulse due to capacitive coupling, and t_v is the collector voltage transition time. (For simplicity, it is assumed here that $t_{fv} = t_{rv} = t_v$) I_p and t_v are fundamentally related as:

$$I_p = C_{cg}\, dv/dt \quad (3)$$

$$\approx C_{cg}\, \Delta V_{CE}/t_v \quad (4)$$

$$\therefore I_p t_v \approx C_{cg}\, \Delta V_{CE} \quad (5)$$

(C_{cg} is the collector-ground capacitance and ΔV_{CE} is the collector-emitter voltage transition.)

Since C_{cg} and ΔV_{CE} are fixed, then $I_p t_v$ is a constant. This being the case, we cannot reduce the envelope maximum (at $f < 1/\pi t_v$). We could alter the first corner frequency by increasing t_v. One way to accomplish this would be to underdrive the transistor at turn-on and oversnub at turn-off, both of which violate our efficiency requirement. Again, non-dissipative load line shaping might be used to some advantage, but the primary goal of load line shaping should be transistor protection and efficiency optimization. Failure to take full advantage of the high speed capability to today's switching transistors might be considered counter-productive with regard to the achievement of high efficiency and small size.

Before examining *viable* solutions for this source of high frequency interference, it might be beneficial to briefly review, by way of example, the *combined* effects of the material thus far presented.

The EMI Contour, An Overview

Shown in Figure 6 is a representative example of an interference profile composed of the three envelopes considered.

Since the vertical axis is logarithmic, the additive effects of the envelopes will follow the local maximum with some smoothing at the intersecting points[2]. The relative maxima (horizontal lines) representative of the amplitude-pulse width product will not necessarily be related as shown, although the envelope due to mains rectification (top) will generally lie above that due to basic switching action (middle). Both of these will invariably lie above the envelope maximum due to collector-ground capacitive coupling.

The attenuation due to filtering (C_1 through C_4, Figure 2) has not been taken into account at this point so that we might avoid clouding the issue at hand.

The first (and second) "corner" frequencies of each envelope approximate the numbers cited in Figures 3, 4, and 5.

Suppose that, as a consequence of space limitations, the overall size of the power supply must be reduced. It might be deeemed necessary to increase the basic switching rate by a factor of three to reduce transformer, capacitor, and inductor sizes. Simultaneously, in order to partially offset the increased switching losses, it becomes necessary to select a transistor with improved transition times.

The preceding changes would not meaningfully alter the interference envelope associated with mains rectification, unless, of course, C_3 and C_4 had been reduced in size to help solve the volume problem. If that had been done, then the first (and only) corner frequency of the mains envelope would occur at a lower frequency, while the magnitude (horizontal line) would stay more or less the same. So, the entire rolloff characteristic would shift slightly to the left, representing a slight improvement.

Operating the power supply at higher switching rate would necessarily lower the envelope magnitude due to switching action below the first corner frequency as explained earlier.

Current rise time and fall time improvements would allow for a further extension of the 20dB/decade rolloff beyond the newly established first corner frequency (switching action).

Voltage rise and fall time improvements would *not* reduce envelope magnitude due to capacitive coupling. In fact, the first corner frequency would shift to the right, allowing for further increases in high frequency interference.

High Frequency Interference Reduction

1—Heatsink Isolation

One method commonly employed to subdue the collector to ground capacity problem is heatsink isolation. Besides circumventing the capacitive effects, this method allows for direct attachment of the transistor without using an insulating washer. This can improve the junction to heatsink thermal resistance, Θ_{JS} by at least 0.2° C/W. However, the isolated heatsink is not without problems. The chassis can no longer be used as an integral heatsink, thereby increasing both cost and size. The isolated heatsink must be enclosed within the system because of shock hazards and radiated emissions. Furthermore standoff insulators must be used to achieve the desired result, with the consequence that heat transfer from the heatsink must be entirely convective. Both of these requirements may dictate a need for forced air unless the degraded switching times and reliablity resulting from high temperature operation can be tolerated. From an electrical standpoint, a separate heatsink must be used for each transistor not common at the collector. If we were to mount both transistors of the half bridge on the same heatsink using insulating washers and isolate the heatsink from ground, then a capacitve link would exist which would couple one transistor to the other creating an interference path involving the mains.

The overall picture of EMI reduction by heatsink isolation is much less than optimal, considering the tradeoffs required. Several years ago, a method was formally introduced which purported to reduce capacitively coupled EMI in a much more straightforward way.

2—Shielding The TO-3 (Fig. 7)

The utilization of Faraday shields as interwinding capacitance reduction elements in trasformers is a well known and often practiced technique.[8] The application of this concept to the screening of power transistors[9] represented a significant contribution in the area of EMI control. Since the transistor had to be isolated from the heat sink anyway, why would it not be possible to add another insulating washer and interpose a solid metal "screen" which could be connected to the emitter. This would allow the capacitively coupled current which would normally be driven into and out of the heat sink to be confined to the transistor only. In effect, the shield would remain at emitter potential which has, at most, a very low frequency sinusoidal relationship to ground. In theory, this "screened heat sink" methodology would virtually eliminate the interference produced directly by the standard TO-3 mounting configuration.

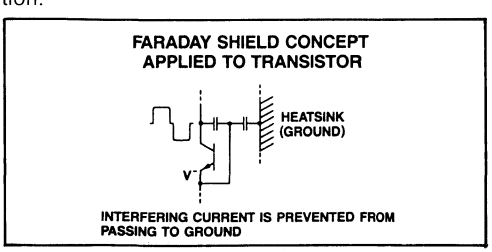


FIGURE 7

Although the large scale problems associated with the isolated heatsinks are resolved by implementation of the Faraday shield, there exists the possibility that the shield can fall far short of expectations when used in conjunction with the high speed switching transistor.

Of primary interest at this point is the critical roll of shield implementation with respect to high frequency interference control. However, it is more than just noteworthy that regardless of shield performance, transistor action will be somewhat impaired, both thermally and electrically by its use.

Shown in Figure 8A is the electrical equivalent of the Faraday shield thus applied. C represents the capacitance due to the TO-3 insulating washers, one between the transistor and shield, and one between the shield and grounded heatsink. E_{OUT} is the shield voltage, and the lumped inductance is descriptive of that due to lead length between the shield and the emitter pin. Distributed capacitance referenced to ground will certainly exist along the wire (which is usually brought through the heatsink to the emitter pin via the shortest practical route) but this distributed capacity will be a small percentage of that due to the insulating washers. E_{IN} is the collector voltage referenced to ground over one complete switching cycle. (Note that this condition is *only* satisfied by the lower transistor of Figure 2.)

Earlier it was stated that the emitter voltage of the transistor under consideration was approximately constant with respect to ground during the short times with which we were concerned ($<<50\mu$sec). There will exist on this line an interference voltage spectrum which will be $<<\Delta E_{IN}(\Delta V_{CE})$.

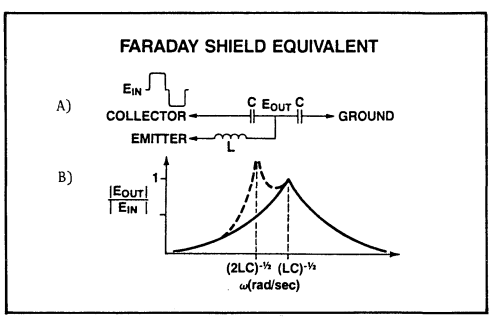


FIGURE 8

The impedance interposed between the emitter and ground will depend upon circuit layout as well as intentional discrete components (usually "bypass" capacitors) and the effective mains-to-ground impedance.

$$\text{If } L \equiv 0, \text{ then } |E_{OUT}| \,/\, |E_{IN}| \equiv 0 \qquad (6)$$

$|E_{OUT}|$ and $|E_{IN}|$ are referenced to the emitter for convenience. Equation 6 satisfies the requirement for no interference and does not depend upon the external impedance mentioned above.

For the sake of further analysis, suppose that we insert a relatively large totally noninductive capacitor

from emitter to ground, thus establishing a low impedance at high frequencies. 5nF is an appropriate choice since this is about the largest capacitor of this nature permitted by certain international regulations.[10] If we allow L, the shield-to-emitter inductance to assume a nonzero value (perhaps 20-30nH) we will reestablish the necessary conditions for interference: (see Figure 8B)

$$\text{If } L \neq 0,\ \omega \neq 0, \text{ then } |E_{OUT}| / |E_{IN}| \neq 0 \qquad (7)$$

Displayed in Figure 8B is a graphic representation in the frequency domain of the relationship between $|E_{IN}|$ and $|E_{OUT}|$. Note that as frequency rises, so does the magnitude of the desturbance produced at E_{OUT}. The dashed lines are indicative of the nature of the drive, and cannot be easily identified for our particular example. Suffice to say that the disturbance $|E_{OUT}| / |E_{IN}|$ will rise to 1 at a frequency of $1/(2\pi(LC)^{1/2})$. This is precisely the same condition that would exist for a TO-3 mounted in standard fashion! At this frequency, there would be no benefit associated with the shielded configuration.

From this simple example and a straight-forward consideration of the maximum energy available to shield network at any frequency, we can establish a maximum value for $|E_{OUT}| / |E_{IN}|$ of 1. Furthermore, an "effective" capacitance can be established:

$$C_E(\omega) = C\ |E_O| / |E_I| \qquad (8)$$

Two important results become apparent (1) the effective capacitance of the Faraday shield will never be worse than that of its nonshielded counterpart, and (2) the effective capacitance of its constituents. The *relative* interference due to this effective capacitance will vary as:

$$e_r = 20 \log C_E(\omega)/C \qquad (9)$$

$$= 20 \log |E_O| / |E_I| \qquad (10)$$

In order to acquire a feeling for the frequencies involved, it is only necessary to subsitiute for L and C at the well defined peak where:

$$|E_{OUT}| / |E_{IN}| = 1 \quad (C_E = C)$$

Measured values of C are typically 240pf, and the inductance measured for an easily constructed shield runs as low as 30nH (equivalent to about 3cm of #18 wire[11]).

$$\frac{(LC)^{-1/2}}{2\pi} = \frac{((3 \times 10^{-8})(2.4 \times 10^{-10}))^{-1/2}}{2\pi}$$

$$= 59\text{MHz}$$

Preceding Eq. 7, a "totally noninductive" 5nF shunt capacitor was attached to the emitter and taken to ground. If this capacitor is allowed to become nominally inductive, then a situatuion will exist where the effective capacitance curve (given by Figure 8B as $C\ |E_{OUT}| / |E_{IN}|$)will shift to the left.

Therefore, the Faraday shield can be totally ineffective as an EMI control element at high frequencies where it would do the most good (Figure 6).

If inductance could be reduced, then the shield might regain much of its intended usefulness. To accomplish any meaningful reduction of this inductance, the hole through which the emitter pin must pass could be reduced in size to approximately .040", and soldered directly to the pin. This would further complicate a configuration that already requires no less than 12 pieces of mounting hardware including two insulating washers (preferably mica), one copper shield (for solderability), one collector solder lug, two insulating and centering bushings, and two sets of fasteners. In addition, if a conventional through-the-heatsink connection is made to the emitter, an insulating jacket will be required. (Figure 13)

3—The TO-3/Isolated (Fig. 9)

We have examined two methods for the reduction of collector-to-ground capacitive in influences. It has been shown that neither will achieve the desired end in any straightforward manner. The straightforward solution is one which will achieve EMI control over a wide range of frequencies by reducing collector-to-heatsink capacitance. The obvious location for establishing this reduction is directly beneath the transistor chip within the package. It is here that the thermal path between the transistor chip and the heatsink upon which the package is mounted is of minimum area.

$$C = \varepsilon_o \varepsilon_r A/t \qquad (11)$$

Given a constant capacitance, minimizing area (A) will allow for a minimum thickness (t) and therefore a minimum dielectric volume (At). This can be a significant point where volume is related to material cost and where product weight is of importance. In order to achieve an effective design, several goals must be established:

1—Thermal conductivity of the dielectric must be very high since all of the heat generated by the transistor will pass through the isolating element.

2—The dielectric must be capable of supporting a metalization system that will allow for minimum interface thermal resistance and gold-silicon eutectic bonding of the chip to the metalized surface and subsequent soldering of this assembly into the package.

3—The dielectric must possess expansion properties compatible with those of silicon and must be capable of absorbing stresses imposed upon it by the thermal gradients with a minimum of mechanical deflection.

4—To be fully effective as an isolating element, the dielectric must exhibit a very high resistivity and dielectric strength. Surface conduction will impose restrictions on thickness of the element.

Difficult as it may be to believe, such a material exists and has been used for many years in the production of military grade power transistors. Commercial grade beryllium oxide (beryllia) possesses higher thermal conductivity than aluminum, resistivity approaching that of teflon, and the ability to form extremely strong bonds with metals.[12]

In order to guarantee more than adequate mechanical properties for the structure under consideration, a relatively thick substrate has been used. This will have a favorable impact upon capacitance, but will detract somewhat from thermal capability.

Normally, a molybdenum expansion buffer is used in the TO-3. This buffer is approximately .01" thick. The thermal conductivity of molybdenum is 3.4 watts/°C-in. Neglecting interface thermal resistance of the gold plated surface, a simple calculation of thermal resistance of the molybdenum buffer for the device under consideration yields a value of .058 °C/watt.

Using a metalized beryllia tab .03" thick, and noting that the thermal conductivity of Beryllia is 6.58 watts/°C-in, a similar calculation yields a thermal resistance of .128°C/watt. It is interesting to note that this tabulation takes into account the interface resistance of the beryllia—metalization bond. (≃40% of total thermal resistance) This is the only difference between the standard TO-3 and the subject TO-3/Isolated. Simple arithmetic shows an increase in junction-to-case thermal resistance (Θ_{jc}) of only .07°C/watt, the total penalty for using a beryllia substrate three times thicker than its molybdenum counterpart. This increased thickness will provide a sound mechanical structure capable of enduring the rigors of thermal shock and cycling.

A definite thermal advantage now becomes apparent. The isolated structure will allow for the elimination of a mica washer at the package-heatsink interface. This will *reduce* thermal resistance from case-to-sink (Θ_{cs}) by at least .2°C/watt.[13] The overall thermal resistance from junction to heatsink will improve significantly. The elimination of the mica insulator suggests some further benefits which relate to mounting the isolated TO-3. Inasmuch as the collector to case breakdown voltage will be a factory tested parameter, the user will be spared the necessity of conducting "hi-pot" tests to detect the presence of imperfections in the mica or conductive paths (e.g. metal splinters) existing at the mounting interface.

Since the transistor case will no longer be connected to the collector, it will never again represent a shock hazard, and for this reason may now be left exposed at will, obviating the need for plastic covers, non-conductive coatings and the like.

With regard to the isolating technique, the effects of altitude and humidity will not again be a consideration, as the atmosphere in the hermetic TO-3/Isolated is dry nitrogen sealed at NTP. Ultimately the pin-to-case behavior will be the only consideration.

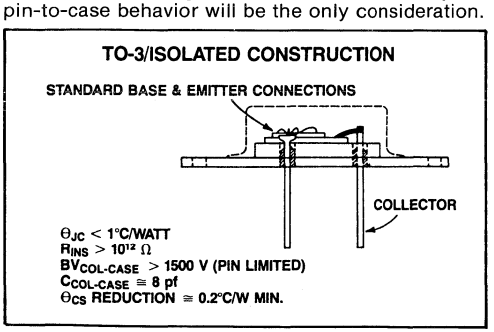


FIGURE 9

Electrical Performance—

The internally isolated TO-3 displays a typical insulation resistance well in excess of 10^{12} ohms, and owing to the high thickness-to-area ratio of the beryllia insulator, will maintain a collector to case capacitance of less than 10pf.

In order to achieve this level of capacitive isolation in a standard TO-3, and maintain good thermal contact, it would be necessary to interpose a BeO washer ⅜" thick!

The usefulness of such a drastic reduction in capacitance becomes immediately apparent if we reconsider, for a moment, the results of equation 8. The analysis of the Faraday Shield indicates that a practical implementation would produce an effective capacitance approaching that of its constituents at high frequencies. Since the level of interface is directly porportional to the value of capacitance, (Eq. 5) it was concluded that the shield might be no better than a standard TO-3 configuration at the high frequencies of interest. By reducing the capacitance of the standard configuration, a uniform reduction of capacitively coupled EMI would be possible without becoming embroiled in the details of shield implementation.

This is precisely the impact achieved by the low capacitance structure.

Application Of The TO-3/Isolated

-Test Results-

In tests conducted at the EMI Evaluation Laboratory of Cincinnati Electronics, Inc. Cincinnati, Ohio, an off-line switching power supply was evaluated as follows:

1) Tests were conducted in accordance with MIL-STD-461A, CE03, conducted emissions—power leads.

2) High frequency filtering devices were removed from the power leads to allow for minimum attenuation of high frequency interference.

3) Two nearly identical sets of high speed triple diffused power transitors were used: Set #1 was a pair of GSTR8045s (Std. TO-3). Set #2 consisted of electrically identical die mounted in the TO-3/Isolated.

4) Set #1 was evaluated in both shielded and unshielded configurations. The results are presented in Figure 10. A three point rolling average has been used to offer a more continuous representation of overall effect.

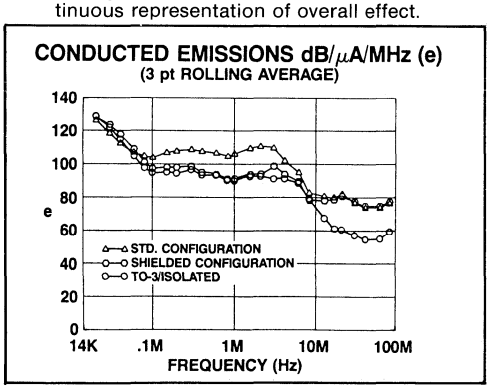


FIGURE 10

Up to approximately 60KHz, low frequency interference souces predominate. Middle frequency (up to about 8MHz) performance is essentially identical for both TO-3/Shielded and TO-3/Isolated configurations. Between 60KHz and 6MHz, an average 15dB improvement can be observed for both structures as expected. It seems likely that any further impovement was probably over-shadowed by basic switching interference, since the shielded configuration should have fared well through this range.

Beyond 8MHz, the shielded configuration performed poorly suggesting the mechanism of Eq. 8. The TO-3/Isolated configuration continued to perform extremely well through this range achieving nominally an 18-22dB reduction throughout. (Theoretical maximum for this structure is 30dB)

Shown in Figure 11 is a graphic representation of the effects of ground wire of third wire conducted interference. This test was performed at General Semiconductor Indusries, Inc. using a high speed current probe on the same supply with *all* filter devices in place. The top trace is third wire generation using the standard TO-3 configuration. The leading edge has a high frequency component which establishes resonance at about 350KHz, with an amplitude of approximately 180mA. The TO-3/Isolated, on the other hand, (second trace) shows considerable improvement in this area thereby reducing the likelyhood for common mode problems. The bottom curve is representative of the current waveform of the transistor at turn-off.

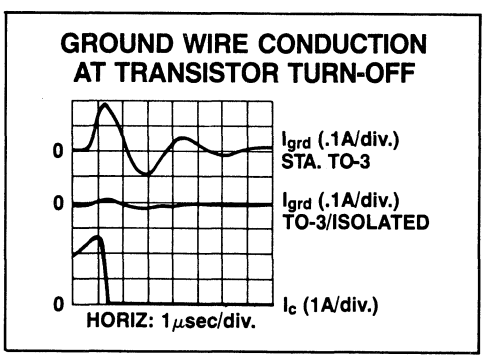


FIGURE 11

Figures 12, 13, and 14, have been included to show the hardware requirements of the various configurations. The simplified assembly and testing of the TO-3/Isolated may well warrant consideration even in those situations where the benefits associated with EMI control are of secondary concern.

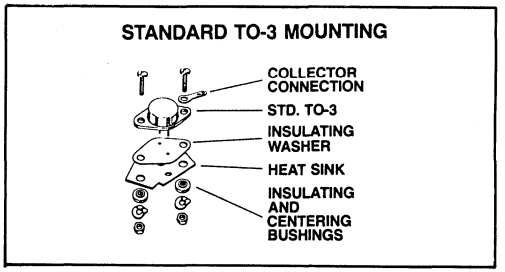


FIGURE 12

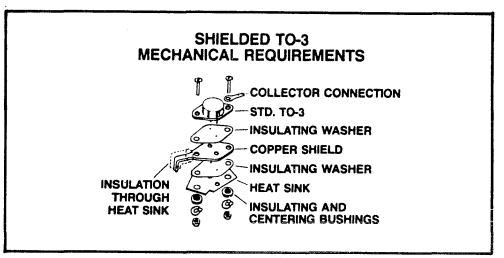


FIGURE 13

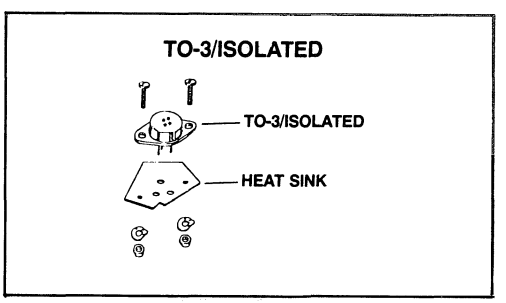


FIGURE 14

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Acknowledgements

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Originally presented as *"Reducing Conducted EMI With a New Ultra-Low Capacitance Switching Transistor Configuration,"* Powercon 5, May 1978.

Understanding And Using Third-Generation Bipolar Switching Transistors*

Speed, Efficiency and Ruggedness Together at Last. . .

by
W. R. Skanadore
General Semiconductor Industries, Inc., Tempe, Arizona

ABSTRACT

A new generation of high voltage bipolar switching transistors is introduced. It is demonstrated that 50nS turn-off crossover times at elevated temperatures can be readily achieved. An attempt is made to develop a sound qualitative understanding of the effects of base drive upon overall transistor performance. A charge control concept is utilized to bridge the gap between stimulus (base-drive) and response (collector current and voltage).

INTRODUCTION

The desirability of high-speed, rugged, and reliable solid state switching devices has been clearly established not only on theoretical bases, but by many years of practical experience. Recent emphasis has been focused onto the emerging power FET technologies; however, it must be remembered that the other applicable technologies are continuing to evolve. A new "third generation" of high-voltage bipolar switching transistors has emerged within the last three years and is available from at least two viable sources. These improved bipolar power transistors can be characterized in general as combining two qualities which were thought to be mutually exclusive only a few years ago: extremely fast switching in concert with substantial reverse bias safe operating area. Moreover, the effects of increasing junction temperature have been reduced to a level where operation at switching frequencies approaching 100kHz is practical.

The intent of this paper is to acquaint the reader with this class of high speed bipolar transistor and specifically to demonstrate methods of more effectively utilizing the full available capability of this device.

In order to develop a sound qualitative understanding of the effects of base drive upon overall transistor performance, a simplified visual model of a transistor cross section will be used throughout. This will effectively bridge the gap between the stimulus (base drive) and response (collector current and voltage), thereby helping the user to deal with the non-ideal behavior so often observed with high voltage switching devices.

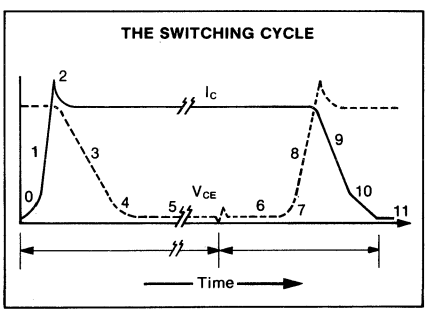

FIGURE 1

Figure 1 Reference	Condition
	TURN-ON:
0	Turn-On Delay
1	Collector Current Rise
2	Rectifier Recovery Current
3	Collector Voltage Fall (Initial Edge)
4	Collector Voltage Tail-In ("Quasi-Saturation" or "Dynamic Saturation")
	ON:
5	Saturation or Near-Saturation
	TURN-OFF:
6	Storage Delay
7	Collector Voltage Lift-Up
8	Collector Voltage Rise
9	Collector Current Fall
10	Collector Current Tail-Out
	OFF:
11	Blocking

TABLE 1—Switching Cycle Terminology

*Originally presented at the International Telecommunications Energy Conference, Washington, D.C., October 1982.

Shown in figure 1 is a rendition of the complete switching cycle. The numbered portions depicted in this figure are tabulated for reference in table 1.

THE SWITCHING ELEMENT

The high voltage device displays a transition region between the saturation characteristic and the active region often referred to as Quasi-saturation (figure 2). This is a by-product of the methods used to obtain high voltage in transistors. The dashed line labeled R_C exists for low voltage devices but usually lies so close to the saturation characteristic as to be nearly indistinguishable. In figure 3,

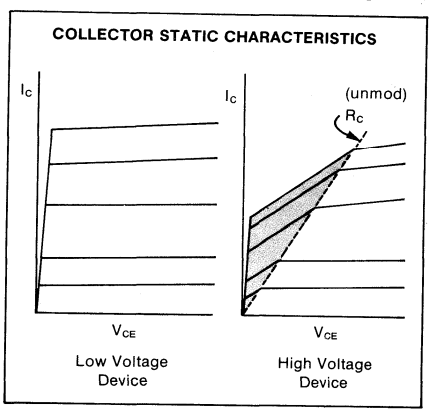

FIGURE 2

simple block diagrams of low voltage and high voltage transistors are shown. The variable resistances shown in the collectors can be thought of as a measure of the *Thickness-Resistivity* product. In a 400 volt switch, for example, the collector region resistance product may be on the order of 15 times greater than the resistance product of a 100 volt switch. This accounts in part for the collector characteristics shown in figure 2.

The thick collector regions associated with high voltage transistors dominate the switching, current handling, and saturation characteristics of such devices when operated at useful current densities.

In order to more fully understand why the collector region plays such an important role in the dynamic behaviour of high voltage transistors, we will endeavor to fall back on perhaps the most basic tool used to describe practically all semiconductor devices: *Charge Control*. In the qualitative treatment which follows, a simplified approach will be used which addresses two properties of charge in the transistor: *Rate* and *Distribution*. *Rate* is the speed with which charge is being injected into or withdrawn from the structure. *Distribution* is simply the location of this charge within the device. The structure used herein for demonstration purposes will be a cross-section of the region surrounding an emitter of a switching transistor as shown in figure 4.

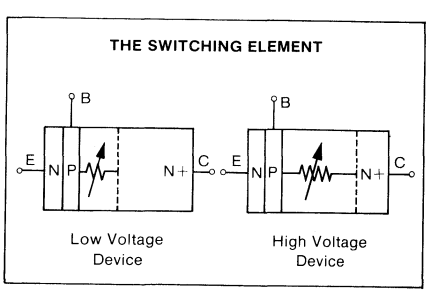

FIGURE 3

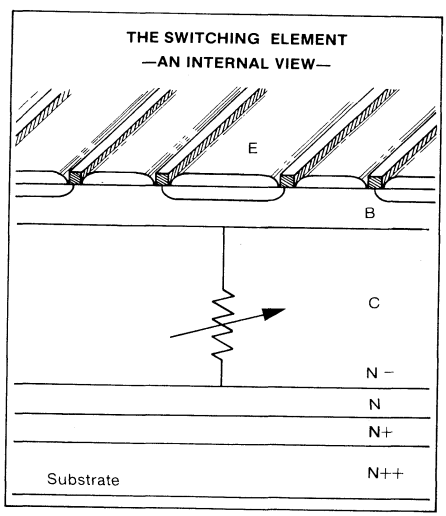

FIGURE 4

BASE RESISTANCE

It has previously been stated that the collector region contributed substantially to the observed switching performance of the high voltage transistor. Another physical attribute which plays a major role in the dynamic characteristics of such devices is the well publicized base spreading resistance, r_b'. Referring again to figure 4, this parameter is often simply described as the lateral resistance of the base region.

Since the base resistivity beneath the emitter is much larger than that in the vicinity of the base contact, the dominant share of resistance by this definition can be found beneath the

emitter. In order to avoid repeated long descriptions of various regions within the base, three terms will be employed with reference to distinctly different locations within the base:

1) Near base: Those regions of the base located directly under base contact metalization. (Resistively "near")

2) Peripheral base: Those regions of the base located beneath the outer edge of the diffused emitter.

3) Remote base: Those regions located beneath the center of emitter stripes or in other regions made resistively "remote" from the base contact by various combinations of distance and geometric factors. For example, emitter bonding pads can cover very remote base regions.

From an operational standpoint, a constant value of base resistance during the switching cycle is clearly unattainable. For example, at turn-on the effective base resistance is a combination of near and peripheral components since the remote base is initially inoperative. At turn-off, conditions leading to current crowding beneath the center of emitters can cause the effective base resistance to rise substantially. This phenomenon is particularly evident in older technology transistors.

TURN-ON

Turn-On Delay—Turn-on commences when a current is driven down into the base of the switching transistor. Base current is best represented by some quantity of charge delivered at a particular rate. A larger base current yields a proportionally larger quantity of charge moving into the base per unit time.

In pushing the Base-Emitter of a 15 amp 400 volt transistor to the threshold of forward bias, this charge amounts to a few nanocoulombs which in most cases will be insignificant compared to the total charge delivered into and withdrawn from the base during the complete switching cycle. Inasmuch as collector current has not yet started to flow, the power dissipated during this delay period will also be inconsequential.

Collector Current Rise—The turn-on delay ends with the base-emitter junction brought to the threshold of conduction. As the base-emitter junction becomes forward biased, charge begins to diffuse across the junction. Relatively larger quantities of charge carried by the emitter diffuse back into the base due to the large difference in impurity doping levels.

Were the collector voltages to remain constant during collector current rise as well as the "Rectifier recovery" phase depicted in figure 1, the rate of rise of collector current would only be limited by di_B/dt and the instantaneous value of the current gain. The upper bound on collector current would be established by the high voltage current gain which is generally several times larger than its low voltage counterpart.

Rectifier Recovery Current—This portion of the switching cycle could be considered merely an extension of the collector current rise. The duration of this phase is established by other capacitive-acting components in the system (eg.: rectifiers, snubbers, and transformers) and an effort should be made to minimize this to the extent that it can be a source of substantial power dissipation regardless of the type of switching transistor employed.

Collector Voltage Fall (Initial Edge)—As collector voltage begins to fall (figure 5), collector current is flowing mainly through the peripheral base region. Base current flow toward more remote regions of the base results in a cumulative inward voltage drop in the base with an attendant decrease in emitter current in these remote regions.

The rate of fall of collector voltage during this time is determined by the amount of base current over and above that required for the continuation of transistor action (supplying collector current for the load). If the only impediment to collector voltage fall was the discharge of collector-base capacitance then the entire process of turning on could be on the order of 40 nanoseconds for a typical 15A transistor. Unfortunately this is not the case. While it is true that the slope of the initial edge may be consistent with this capacitive process, the level to which the collector voltage initially

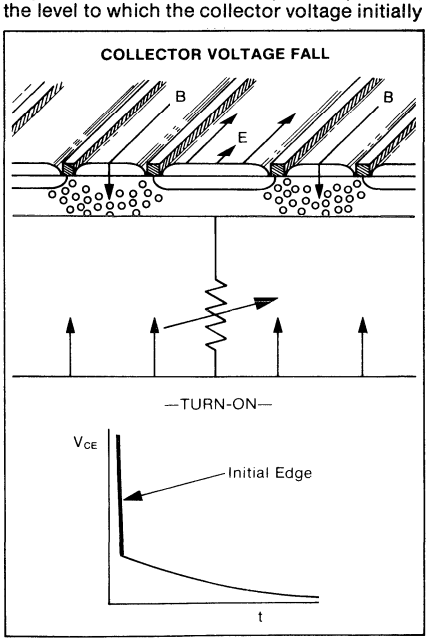

FIGURE 5

drops can be substantially greater than the saturation voltage.

Since the center of the emitter is not conducting, all the collector current is confined to regions beneath the emitter edges. Consequently, a relatively small area of the transistor is being used. The resistance per unit area of the collector is as yet unchanged, and rather large. Combining this feature with restricted conduction area implies a rather large voltage drop through the collector.

By increasing the amount of "emitter edge" it is possible to utilize more of the transistor area during turn-on thereby reducing switching losses. Therefore to promote rapid turn-on, a highly interdigitated emitter and base is desirable. This feature is characteristic of many transistors but do not be misled into believing that the transistor with the highest degree of interdigitation will automatically be the fastest. Other design limitations may prevail. The advent of the third generation switching transistors has been characterized by careful attention to this particular detail with an emphasis on overall performance.

Collector Voltage Tail-In (Dynamic Saturation)—Following this rapidly falling "initial edge" of collector voltage, a much slower process begins to take effect which will ultimately drive the transistor into or near full saturation.

In figure 6 it can be seen that the charge being driven into the near base has begun

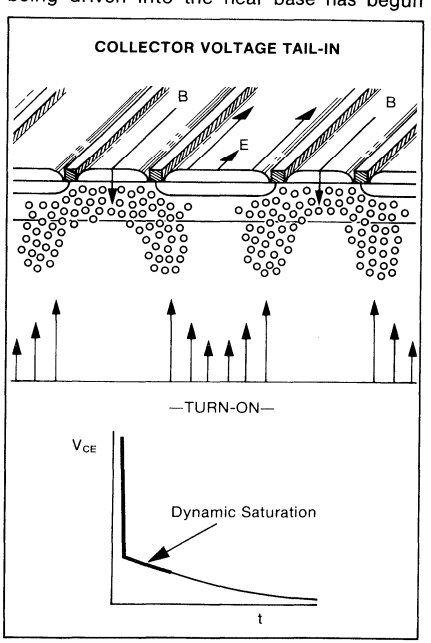

FIGURE 6

spreading laterally toward more remote regions of the base and vertically into the collector. The reason that this charge moves in this fashion can best be understood by first explaining the concept of *conductivity modulation* (or its inverse, resistivity modulation) and briefly restating some relevant properties of the semiconductor material.

Conductivity Modulation, Drift, Diffusion, and Lifetime: A Synopsis—For our purposes, a simple description of conductivity modulation will suffice: It is a direct result of *excess charge* in a semiconductor. The effect of this excess charge, then, is to lower the resistivity of the semiconductor to a value substantially below that established by impurity doping.

Drift is nothing more than a term used to describe the motion of charge in an electric field; holes drift in the direction of the field while electrons move against the field.

Diffusion will herein refer to the tendency of charge to move from regions of high concentration to regions of lower concentration.

Lifetime or minority-carrier lifetime refers to the natural tendency of oppositely charged excess carriers to combine with (or neutralize) one another. An unreplenished quantity of excess charge in a semiconductor will diminish to 1/e of its original value after a passage of time equal to the lifetime. So much for semiconductor physics!

It was previously stated that the initial-edge portion of the switching cycle ended with collector voltage which was resistivity and conduction area limited. The voltage drop in the collector beneath the peripheral base causes the collector-base junction in this region to be very close to forward bias.

The following conditions now exist in the vicinity of the peripheral base:

1) Base charge is being provided at a rate in excess of that required to maintain collector current.

2) Excess charge is therefore building in the peripheral base causing the resistivity in this area of the base to drop. (conductivity modulation)

3) The excess charge tends to spread out from the peripheral base in accordance with diffusion.

4) The collector-base junction becomes forward biased.

5) Excess charge diffuses slowly into the collector and collector conductivity modulation begins.

These conditions result in:

A) More remote portions of the emitter begin to operate since lateral voltage drops in the conductivity modulated base have been reduced. (increased conduction area)

B) Current flowing vertically through the collector results in lower cumulative voltage drops in the now conductivity modulated portions of the collector. (reduction of collector resistivity)

These two tendencies in combination will cause the collector to emitter voltage to drop, albeit at a slower rate. Figure 7 further illustrates the effects of the spreading "charge front" in the transistor. The electric field in the

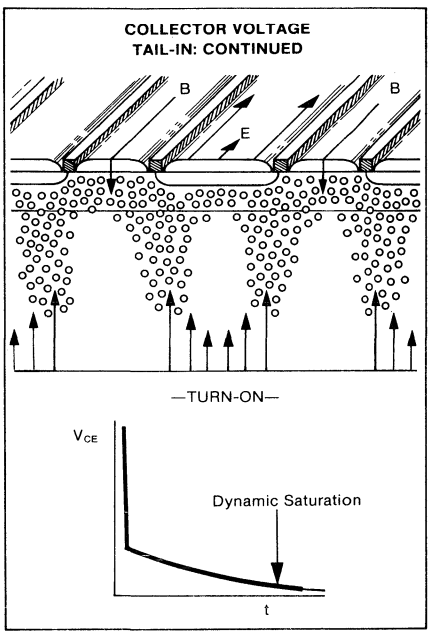

FIGURE 7

collector tends to oppose the advance of excess charge in the collector, retarding the rate at which it moves through the collector by diffusion. Drift and diffusion in this instance act in opposition. From a structural standpoint, then, it is very important that the initial edge" end point be as low as possible to reduce this field thereby favorably altering the "pressure vector" associated with the opposing forces of drift and diffusion. Again, this would justify the large emitter periphery characteristic of the third generation switch, and would also explain in part the turn-on behavior of the low voltage switch. The amount of time required to drive the transistor into saturation depends not only on the amount of emitter periphery, but also on the distance tha charge must travel to the far edge of the collector. It can be seen that if the collector is quite thin, the amount of time required to traverse it will be shorter and the total quantity of excess charge much smaller, thus explaining the excellent turn-on behavior of a low voltage device. (Figure 8)

Base Drive Effects at Turn-On—The saturation of the intrinsically slower high voltage transistor can be hastened by increasing the

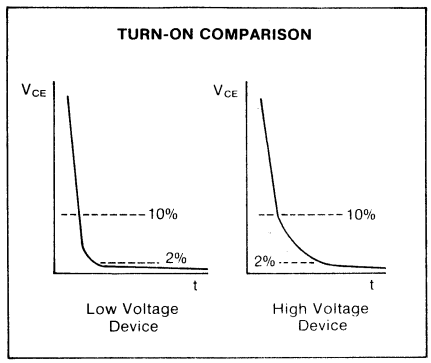

FIGURE 8

rate at which charge is applied into the base. This has the effect of supplying the required charge in a shorter period of time as well as supplying a little more push (increased charge gradient leading to more rapid diffusion) to that charge already in the structure to hasten its advance to the far side of the collector.

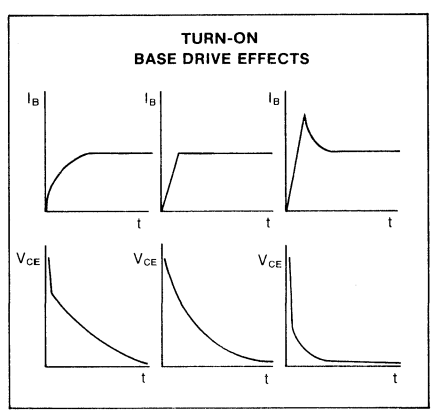

FIGURE 9

Figure 9 shows three possible base drive current waveforms and the resulting collector voltage waveforms associated with each. On the left is an inefficient base drive wherein the current rise time is relatively slow causing the initial edge of collector voltage to terminate at a much higher level and the voltage tail-in region to be much more pronounced. Needless to say, this can lead to substantial power losses at turn-on. Unfortunately this type of drive waveform is the rule rather that the exception. Two factors contribute in varying degrees to this behavior.

First, it can be the direct result of what might be termed limited compliance drive where a low voltage drive source (2-3 volts) such as the secondary of a transformer forms a drive

loop comprising a current limiting resistance in series with the secondary leakage inductance feeding the base. Naturally, the time constant of such a circuit will vary inversely with the secondary voltage of the drive transformer.

The second factor advancing the cause of poor base drive is a result of package inductance. For instance, the skin effect due to a rapidly rising emitter current in a magnetic package lead can add in excess of 10 volts to the measured base emitter voltage at the first instant on turn-on.[1]

Factoring in voltage drops due to self-inductance of pins and wires would at least double this value.[2]

The solution to this problem is a constant current base drive. The center set of waveforms of figure 9 shows that a current drive, where the base-emitter voltage does not restrict the rate of rise of base current, allows the collector emitter voltage to drop more rapidly toward saturation. Proportional drives utilizing high frequency drive transformers can be configured to yield this kind of result. Additionally, steered current sourses can be used effectively.[3]

Although the results obtained with current drive are to be preferred over those using limited compliance drive, there is still room for improvement. The best method for achieving rapid turn-on in the transistor is to overdrive the base during this interval. This procedure will yield the lowest loss turn-on available while still using conventional drive techniques.

ON

Saturation—Figure 10 is a representation of the state of the transistor after it has reached saturation.

Since excessive base drive at this point will not significantly lower conduction losses it may just as well be reduced to a level to adequately maintain saturation in preparation for a shorter *and more efficient turn-off.* Excessive overdrive in saturation will only serve to accumulate large amounts of charge in the collector which will move under the influence of diffusion to regions from which this charge may well be difficult to remove at turn-off.

TURN-OFF

Storage Delay—At the end of the "on" period, base drive is abruptly reversed and charge will now be withdrawn from the transistor (figure 11). Charge located under the emitter will continue to act as though it were supplied from the base terminal and find its way to the emitter base junction where it will maintain the transistor in its saturated state.

The process of recombination also tends to reduce the total charge in the collector, this being more important for lower levels of reverse base drive. At high levels of reverse base drive this charge can be withdrawn very rapidly

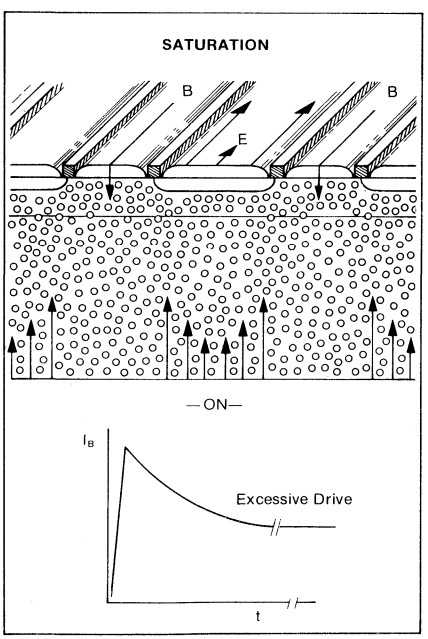

FIGURE 10

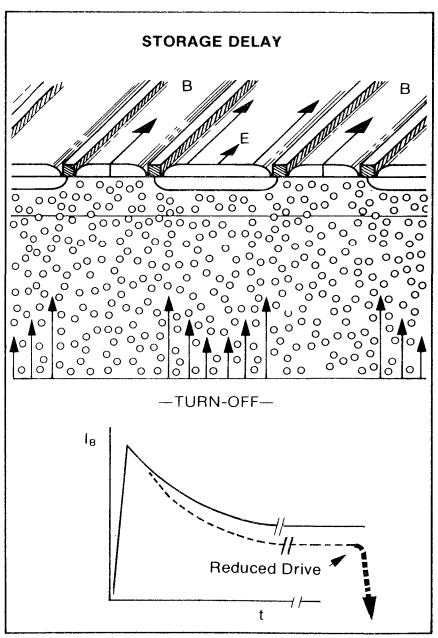

FIGURE 11

and in actual practice this is usually the case. However, with *some* high voltage transistors, attempting to withdraw this charge too rapidly can hinder the transistor during the turn-off interval when the collector voltage is rising and collector current is falling.[4,5]

Collector Voltage Lift-up and Rise—While the storage time may be reduced considerably by applying a large reverse base drive, the voltage rise and current fall times may be seen to decrease at first but then begin to extend as reverse base drive is further increased. This, of course, can lead to inefficiency in the switch. Shown in figure 12 is a structural diagram applicable during the collector lift-up and voltage rise period where the resistance of the collector is seen to begin to increase. As with turn-on this occurs for two reasons. The quantity of charge in the collector is being reduced thus causing the collector to become demodulated (its resistance is going up). The second effect which is taking place is a gradual reduction in the effective transistor cross-sectional area. A smaller portion of the transistor nearer the remote base beneath the emitter is conducting while the peripheral base-emitter regions have become reversed biased and therefore nonconducting. The charge remaining in the collector is caused to move toward the base by virtue of increased voltage from collector to emitter and that charge can either be withdrawn, if it comes up directly under a base contact, or it can continue to contribute to transistor action by coming up directly under the central region of an emitter. In the case of excessive overdrive at turn-off where reverse base drive is made very large, additional current crowding will tend to further reduce the effective area causing collector voltage to rise prematurely and actually increase turn-off dissipation.

Collector Current Fall and Tail-Out—Collector voltage continues to rise until a clamp voltage is reached. In an inductive load the current will then begin to fall. Since charge still remains deep in the collector as well as in the base region underneath central parts of the emitter, transistor action will continue even after voltage has stopped rising (figure 13). In the case where very hard reverse drives are employed, the amount of charge located deep in the collector may be large enough to increase the current fall time due to a collector current "tail".[6] The location of this charge depends upon the level of saturation employed during the on-phase of the switching cycle. Additionally, the quantity of charge will depend upon the maximum collector clamp voltage inasmuch as very low clamp voltages ($<$ ½ of BV_{CEO}) will prevent the electric field associated with the collector depletion region from extending deep into the collector where it can act to sweep out remote charge. This characteristic would suggest that high voltage transistors ought to be used only in high voltage applications.

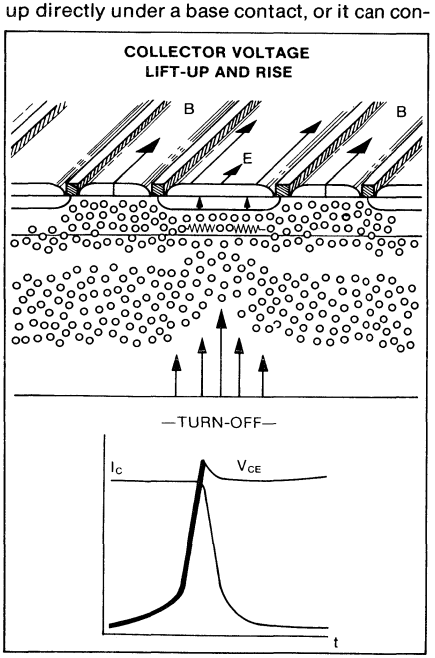

FIGURE 12

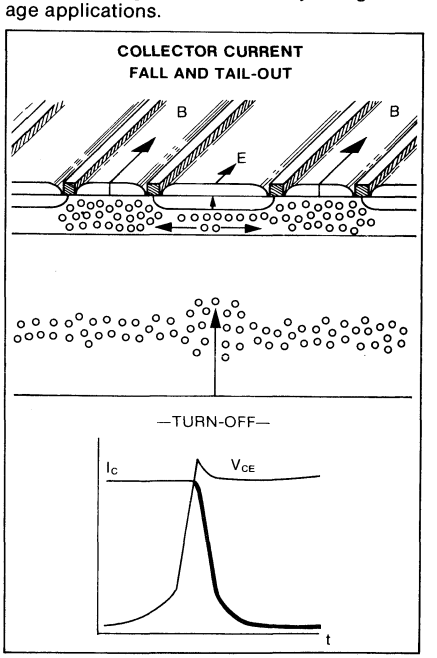

FIGURE 13

The Role of Base Resistance at Turn-Off— During the storage delay period, the base resistance will be extremely low since the peripheral base is still heavily modulated. However, toward the end of the storage time older technology switching transistors may show telltale signs that base resistance is about to rise substantially through the turn-off transistion. As excess charge is withdrawn from the peripheral base, the same current crowding phenomenon discussed earlier with regard to emitter area reduction will bring about ever-increasing voltage drops through the now *un*-modulated base regions between the peripheral base and the remote base. It is therefore possible to "run out" of base drive as the transistor turns off because of rising base resistance. Under these conditions, a slow rising collector-emitter voltage and more commonly a current tail will appear due to uncontrolled transistor acton at resistively remote base-emitter sites. With the application of substantial reverse base drive, where considerable charge remains in the collector as the voltage begins to rise, the sudden release of excess charge into the base may cause the collector voltage to momentarily drop as though the transistor was turning on again even though reverse base current has not appreciably changed.[7]

This disturbing trait has been addressed in the third generation switch by maintaining base resistance to *all* parts of the base at levels compatible with a wide range of reverse base drives. The changes made in such structures make the remote base much less remote. One aspect of this solution is of course a high degree of interdigitaiton. Another aspect involves the elimination of unnecessary or inoperative base regions. The base-to-emitter voltage of such devices is seen to remain positive until the collector current has fallen to near zero just prior to blocking.

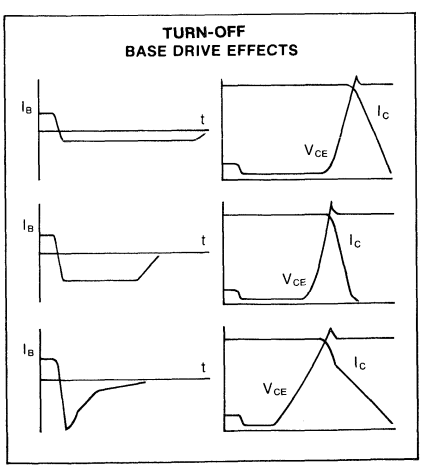

FIGURE 14

Base Drive Considerations at Turn-Off— Shown in figure 14 are the collector characteristics of an older switching transistor associated with various reverse base drive waveforms. Several features should be noted. Increasing reverse base drive in all cases reduces storage time. An optimum reverse base drive is achieved at a level intermediate between low reverse drive and high reverse drive. Low level reverse drive brings about longer switching times as a result of extended transistor action. High level reverse drive can result in increased power losses because much of the charge that might otherwise have been removed during the storage interval must now be expelled during the turn-off transitions.

Pulling the maximum amount of reverse current out of the base to improve the turn-off of a power transistor does have its limitations. These limitations apply not only to the efficiency of operation but also the ability of the transistor to withstand the peak stress which occurs when V_{CE} and I_C are simultaneously at their maximum values. The subject of base drive effects on turn-off safe operating area is of great importance, but beyond the constraints of this paper. However, such efforts have been previously undertaken and are of great value in both the understanding and the application of high voltage switching transistors.[8] It can be demonstrated that the philosophy of uniformly minimizing base resistance is of vital importance in the achievement of transistor designs which are capable of being driven off safely with a wide range of reverse base drive currents. In the process of taking data to evaluate the switching characteristics of the **GSRU15040**, for example, reverse base drive was extended out to levels exceeding 9 amps (15 amps I_C). Collector clamp voltages were maintained at the rated 400 volt level and there were no failures. On the other hand, increasing reverse base currents to six amps caused failures on some "older" designs made elsewhere and also touted as rugged devices.

Turn-Off Performance of the GSRU15040— Up to this point the general operating principles of the high voltage switch have been discussed with limited reference to a real device. The charge control model has been developed to aid in the understanding and application of the high voltage bipolar transistor switch regardless of vintage. However, these same concepts have been instrumental in the design of a new class of high voltage devices referred to here as third generation. An example of the switching performance obtainable with this new class of bipolar transistors is shown in figures 15 and 16.

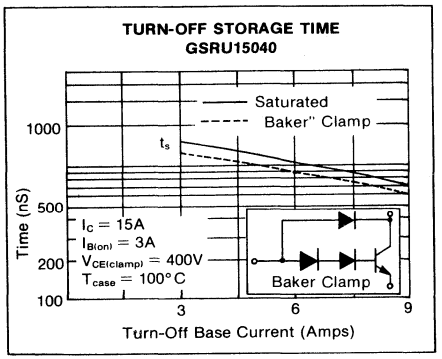

FIGURE 15

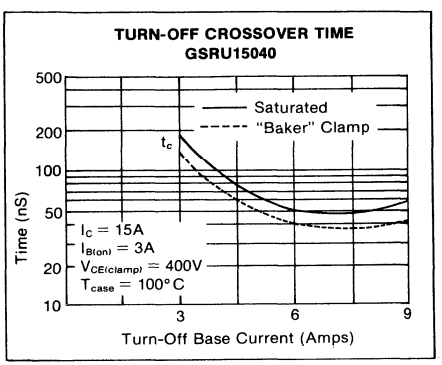

FIGURE 16

Based upon the data presented in these figures, a number of salient points can be discussed. First and probably the most dramatic, is the switching speed obtained. At 100°C case temperature, turn-off crossover times of 50 nanoseconds have been achieved. Consistent with the model previously presented, this characteristic is a strong function of reverse base drive. However, in figure 16 a point of diminishing return is reached. Increasing the turn-off base current to levels approaching I_C appears to cause a slight loss in turn-off crossover performance, although storage time continues to improve. Other similarly rated devices exhibited a much more pronounced upturn in crossover time and/or were not able to withstand the current and voltage stresses experienced during turn-off. With regard to the turn-off safe operating area of these new devices it should be noted that the 400 volt, 15 ampere test is not an upper limit. Considerable testing has demonstrated capabilities above 450 volts and 25 amperes (figure 17).

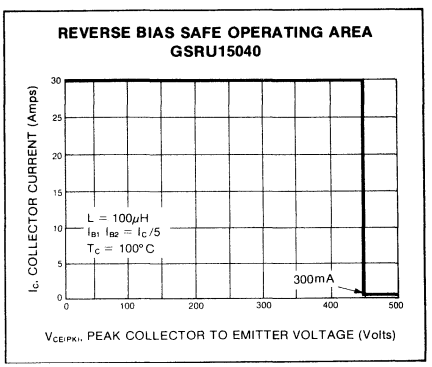

FIGURE 17

Further switching improvements can be achieved by limiting the degree of saturation, or excess charge within the device. Also shown in figures 15 and 16 are the effects of anti-saturation techniques (Baker Clamp). Based on the model presented one might reasonably expect greater improvement than that shown. This can be explained by the fact that a 2diode clamp, as in the example, still allows the device to be driven well into the quasi-saturation region.

Additional benefits appear to be derived from the "Baker Clamp" although not presented in this data. An apparent tightening of the switching characteristic spread occured. Also observed was an improvement in the turn-off safe operating area with earlier designs not designed to handle the high reverse currents.

Much work remains to be done in the characterization and application of these devices to extract their full capability. However, it is quite apparent that bipolars are alive and well and a new dimension has been added to high speed, high power transistor switching.

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HIGH VOLTAGE MOSFET AND BIPOLAR POWER SWITCHES

Close Cousins - Different Destinies

by
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and
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Since the advent of power MOSFETs with voltage ratings of 400 volts, their use in off-line converters has been strongly advocated by their manufacturers and others who feel inclined to use the latest technology components. Their cost effectiveness is subject to debate. To delve into the issues, this paper provides a background by considering some key factors in a power converter design such as choice of operating frequency and converter topology. Next a critical comparison of high voltage bipolar and MOSFET characteristics is given. Practical converter drive circuits for both the bipolar and MOSFET are described. From this background, the various circuits are examined for application of the MOSFET. It is found that no significant off-line power converter application exists where use of a FET as the main power switch is justified.

In the design of an off-line switching power supply, operating frequency and topology should receive first consideration. Next the choice of the power switch is of major importance because it determines many details of the design. The choice of the switch is complex and involves an examination of numerous factors such as the following:

1. Power dissipation of the output stage; that is, the switch and snubber. The switching portion of the power loss is not easy to determine because it is influenced not only by the load current, but also by the load line, which can be modified by snubbers, and the drive signal to the input of the power switch.
2. Level of complexity of the drive circuit required to achieve acceptable performance from the power switch.
3. Purchase and assembly cost of the switches and associated drive and snubber circuitry.

To aid or influence the power supply designer in making this choice, a number of papers have been written. Understandably, papers written by engineers associated with companies manufacturing power MOSFETs tend to stress the advantages of MOS while glossing over or ignoring some serious application problems. The few papers written by those favoring bipolars have also not covered all the issues. Within the framework of off-line power conversion, it is the purpose of this paper to bring all the issues into focus so that the designer will have clear guidelines for making the best choice of a power switch. In this case, the choice will be limited to a bipolar junction transistor or a MOSFET.

In order to provide the proper background, a discussion regarding the selection of operating frequency is given, followed by a brief review of the switch requirements imposed by some popular converter topologies. Next, a look at some fundamentals of bipolar and MOSFET transistors will separate those characteristics based upon physical principles from those that are somewhat dependent upon technology. While both device types have many similar characteristics, they differ markedly in others. Data taken on state-of-the-art power switches are given and some speculation on performance improvements made. It then becomes relatively easy to see which class of device will best meet the needs of a given design today and for sometime into the future.

CHOOSING OPERATING FREQUENCY

The availability of power MOSFETs has opened the possibility of designing power converters at switching frequencies into the megahertz range. Power MOSFET manufacturers stress high frequency operation, undoubtedly because the total power consumed by the MOSFET is much higher than a comparably rated bipolar until frequencies above 100kHz are used. Going to a high frequency, however, should be based on reasons other than a desire to use a MOSFET. In this section some criteria for choosing an operating frequency will be examined.[1]

The Case for High Frequencies

Since a dramatic shrinkage in size and cost of magnetic components (4:1 in volume) takes place when the power supply frequency is changed from 50/60 Hz line to the vicinity of 25kHz (a 500:1 frequency change), further reduction in their size and consequently in their cost might be expected as the frequency is further increased. However, the size of the magnetics changes rather slowly with frequency, so that a rather significant change is needed — to at least 200kHz — if any significant reduction (approx. 2.5:1) in magnetic volume is to be realized. The move to 200kHz permits the use of smaller valued capacitors; but electrolytics have too much effective series resistance (ESR) and inductance (ESL) to be of much use,so that plastic film types are better choices. By the same rationale, the components used in RFI filters can be smaller and therefore less expensive. In addition, the transient response of the system can be improved, proportional to the operating frequency, but this generally requires a change in the control loop design.

The Case Against High Frequencies

The difficulties with high frequency design provide a good basis for staying in the region of 25kHz. Problems occur with every part of the design, as follows:

1. Circuit Topology - The commonly used voltage fed circuits (flyback, forward, half-bridge, etc.) are not good choices. Current-fed or resonant converters show more promise but are not widely used. The best configurations for high frequencies are really not known at this time.
2. Control Circuitry - A number of IC pulse width modulators, op-amps, etc. are available for 25kHz switching but few are good to 200kHz. Modulator faults include: limited operating frequency, slow output pulse transistions, insufficient drive current, and excessive minimum dead time. Op-amps suffer from slew rate limiting, limited bandwidth and subharmonic oscillations.
3. Magnetics - present ferrite cores operate at 200kHz but the flux density must be reduced below that used at 25kHz to prevent excessive heating. Furthermore, standard core shapes have excessive window area for the reduced turns used at high frequencies. Consequently, the anticipated size reduction is only partially achieved. Skin effect necessitates the use of Litz, multifilar or copper ribbon wire to prevent excessive ohmic losses. New winding techniques must be used. To quote Severns:[1] "The greatest ingenuity is required in the winding of the transformer to reduce the leakage inductance and to produce symetrical and predictable voltages in the output windings." The final product generally has proportionally higher leakage inductance, a particularly problematic area if V.D.E. insulation requirements are to be met. Techniques used to reduce leakage inductance result in higher primary to secondary capacitance which causes current spikes in the power switch at turn on.
4. Capacitors - Very low ESL and ESR are necessary in the output filters. Electrolytics are not the best choice at 200kHz: plastic film types perform better and since only small values are necessary, some size reduction is available now but costs are still high. If a substantial holdup of the dc output is required or a severe transient load condition exists, high capacitance electrolytics will need to be used in addition to the plastic units.
5. Rectifier Diodes - Reverse recovery time (t_{rr}) losses are significant in junction diodes so that very fast relatively expensive types are required. Schottky barrier types are useful for low voltage supplies but their high capacitance causes problems similar to the t_{rr} of a junction diode. Some designers are advocating the use of low voltage power MOSFETs in a synchronous rectification scheme as a means of reducing rectification losses but problems need to be solved to have good high temperature operation.
6. EMI - The more rapid switching of a 200kHz converter produces severe EMI. The filters required are smaller but the RF energy extends into the VHF spectrum and permeates everything. Sophisticated filtering and shielding are required.
7. Circuit Layout - RF techniques must be used and RF bypassing provided at key locations.
8. Power Switches - Losses in the power switches will be higher at 200kHz than at 25kHz no matter what type of device is used. At 25kHz snubbing can reduce switching losses to vanishingly low levels while maintaining reasonable snubber power losses. At 200kHz, snubbing becomes more difficult: the smaller capacitor size and proportionately higher transformer leakage inductance allows voltage spikes to occur which may require use of a clipper circuit of some type. In addition, considerably more care is required in the drive circuit design in order to have fast transition times.

In view of the difficulties involved, it is easy to conclude that switching at frequencies of 200kHz and above is only reasonable under special circumstances. These are cases where the very minimum in size and weight are required such as in space, military portable, and airborne equipment where cost is not a key factor. These circumstances are not likely to be encountered in an off-line switcher. Obviously, the design cost is higher than for a more standard design until such time as much of the industry masters the art. In addition the semiconductor component cost is higher which usually outweighs the small cost savings in magnetic materials and capacitors.

SWITCH REQUIREMENTS OF POPULAR CONVERTER CIRCUITS

The popular voltage-fed converter circuits have been in use for such a long time that their original introduction is obscure.

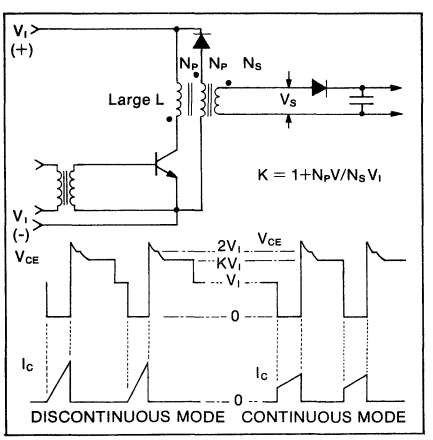

FIGURE 1. Basic flyback converter and waveforms.

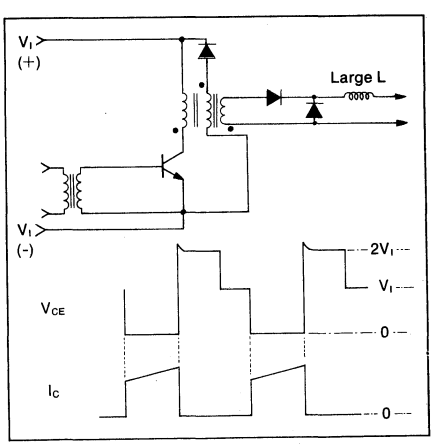

FIGURE 2. Basic forward converter and its waveforms

General descriptions of seven basic types are found in the literature.[2] They will be viewed here strictly on the basis of what is required of the power switch. They can be grouped into two categories, single ended and push-pull. *Figures 1 and 2* show the single ended converters and associated switch waveforms. The basic single transistor flyback and forward converter switches must block twice the maximum supply voltage plus a spike caused by leakage and layout inductance and the forward recovery transient of the clamp diode.

Push-pull configurations utilize the transformer more effectively and are used extensively above 500W. The basic circuit and half and full bridge versions are shown in *Figures 3, 4, and 5*. The waveforms show that the basic circuit must block $2V_I$ while the bridge circuits only need block V_I.

R & D interest at this time is being focused on new current fed square wave converters and resonant sine wave types. The number of topologies is virtually endless; Severns has identified about 40.[3] Regardless of the topology, the key characteristic in matching a transistor switch to a circuit is the load locus; that is, the current voltage trajectories during turn-on and turn-off. These trajectories must lie within the forward biased and reverse biased safe operating areas respectively. The naturally inductive locus during turn-off can be modified by snubbers to avoid overstressing the transistor and obtain the advantage of lower power dissipation. Note that the load locus during turn-off extends past $2V_I$ but during turn-on, the upper voltage limit is near V_I for the basic forward converter, the flyback converter operating in the discontinuous mode, and the basic push-pull converter. When snubbing is used, these voltage requirements fit in nicely with the characteristics of bipolar transistors as will be demonstrated later. The bridge circuits limit the voltage essentially to V_I.

Table 1 shows the peak voltage and current levels required for the various converter topologies for off-line switchers of different

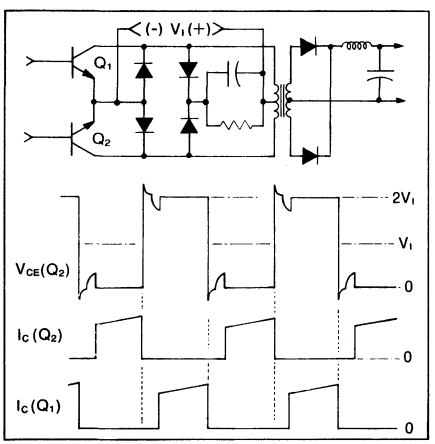

FIGURE 3. Basic push-pull circuit and its waveforms.

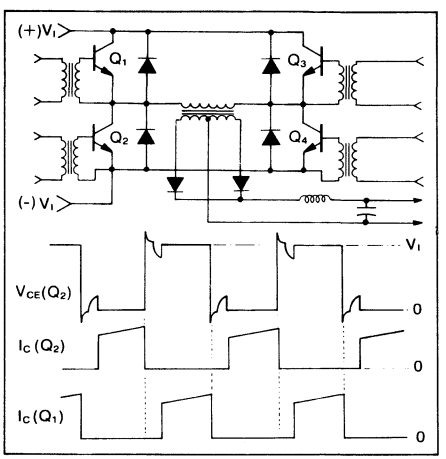

FIGURE 5. Full bridge circuit and its waveforms.

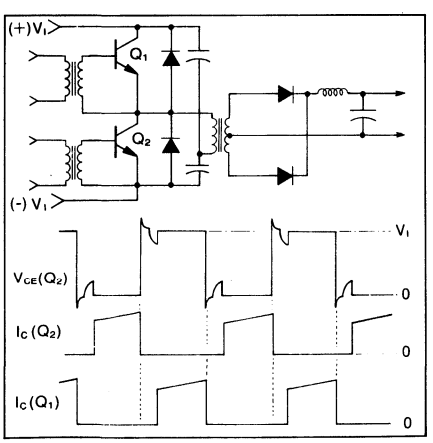

FIGURE 4. Half bridge circuit and its waveforms.

Circuit		Single Ended Converters		Push-Pull Converters		
		Flyback	Forward	Half Bridge	Basic	Full Bridge
Number of Transistors		1	1	2	2	4
V_M 240V Line / 120V Line		740V / 370V	740V / 370V	370V / 185V	740V / 370V	370V / 185V
Po (Watts)						
240V Line	120V Line	I_C*	I_C	I_C	I_C	
125	63	2.5A	1.25A	1.25A	0.63A	
250	125	5.0A	2.5A	2.5A	1.25A	
500	250	10A	5.0A	5.0A	2.50A	
750	375		7.5A	7.5A	3.75A	
1000	500		10A	10A	5.0A	
1500	750		15A	15A	7.5A	
2000	1000		20A	20A	10A	
3000	1500			30A	15A	
4000	2000			40A	20A	

*Discontinuous Mode
High Line Voltage = +10%, Circuit Efficiency ≈ 80%
Low Line Voltage = -10%, Transistor Conduction ≈ 45%

TABLE 1
Voltage and current requirements of transistors used in popular off-line voltage fed converters.

power capabilities. Leakage inductance spikes will add to the voltages; snubber networks, diode recovery currents, etc. will add to the currents.

Examples of matching the switch to the circuit are shown later in the article. Next, it is necessary to examine the basic properties of the two devices most suitable for high speed switching at power levels up to a few kilowatts - the bipolar junction transistor and the vertical MOS field effect transistor.

CHARACTERISTICS OF HIGH VOLTAGE BIPOLAR AND MOSFET POWER SWITCHES

Low power MOSFETs having maximum current ratings to an amp or so have been available for several years; however, only in the past three years have devices with low enough on-resistance to allow truly high power operation become available. Manufacturers of these devices have extolled their virtues,such as fast switching speeds, high input impedance (DC), and excellent safe operating areas. However, FETs also have their limitations and problems. In this section, characteristics of FETs and bipolars will be examined with the objective of determining which device fits best in certain converter applications.

Static Characteristics

Perhaps the easiest way to understand the similarities and differences is to examine briefly the physical construction of a high voltage bipolar and a vertical DMOS FET and their corresponding DC output characteristics. To start, assume both devices have the same chip area and the resistivity and thickness of the epitaxial collector or drain region is the same, so that the breakdown voltage of the collector base junction is identical in both cases. Note from *Figure 6* that the FET has a bipolar transistor associated with it so that it is not improper to refer to its collector-base junction. Hower and Tarneja[4] have shown that the output characteristics of both devices show the effect of this high resistivity n layer and that $R_C = R_D$ (see *Figure 6*). If the output characteristics of the bipolar and the FET are overlaid, the result is as shown on *Figure 7*. Note that a line having a slope of $1/R_C$ is the boundary between the active and quasi-saturation region of the bipolar and is the $r_{DS(on)}$ of the FET. By applying suitable overdrive to the bipolar, operation to the left of the boundary is possible, but this option is not possible with the FET. The bipolar thus can have a steady state conduction loss easily an order of magnitude less than the FET. Of course, operation in the quasi-saturation or hard saturation region stores excess charge in the bipolar. This charge must be removed during turn-off which causes the storage time delay.

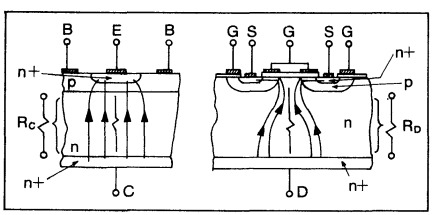

FIGURE 6. Cross-sections of a high-voltage bipolar and DMOS FET. The arrows indicate the dominant current flow paths when the device is "on". Area used for current flow is approximately the same.

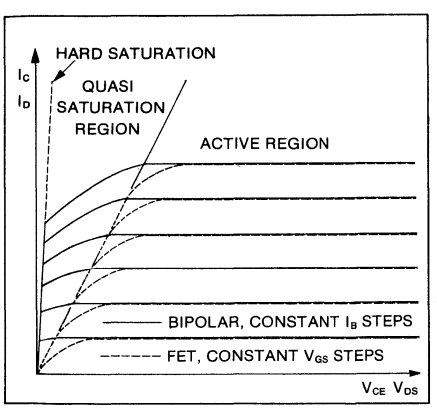

FIGURE 7. Low voltage region output characteristics for a bipolar and equivalent MOSFET.

A technique developed long ago by R. H. Baker to reduce storage time is shown in *Figure 8*. The feedback action of diode D_1 holds V_{CE} to a voltage that is one diode drop below the input; therefore the on-state operating point is held in the quasi-saturation region as determined by the number of diodes in the base string, D_3. During turn-off, reverse base current is channelled through D_2 (or a capacitor across D_3).

Any standard recovery low voltage diode which can handle the base current may be used in the base. The collector base feedback diode, D_1, must be a fast recovery high voltage type with a voltage rating at least equal to that of the transistor and a current handling capability which exceeds that of the input drive current.

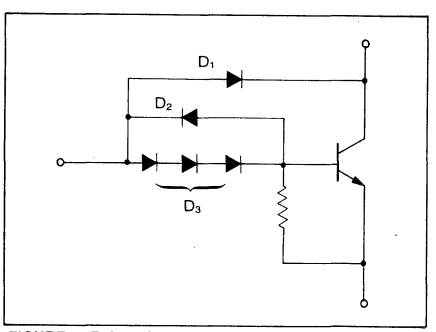

FIGURE 8. Baker clamp connection for reducing bipolar storage time.

Under conditions of drive current comparable to collector current, a common condition in a power converter under light loads, a recent article[5] shows the dramatic reduction in storage time achieved with the Baker clamp. Experience has shown that usually three series diodes for D_3 reduce storage time to less than a microsecond for most high speed, high voltage switching power transistors. It is possible to reduce storage time to the vanishing point by increasing the number of diodes until the operating point is out of the quasi-saturation region. Under this condition the drive voltage requirement, collector-emitter voltage, and switching speeds are quite similar to the equivalent FET.

The high voltage region of the output characteristic is shown in *Figure 9* for the devices constructed as shown in *Figure 6*.[6] Note that the FET has only one breakdown voltage, BV_{DSS}, as long as its parasitic bipolar is kept inactive. The bipolar shows a breakdown $V_{CEO(sus)}$ which is approximately one-half of the breakdown of the collector base diode (BV_{CBO}). BV_{CBO} equals BV_{DSS}. It takes careful design to switch the bipolar above the BV_{CEO} level but it can be done by controlling the load line such that it stays close to the voltage axis.

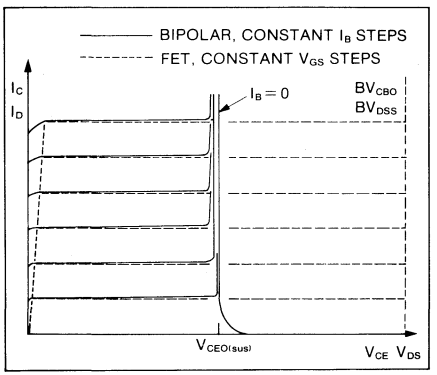

FIGURE 9. Output characteristics for a bipolar and a MOSFET showing breakdown region.

Let us suppose however, that the application is for a bridge converter where operation above BV_{CEO} is not practical. In this case the FET could be made with lower resistivity material and a thinner epitaxial n layer such that its BV_{DSS} equals BV_{CEO} of the equivalent bipolar. A significant improvement results, as the resistance R_D (and R_C) is proportional to $(BV_{DSS})^{2.3}$. Thus a reduction of BV_{DSS} from 800 volts to 400 volts results in a decrease of $r_{DS(on)}$ by a factor of 5, a significant decrease but not one which allows the FET on-state voltage drop to equal that of the bipolar.

The actual difference between a FET and third generation[7] bipolar when the V_{CEO} of the bipolar equals the BV_{DSS} of the FET is shown in *Figure 10* for commercially available devices having approximately the same size chip (1/4" x 1/4"). Note that the FET suffers from current modulation; i.e., no amount of overdrive will keep $r_{DS(on)}$ constant. (Values quoted on FET data sheets are usually well below maximum rated current.) In addition, $r_{DS(on)}$ increases significantly with temperature having roughly twice the value at 125°C as at 25°C for a 400 volt part. *Figure 11* shows the effect of temperature on the devices used for *Figure 10*.

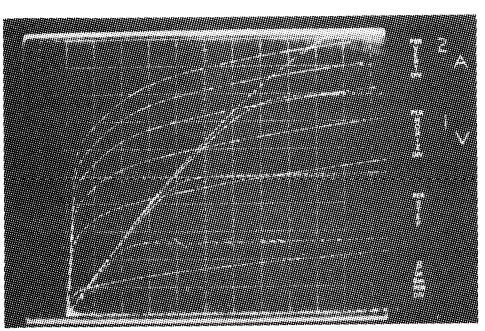

FIGURE 10. Comparison of the output characteristics of MOSFET and bipolar transistors having the same size chips. BV_{CEO} = BV_{DSS}

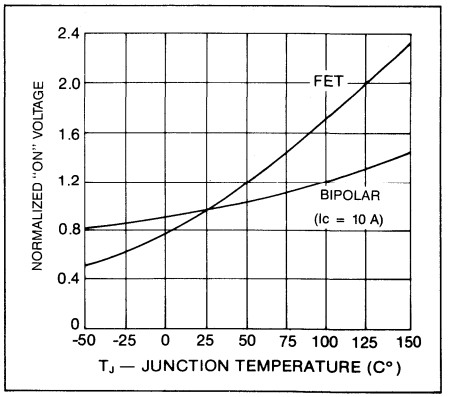

FIGURE 11. Temperature behavior of on-state voltage for the transistors of Figure 10.

FET Failure Mode

The FET appears electrically to have a "free" built in reverse diode which sometimes can be used as a circuit element. It is not very fast, however, and therefore creates problems in high frequency switching. Only one article[8] (to these authors' knowledge) has admitted that use of this diode can lead to device failure. The diode characteristic is derived from the parasitic bipolar transistor which is used to support the FET as shown in *Figure 6*. The base is shorted to the emitter by source metalization in the MOS structure. Consequently, the equivalent circuit of the FET is described by *Figure 12*. When using this "diode", it must be borne

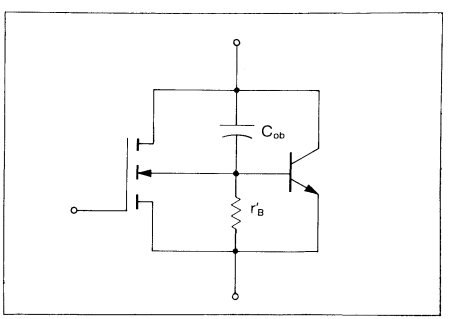

FIGURE 12. MOSFET equivalent circuit showing presence of the parasitic bipolar transistor.

in mind that the "diode" is part of a bipolar transistor with a BV_{CEO} of about one-half of the FET BV_{DSS} rating. Whenever current flows in the diode, the bipolar transistor has an opportunity to become active if its base-emitter can be forward biased by accumulated charge. Activating the parasitic bipolar transistor can lead to device failure because it is a very delicate structure with a poor safe area capability.

The usual failure scenario probably proceeds in the following fashion. Consider the half bridge circuit of *Figure 13* using FETs as the switches and the integral diode as the catch diode. To start, assume the top transistor (Q_1) is off and the bottom (Q_2) is conducting. When the bottom transistor switches off at t_0 the inductive flyback causes a large positive voltage to be generated at the

common tie point; when it tries to exceed the positive rail voltage, the collector base diode of Q_1 conducts thereby clamping the voltage to the rail.

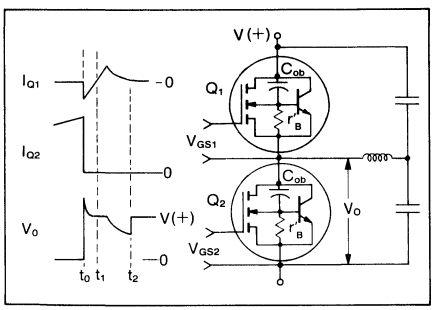

FIGURE 13. Output circuit of a half bridge converter using power MOSFET switches and associated waveforms.

Some portion of the minority carrier charge which has been injected into the "collector" or drain during this base-collector diode forward bias transient will return to the base during the recovery phase commencing at t_1. The charge in the base is further increased by the current being fed into the base via the collector base capacitance (C_{ob}) due to the rising collector-base voltage. Depending upon the effectiveness of the internal short and junction temperature, the emitter-base junction may become forward biased at some location on the chip. As the voltage approaches the avalanche voltage (V_{CEO}), failure occurs at t_2 because of second breakdown.

One approach to avoid this problem is to use a FET with a higher voltage rating but this exacts a stiff penalty in terms of $r_{DS(on)}$. Another approach is to modify the circuit as shown in *Figure 14*. In principle the Schottky series diode insures that all the flyback current goes through the shunt fast recovery rectifier so that the diode within the FET cannot store charge. Besides the obvious penalty of the extra components, additional power is dissipated in the Schottky because it must pass the full load current. The scheme is not entirely foolproof because the high capacitance of the Schottky diode will feed some current into the FET during flyback.

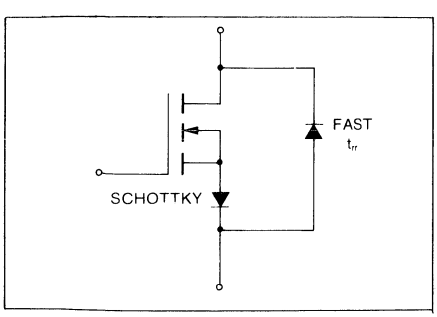

FIGURE 14. Circuit to prevent parasitic transistor conduction of reverse current.

Switching Performance

The final area to be considered in choosing between a power MOSFET and a bipolar is the switching performance. One can logically argue that when a circuit is switching at frequencies above 20kHz, true steady state may not be achieved before a change of state occurs.

Turn-on Characteristics

Figure 15 illustrates the time to reach steady state when turning on a transistor. The time beyond the usual 90%-10% fall time of voltage is referred to as dynamic saturation[9] time. The transistors used are the 1/4" chip third generation bipolar and equivalent FET used for *Figures 10 and 11* (GSRU15040 and IRF451). Note that the FET displays a short period of dynamic saturation; it is caused by the drain-gate capacitance which increases rapidly with decreasing drain voltage and becomes quite large as its voltage polarity reverses. The FET reaches steady state in about 0.2μs at a level of 5 volts. The bipolar has reached 5 volts in one microsecond and continues to drop to a final level of about one volt, but it takes about five microseconds. The power represented by the turn-on times is about the same for the bipolar and the FET at 2.5μs which is the maximum theoretical on-time of a converter switch operating at 200kHz.

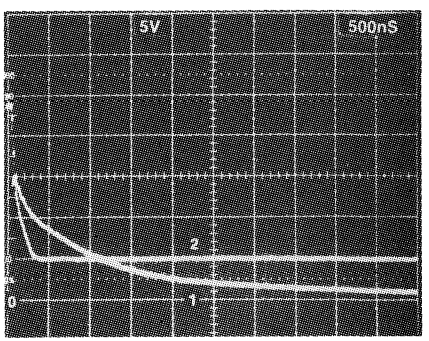

FIGURE 15. Turn-on behavior illustrating dynamic saturation for a third generation bipolar (1) and an equivalent MOSFET (2).

Bipolars can have better dynamic saturation than that displayed by the third generation part; however, the tradeoff is in turn-off speed and ruggedness. An example of excellent dynamic saturation is displayed by the 2N6655 transistor. *Figure 16* shows a comparison of the 2N6655 and the third generation part.

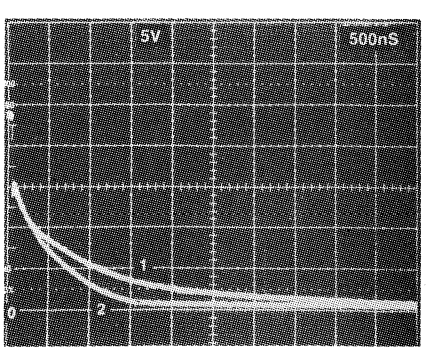

FIGURE 16. Dynamic saturation comparison between a third generation (1) and older high speed (2) bipolar transistor.

Turn-Off Characteristics

Turn-off characteristics are of the most interest for three reasons:

1. Power loads are usually more inductive than capacitive which causes high peak power dissipation.
2. Transistors have a switching reverse bias safe operating area (RBSOA) which may limit instantaneous voltage-current combinations to levels well below maximum ratings.
3. Bipolar turn-off characteristics can display unpleasant surprises if the drive circuit is not correctly designed to fit the particular transistor type being used.

A designer's dream has been to have a fast transistor which would safely switch off rated current to rated voltage. This dream has been fulfilled by most power FETs and most third generation bipolars. Therefore, use of snubbing[10] to permit transistor survival is not required in applications where voltages near the V_{CEO} rating will not be exceeded; however, snubbing may still be desirable in order to reduce stress on the power switch and improve overall system efficiency. Snubbing also reduces EMI generation.

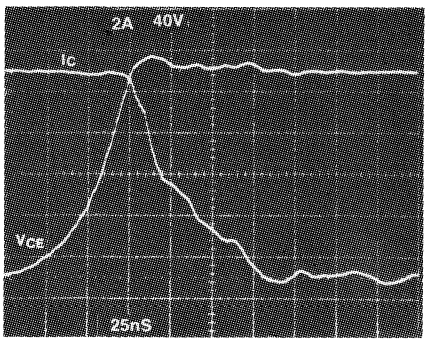

FIGURE 17. 2N6655 turn-off unsnubbed.

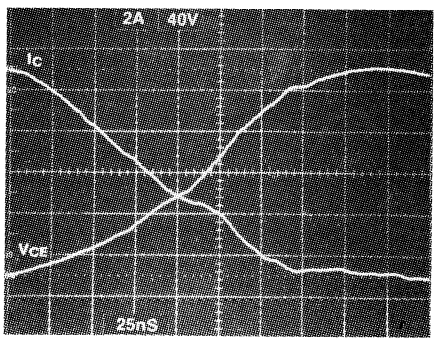

FIGURE 18. 2N6655 turn-off snubbed.

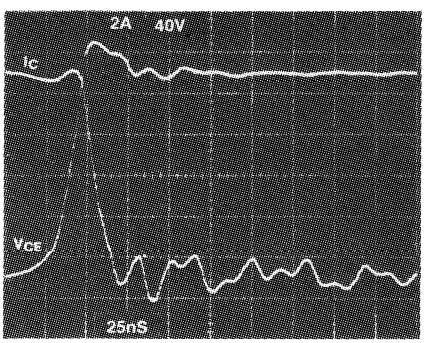

FIGURE 19. GSRU15040 turn-off unsnubbed.

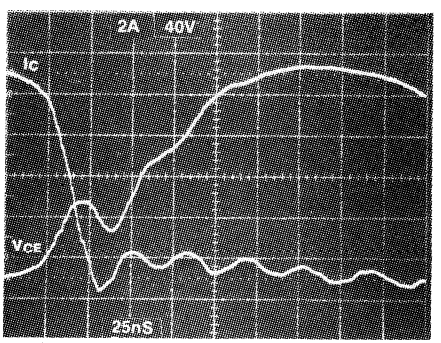

FIGURE 20. GSRU15040 turn-off snubbed.

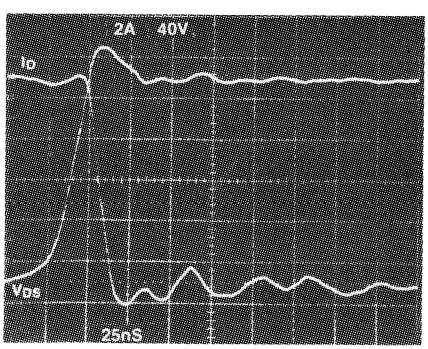

FIGURE 21. IRF451 turn-off unsnubbed.

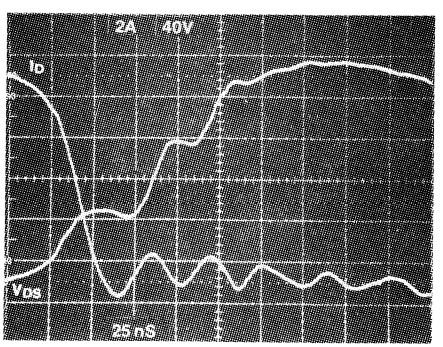

FIGURE 22. IRF451 turn-off snubbed.

The next six figures are photos of transistors working into a highly inductive clamped load with and without a snubber. With no snubber the 2N6655, an older generation bipolar, shows a cross-over time of 121 ns. Under identical drive conditions the third generation GSRU15040 shows 41 ns, while the IRF451 shows 39 ns. The third generation bipolar and the FET behave quite similarly. The advantage of the FET is only in the drive current; 0.5A of off drive is required to achieve the times shown. It was self-generated by using a 7.5Ω resistor from gate to ground (R_G).

Snubbing can be used to slow the voltage rise time thereby giving the current a chance to fall to a fairly low level before the voltage rises appreciably. Results using a .005μF capacitor are shown on *Figures 18,20, and 22*. The older bipolar part responds to this by increasing the current fall time to such a large extent that the usually specified inductive current fall time is of little value in trying to determine the dv/dt of the snubber. The change in fall time is much less severe with the third generation part and the FET. Key times taken from these waveforms are recorded in *Table 2*. Somewhat surprisingly, snubber action affects the fall time of the FET more severely than the fall time of the third generation bipolar. The change in time for the bipolar parts is caused by the reduced f, at low voltages and the stored charge removal process of the quasi-saturation region. FETs have higher junction capacitances at low voltages which explains why their fall time is also slower at low voltages.

The turn-off storage delay time is also of interest. During this time the voltage is low so that power dissipation is not a problem, but the delay, which is not constant as load current or temperature varies, must be considered when determining timing relationships in a converter. In single ended converters, the on time period must never exceed 50%; in a driven push-pull design; a dead time must be allowed so that all power switches are never on at the same time. Therefore, the storage time, or more properly, the variations in storage time, place a practical upper limit on the operating frequency.

Even though FETs are majority carrier devices, they also show a storage delay time. It is caused by the charge stored in the device capacitances, particularly that stored in the drain-gate capacitance, which is much larger than the specified data sheet values when the drain is negative with respect to the $gate_{(+)}$. For example a drain-gate capacitance which measures 400pF when the drain is 10 volts positive becomes 1800pF when the drain is over 3 volts negative relative to the gate. Since the gate to drain capacitance is a Miller capacitance, it effectively appears to the gate signal as a capacitance on the order of 0.1μF! (So much for the myth of the FET having a high input impedance; it displays only a high resistance.) Consequently it is not absurd to consider using a Baker clamp on the FET to keep operation out of the region of high capacitance.

Table 3 shows the results of storage time tests. The chief attribute of the FET is quite apparent; storage time is only 151 ns with 0.5A of off drive current, whereas the bipolars run just under a microsecond with 4A of off drive. Note the effectiveness of the Baker clamp. The bipolar storage times have been reduced to the vicinity of 400 ns while the FET storage time is a remarkable 18 ns. The turn off waveforms and data discussed were measured at 25°C. Temperature has virtually no effect on FET switching. It is well known that all the turn-off times for a bipolar increase with temperature and must be properly accounted for in a bipolar design. The third generation parts are less sensitive than older designs. For example, at the normal unsnubbed test conditions used for *Tables 2 and 3*, storage time, voltage rise time and current fall time increase by factors of 1.3, 1.5, and 1.2 respectively at a temperature of 100°C.

Transistor	Condition	t_c(ns)	t_{rv}(ns)	t_{fi}(ns)
2N6655	Unsnubbed	121	48	68
	Snubbed	111	120	125
GSRU15040	Unsnubbed	41	20	18
	Snubbed	24	101	27
IRF451	Unsnubbed	39	23	13
	Snubbed	27	100	32

I_C = 10A, I_{B1} = 2A, I_{B2} = 4A, $V_{BE(off)} \approx$ -6V
I_D = 10A, $V_{GS(off)}$ = 0, R_G = 7.5Ω, $I_{G(PK)} \approx$ 0.5A

TABLE 2
Turn-off times.

Transistor	Condition	t_s(ns)
2N6655	Normal	994
	Baker Clamp	350
GSRU15040	Normal	986
	Baker Clamp	441
IRF451	Normal	151
	Baker Clamp	18

I_C = 10A, I_{B1} = 2A, I_{B2} = 4A, $V_{BE(off)} \approx$ -6V
I_D = 10A, $V_{GS(off)}$ = 0, R_G = 7.5Ω, $I_{G(PK)} \approx$ 0.5A

TABLE 3
Storage time behavior.

DRIVE CRITERIA FOR POWER SWITCHES

In order to have fast switching speeds which in turn result in lower power losses, the power switch must be properly driven. Much has been written on the subject, to the point where one gains the impression that almost every designer has his own ideas. There are, however, a few design goals which are generally agreed upon as being important.

1. To achieve good noise immunity, it is best to have a very low impedance at the transistor input when it is in the off-state.
2. The on-drive should be fast and of a high amplitude at the leading edge to minimize turn-on losses, especially if the load appears capacitive because of the presence of a snubber or the recovery current of a catch diode.
3. After the initial peak, the amount of over-drive (voltage for a FET, I_{B1} current for a bipolar) should be kept to the minimum required for low on-state losses in order to reduce the turn-off storage delay. For bipolars, proportional drive schemes are attractive to achieve this condition.
4. When turning off bipolars, I_{B2} generally should not at anytime exceed I_C until I_C is relatively small, otherwise the emitter is cut off and the remaining charge must be removed as in a diode. Diode recovery usually is a slower process than transistor turn-off and produces a waveform often described as "tailing". However, third generation bipolars are relatively immune to tailing.
5. The off-drive should have a high amplitude to minimize storage delay and turn off time. For FETs, usually having the gate signal return to ground through a low impedance is sufficient. For bipolars, the nature of the off-drive depends upon the characteristics of the charge removal process of the particular power switch. The two extremes of drive are:
   a. The transition from I_{B1} to I_{B2} is gradual. It is controlled by a critically chosen inductor which slowly decreases I_{B1} and increases I_{B2} until a maximum is reached at the start of the current fall time. The slow change from I_{B1} to peak I_{B2} allows an orderly removal of stored charge so that deleterious effects during the fall time are avoided. *This technique is necessary to drive the older high voltage devices* and had its origin in the early days of transistor horizontal deflection circuits for television receivers. The penalty paid is a fairly long storage time.

b. The transition from I_{B1} to I_{B2} is rapid and a high level is maintained during turn-off. Third generation bipolars respond well to this drive method.

A fairly complete discussion of the turn-off process in a high voltage bipolar is given by Hetterscheid[12]. Several approaches are discussed and the rather complex waveshaping network of *Figure 23* is proposed to minimize the rise and fall times at the expense of storage time. In some cases this network is necessary but usually simplified versions are adequate. For example, in a flyback converter the current at turn-on is small, so that a fast rising high amplitude base current (I_{B1}) is unnecessary. The circuit of *Figure 24* is optimum, but some driving arrangements work better with the R-C network of *Figure 25*. In a forward converter, a fast drive pulse is usually needed because high collector current usually flows initially. Under these conditions the circuit of *Figure 23* may be optimum although the simple R-C circuit of *Figure 25* is usually adequate. Push-pull designs are more efficient if dead time is small because lower switch peak current is needed. Therefore, low storage time is important and the scheme using a series inductor is abandoned in favor of a simple constant current (high compliance) drive or an R-C network as shown in *Figure 25*. The values must be chosen carefully or poor fall time performance can result as shown in the Hetterscheid paper. When driven from a low impedance source, the capacitor provides high peak currents to shorten turn-on and storage time. The best choices for values of R and C and the levels V_1 and V_2 are usually determined empirically.

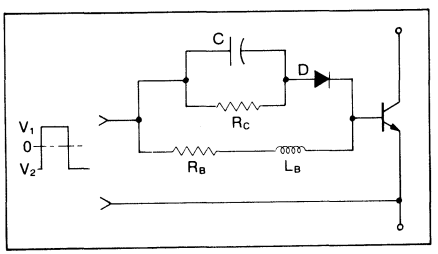

FIGURE 23. Waveshaping for bipolars when long storage time is acceptable and minimum rise and fall times are required.

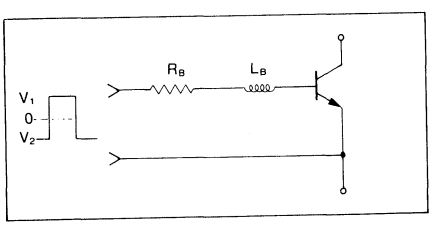

FIGURE 24. Waveshaping network when fast fall time is required but long storage and rise times are acceptable.

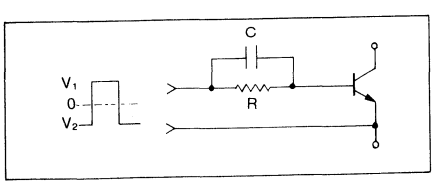

FIGURE 25. Waveshaping network for bipolars when short storage time is required. Rise and fall times are also fast.

The drive network for a FET operating in the 20 - 40kHz range need not be complex because the FET usually displays switching speeds faster than required. The circuit of *Figure 26* is usually used. A voltage regulator diode is advisable if any type of a-c coupling is used to avoid damage to the sensitive MOS gate and hold the signal swing to well defined limits. The series resistance serves to eliminate parasitic oscillations and may be used to slow down transition times.

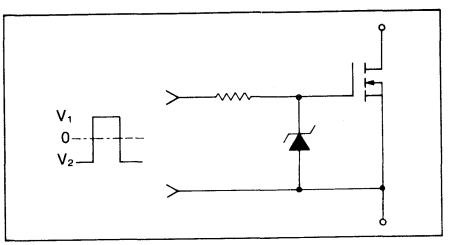

FIGURE 26. Waveshaping network for FETs.

Another consideration is whether the drive circuit needs to be isolated regardless of which type of power switch is used. Isolation is mandatory in the bridge configurations because of the totem pole connection. In the other circuits, the drive circuitry could be coupled directly to the power switching input as in *Figure 27* but this places its common connection to the negative rectified line. Called primary side control, the system arrangement eliminates the drive transformer but the control loop becomes greatly complicated. An opto coupler is required for isolation and though it is physically small it has limited bandwidth and requires an op-amp to compensate for its gain loss. The op-amp needs at least a 10 volt supply to operate; if not available from the switcher windings, another winding or a voltage doubler will need to be added. Some system specs such as foldback current limiting are difficult to achieve with this system. Consequently, primary side control is only practical for rather simply specified low power supplies which allow elimination of the 60 Hz transformer of the "housekeeping" supply for the driver and control IC.

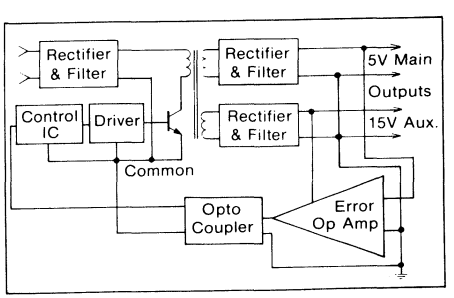

FIGURE 27. Primary side control system.

The other, more conventional, approach is secondary side control as shown in *Figure 28*. The drive transformer provides the necessary isolation and can also perform part of the waveform shaping needed to optimize the drive. The usual system requirements make secondary side control the preferred method. In addition, the common secondary side ground simplifies testing and servicing.

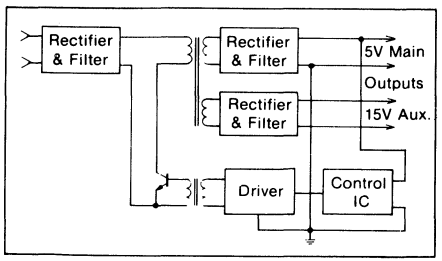

FIGURE 28. Secondary side control system.

SIMPLE EFFECTIVE DRIVE CIRCUITS

Circuits which form a good compromise between meeting the criteria outlined in the previous section and simplicity, which translates into low cost, are shown in this section. Two types are used: fixed and proportional.

Bipolar Fixed Drive Circuits

The simplest isolated or transformer coupled type drive circuits are those which produce a fixed amplitude base current independent of the I_C amplitude. They have been used successfully in off-line half and full bridge geometries up to about 1KW and can be used in medium power center tap/push-pull configurations. *Figures 29 and 30* illustrate two variations of this drive scheme.[13]

In *Figure 29* the two driver transistors Q_1 and Q_2 are driven with inverted base signals. In other words when the power switches are off, Q_1 and Q_2 are both on and the current through them is limited by R_P. To turn on the ΦA power switch, Q_1 turns off which causes current to flow in secondary winding W_1 so as to turn on ΦA power switch. At turn-on most of the drive current flows through C_1. Since the power switch is initially overdriven due to the low impedance of C_1 a rapid turn-on results. As C_1 charges I_{B1} drops and reaches the value limited by R_1 before turn off commences. The on drive level and R_1 are chosen to place operation just into the hard saturation region under worst case conditions.

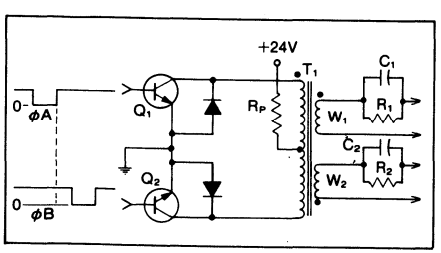

FIGURE 29. Fixed Drive Circuit.

To turn the ΦA power switch off Q_1 turns back on. This essentially shorts out the entire primary winding of T_1 and the impedance of this "short" is reflected to W_1 by the inverse of the turns ratio squared (i.e. 1/16). The actual transformer impedance is primarily determined by transformer leakage inductance. With this low impedance path across W_1, C_1 can now reverse bias the base emitter junction of the power switch. The I_{B2} will typically be 2 to 3 times I_{B1} for this condition which produces short storage and fall times. The "clamping" of the primary windings by having both Q_1 and Q_2 on is very important in providing a low impedance path for the charge on C_1. This allows for minimal storage times and rapid fall times for the power switch. To turn the ΦB power switch on, Q_2 must turn off and the same sequence follows for secondary W_2 and the associated circuitry.

The circuit of *Figure 29* is inefficient because the inverted drive of Q_1 and Q_2 may cause the 24 volt current drain to be excessively large with maximum current being drawn when both power switches are off. Therefore, the power loss becomes worse as the duty cycle decreases causing the overall converter efficiency to degrade as load current decreases. Almost all of this power is dissipated in R_P. An alternative circuit which adds some complexity but results in much better efficiency is shown in *Figure 30*. The basic operation of *Figure 30* is similar to *Figure 29*; however, the drivers Q_1 and Q_2 are driven in the normal (non-inverted) mode. The clamping action for proper I_{B2} generation is done by a separate clamp winding on the transformer and clamp transistor Q_3. This device should have the same current capabilities of the drivers and be able to switch efficiently at twice the inverter frequency. The clamp transistor is driven in such a way that it is on only when both drivers are off. The clamp and primary windings should have the same number of turns and be wound quadrafiler for maximum effectiveness. Diodes D_1 and D_2 should be 1 amp fast recovery types.

It should be noted that although *Figures 29 and 30* show two secondaries, four may be utilized when driving a full bridge inverter. In this case the available drive current will be split between the in-phase pairs of power switches. It follows that for the single ended converters only one secondary is used.

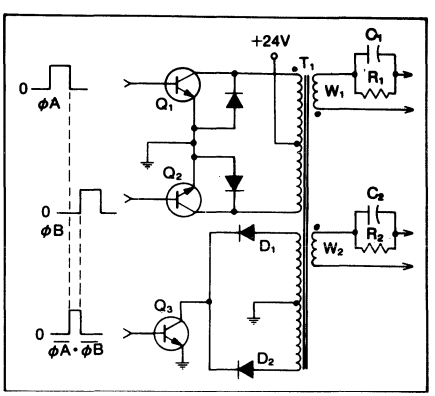

FIGURE 30. Low dissipation isolated fixed drive circuit.

A major disadvantage with all constant I_B drive schemes is that at low values of inverter current, the forced gain of the power switches becomes very low, i.e. the devices are heavily overdriven. The heavy overdrive often results in current tails during turn-off so the I_{B2} at maximum collector current should be chosen

to give acceptable performance, but not excessively fast fall times, which may degrade badly at lower collector currents. In addition, the heavy overdrive results in long storage times at light load currents. Consequently the push-pull circuits require a fairly substantial dead time in order to avoid fatal inverter cross conduction at maximum duty cycle. For most recent technology power switches, 4 to 5 microseconds of dead time is adequate. Worst case storage times are usually on the order of 3 microseconds.

In the event the 5 microsecond dead time is unacceptable, the Baker clamp circuit previously discussed will keep storage times generally a microsecond or less under all load conditions. The obvious trade-off in using the Baker clamp is minimal storage time and fast switching at the expense of saturation losses. When operating bipolar switches above 60kHz the use of the Baker clamp is usually well worth the trade-off.

A Proportional Drive Circuit

Another class of bipolar drive circuits which do not require any substantial power from the housekeeping or logic supply for effective bipolar control are regenerative or proportional drivers. Most of the published circuits are very effective but are also very complex.[14-15-16]

Figure 31 shows a relatively simple proportional driver which has proven very effective in providing the power switch with adequate on and off drive. An identical circuit is necessary for driving the phase B power switch of a push-pull design.

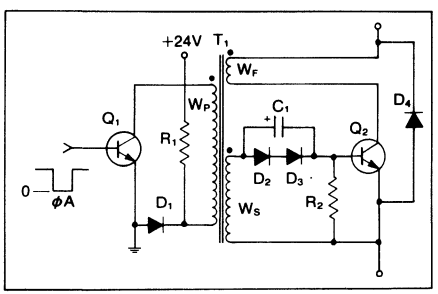

FIGURE 31. Simple proportional drive circuit.

The operation of the proportional driver is as follows: When Q_1 is on, current limited by R_1 flows through winding W_P of T_1 of a polarity such that Q_2 is reversed biased. At the same time the flux excursion in T_1 moves toward the negative saturation region. When Q_1 turns off, the magnetic field which has built up in the core of T_1 collapses and the dotted end of winding W_S becomes positive due to this flyback action. The induced voltage causes Q_2 to turn-on. Collector current flowing through feedback winding W_F induces current in winding W_S due to regenerative action. The ratio of base current to collector current is determined by the turns ratio W_F to W_S. A typical configuration is 8 turns for W_S and 1 turn for W_F which results in I_{B1} being 1/8 of the collector current. Keeping the ratio of I_C to I_{B1} constant eliminates most of the problem of storage time increasing as the load current decreases.

During the on-period, C_1 charges to the sum of the voltage drops of D_2 and D_3 in order to provide the reverse bias to Q_2 during turn-off. To turn Q_2 off, Q_1 turns on and winding W_P now acts like a clamp winding via diode D_1. This terminates the regenerative action in T_1 and allows C_1 to provide I_{B2} for the power switch as it discharges. After turn-off, current through R_1 will reset the flux in T_1 for the next cycle.

It is possible to supply several amperes of drive current while the current necessary from the housekeeping supply to reset the driver transformer may be under 100mA. With a proportional drive scheme, it should be noted that the drive circuit for a bipolar is not greatly different from that of a FET. All that is basically different is the elimination of the 1 turn feedback winding and the substitution of the waveshaping network. The FET drive circuit described next is the result.

A FET Drive Circuit

A suitable transformer coupled drive circuit for FETs is shown in *Figure 32*. It operates in a similar fashion to the bipolar proportional driver of the previous section but no feedback winding is required. Q_1 is normally on; the primary current flow induces a negative voltage at the gate which is clamped to a few tenths of a volt negative by the forward characteristic of the diode. When the driver is switched off, the large flyback voltage is clamped by a regulator diode D_2 chosen to provide enough gate drive to minimize the on-resistance. The clipping level is usually in the vicinity of 12 volts. By using the diode, the proper on and off drive levels are maintained despite duty cycle variations of the drive pulse. The resistor R_2, is chosen to achieve the desired switching speed from the FET.

At high frequencies, the drive circuit of *Figure 32* is usually not satisfactory. To obtain the high drive current required, R_2 and the impedance of the transformer must be small causing excessive power dissipation in the voltage regulator diode. The drive circuits of *Figure 29 or 30* are more appropriate because they provide a low-impedance drive with controlled voltage levels. Retaining the regulator diode is still good insurance against the FET gate falling victim to voltage transients; when high energy transients may be encountered, a TransZorb® is preferable to a zener. By careful design and layout, however, the diode may often be eliminated.

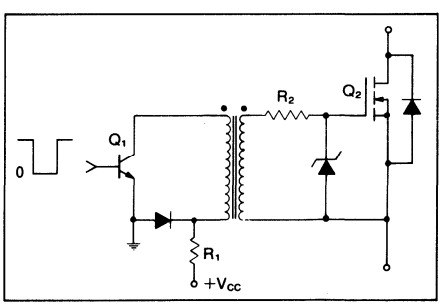

FIGURE 32. Suggested isolated FET driver circuit.

FET COSTS

To this point, the switch characteristics have been examined in some detail and appropriate drive circuits discussed. FET drive circuitry is simpler, which results in small cost savings, but high voltage FETs are now and will continue to be more expensive than equivalent bipolars.

At present, large geometry FETs are very expensive. For example, the single 1/4" chip IRF451 used for most of the actual data shown, costs $42.23 in quantities of 250-999. Other vendors offer similar - probably dual chip - parts in the $12.00 to $19.00 range.

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The "equivalent" bipolar, the GSRU15040, costs $8.50; however, the GSRU15040 far excells the IRF451 in on-state losses. A bipolar chip about one fifth the size of the GSRU15040 could be used in most 20-40kHz converter applications where the IRF451 would function.

FET manufacturers claim that prices will come down but that only occurs where one or more of the following events take place:

1. Production volumes go up. For this to occur a large market must be available to consume millions of units per year. No such market has been identified for the high-voltage FET.
2. Technological improvements in design and manufacturing techniques which allow more efficient utilization of the silicon chip and accordingly a reduction in chip size. At present, bipolars and FETs utilize about 50% of the chip. Some improvements, possibly up to 60% utilization, may occur but the better techniques will apply to both bipolars and FETs.

Therefore, barring some major technical innovation, even if the cost per unit area of a bipolar and a FET are equal, which is unlikely, the high voltage (450V) FET will require at least 5 times the die area to achieve equal conduction losses. Therefore, the FET can never approach the bipolar price.

MAKING THE CHOICE

With most of the salient factors discussed, it is now possible to make an intelligent choice. The question of frequency needs to be addressed first. Pshaenich[17] has run tests comparing the total losses in different bipolar transistors and FETS when switching a 3.0A clamped inductive load and a 2.5A resistive load. The frequency where the third generation bipolar losses had surpassed those of the FET varied from 75kHz to 100kHz depending upon the drive conditions. It is likely that the general results would be the same for the larger geometry transistors used in this article. Also using a snubber lowers switching losses and pushes the crossover frequency upward. Therefore FETs should be considered if switching frequency exceeds 100kHz; presumably all the difficulties of a high frequency design are acceptable in order to achieve some difficult goals such as fast transient response or minimal weight and size. Bipolars should not be ruled out at high frequencies, as some bipolar supplies with excellent performance have been constructed to operate at 100 KHz[18] and 500 KHz[19].

In the widely used frequency range of 20-40kHz, the issue becomes one of whether the simpler drive circuitry might offset the higher cost of the switch. To reach this conclusion, some guidelines as to the maximum allowable $r_{DS(on)}$ need to be developed. It is pretty generous to allow the power switches to consume 10% of the power output but this allows a quick evaluation of available devices to be made in order to find where FETs might fit in. Because of the different waveshapes and drive circuits in the different converter configurations, each one will have to be evaluated individually.

Flyback Converter

For the usual case of doubling off a 120 volt line to be compatible with 220/240 volt lines, an 850V FET is required. With the triangular waveshape of the normally used discontinuous mode operation, 50% maximum duty cycle, and using $P = I^2R$, average power dissipation is $P_D = I^2_{D(PK)} r_{DS(on)}/6$. Since the part will usually operate at 100°C to 125°C and specs are at 25°C, a part having half the $r_{DS(on)}$ from the equation must be selected. Using the temperature factor of 2 and the criteria of $P_D = 0.1P_o$ the maximum on resistance is $r_{DS(on)} = 0.3P_O/I^2_{D(PK)}$. Trying some values scaled from *Table 1* in the equation reveals that 7.5Ω is required for 100W output, which is about the upper limit used for the flyback configuration because of the large size of the transformer required at higher power levels. An 8Ω, 850 volt part, 100-up price is $8.00; suitable bipolars cost $2.00 to $3.00

The driver shown in *Figure 32* may be used for the FET. The transistor could be integral to the control IC if a suitable modulator IC is chosen.

The bipolar drive circuit of *Figure 29* works well in low power circuits. Proportional drive is more efficient and since the drive requirements are similar to that of the FET, Q_1 of *Figure 31* could be part of the IC control chip.

It is apparent that there isn't any large cost difference between the bipolar and the FET drive circuit. The decision of which type device to use becomes one of power loss and cost of the power switch. Since the bipolar device is lowest on both counts, it is the preferred device.

Forward Converter

The drive circuitry for the forward converter is similar to that for the flyback. For bipolars, the waveshaping circuit of *Figure 23* would yield the fastest response for a fixed drive arrangement, but proportional drive is preferred.

The switch power dissipation for a FET in a forward converter is $P_D = I^2_D r_{DS(on)}/2$. Using the same criteria as with the flyback converter, maximum $r_{DS(on)} = P_O/10\, I^2_D$. The usual range of forward converters is 100 watts to 500 watts. Below 100 watts the flyback is less costly and above 500 watts the push-pull types have a smaller transformer. Again, an 850 volt part is normally needed, although an interesting scheme has been proposed[20] as a means of lowering the voltage stress on the switch; the tradeoff is in higher peak current. Using the more conventional approach, the 8Ω, 850 volt part is only good for 125 watts. An 800 volt 2Ω part is available for about $20.00. This would allow operation to 500 watts, but judging from present pricing, there would be no point in using the FET for such applications now or in the foreseeable future.

Basic Push-pull

This circuit is not very compatible with FETs. Voltage ratings of 850 volts are required. The total power loss of the two switches is $P_D = I^2_D r_{DS(on)}$ at maximum duty cycle so that maximum $r_{DS(on)} = P_O/20\, I^2_D$.

The 8Ω part is good for only 250 watts, a level where it is usually uneconomical to use the push-pull configuration, the 2Ω part is too expensive.

Half Bridge

The equations for power loss and $r_{DS(on)}$ developed for the push-pull configuration apply. However, since the blocking voltage need only be 450 volts, a number of FETs are available and the on-resistance is much lower than with the 850 volt parts. For a 500 watt supply, a 1Ω FET is required (a 0.8Ω FET unit is available for $8.75), a 1KW supply requires a 0.5Ω FET ($12.78). The problem with this circuit is that external diodes must be added as in *Figure 14* in order to prevent an RBSOA failure from occuring during the "diode" recovery phase. The purchase and assembly cost of these components increase the price considerably over that of a bipolar; approximately by a factor of 3.

Full Bridge

The same arguments used for the half bridge apply to the full bridge with the same results.

Conclusion

Even when drive circuits are considered, the present costs and $r_{DS(on)}$ limits make FETs economically unattractive in the commonly used voltage fed converter circuits operating at under 100kHz. The relative cost structure cannot change significantly in the future because of the large ratio of the FET chip area to the bipolar chip area required to achieve comparable conduction losses.

POSTSCRIPT

Since the title of this article implies a different destiny for the high voltage MOSFET and the bipolar, one might ask, "If the bipolar's destiny is off-line conversion but the MOSFET is not practical, where is the MOSFET's destiny?" It is the authors' opinion that it will find use in RF transmitters, very high power linear audio amplifiers, and high voltage linear regulators where the high on-resistance is not a serious problem. The low voltage FETs (below 100V) have on-voltages similar to bipolars and may well find use in power conversion from aircraft and telecommunications sources, high speed linear regulators, audio amplifiers and many digital applications where they can be easily interfaced to logic circuits.

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Thanks are due especially to the following:

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APPENDIX

For proper operation of the proportional drive circuit (*Figure 31*):

1. The commutating diode D_4 should be connected around the feedback winding so as to prevent commutating currents from interfering with T_1's action.
2. For proper turn-off of Q_2, Q_1 must be saturated for the highest peak currents, reflected back through T_1. This will be the sum of the current in W_F and W_S translated by their respective turns ratios with W_P. A typical situation would be:

   W_P = 50 turns
   W_F = 1 turn
   W_S = 8 turns

   Assume at the moment of turn-off that I_C = 8 amps and I_{B2} = 2 amps. The reflected current to W_P will be:

   $$8x\ (1/50) + 2x(8/50) = 0.5 \text{ amps}$$

   The selection of Q_1 and its base drive should be able to accommodate this situation.
3. The value of R_1 should be chosen to provide enough current to reset the core of T_1 under worst case conditions. This will occur under maximum Q_2 duty cycle. The core cross sectional area, the switching frequency, and the forward drops of D_1, and D_2 and V_{BE} of Q_2 are all variables. Inadequate reset current (R_1 too high) will result in a premature time-out of T_1 of T_1 in the regenerative mode which causes Q_2 to turn off before Q_1.
4. Standard p-n diodes are adequate for D_2 and D_3. Diode D_4 should be a fast recovery diode.
5. Square loop toroidal cores give best results although any type of ferrite core will work.

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A Return from the Exotic — A Simple 1KW Off-Line Converter Using Two Power Switches In A Half-Bridge Topology

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An off-line 1KW converter is described. A discussion justifying the half-bridge voltage fed topology as a good choice for commercial applications is presented. Operation of the various circuit sections, such as the proportional drive scheme and the control loop, is described. Performance data are illustrated.

The primary impetus for this project originated during the development of the 2N6925 450V, 35A power switching transistor. It is a "third generation" (1) product featuring very fast switching, rugged RBSOA, and low on-state saturation voltage at a design center current of 25A. It seemed that a good way to show this transistor's capability would be to actually illustrate its performance in a well engineered commercial power supply.

The secondary impetus for this project came from observing a developing need to acquaint engineers newly entering the power conversion field with design practices that lead to a supply having reliable and trouble-free performance. Being able to build and experiment with such a supply would further assist in the educational process.

One of the first design engineers to use the 2N6925 in a power converter was co-author Frank Cathell. Excited about the transistor's performance, he called co-author Bill Roehr and the proposed project became a reality. The resulting supply constitutes a reliable design that includes the most commonly needed features such as overload protection, inrush current limiting, and AC line EMI filtering and transient protection. The circuit is relatively simple making it a valuable educational tool as well as a satisfactory supply for a mainframe computer. Similar power supplies, manufactured by several companies, have an outstandingly good field history.

In the following sections of the article, subjects such as the rationale for the choice of topology, circuit description, and performance data are discussed. For those interested in building the supply, a complete schematic, parts list, construction hints, and performance data are available from either author upon request.

Choice of Topology

Based upon previous experience with supplies operating above 500W, the popular half-bridge power circuit was chosen for this project. There are other circuits that could be used, but when all design constraints are considered, the half-bridge is preferred. Since this project is intended as an educational tool, the rationale for preferring the half-bridge circuit follows.

Table 1 shows a somewhat idealized summary of the voltage and current requirements for several popular converter topologies. The requirements are idealized in that no allowance is made for switching voltage spikes that could add 50 to 100V, or for current peaks caused by snubber networks, diode recovery currents, and transformer magnetizing current, that usually raise the peak current in the power switch by 10 to 50%. However, the table values do permit relative circuit comparisons to be made. Comments will be focused on 240V operation, assuming that voltage doubling is used for 120V.

Table 1. Voltage and current requirements of transistors used in popular off-line voltage fed converters.

Circuit		Single Ended Converters		Push-Pull Converters		
		Flyback	Forward	Half Bridge	Basic	Full Bridge
Number of Transistors		1	1	2	2	4
V_M 240V Line / 120V Line		740V / 370V	740V / 370V	370V / 185V	740V / 370V	370V / 185V
Po (Watts)						
240V Line	120V Line	I_C*	I_C	I_C	I_C	
125	63	2.5A	1.25A	1.25A	0.63A	
250	125	5.0A	2.5A	2.5A	1.25A	
500	250	10A	5.0A	5.0A	2.50A	
750	375		7.5A	7.5A	3.75A	
1000	500		10A	10A	5.0A	
1500	750		15A	15A	7.5A	
2000	1000		20A	20A	10A	
3000	1500			30A	15A	
4000	2000			40A	20A	

*Discontinuous Mode
High Line Voltage = +10%, Circuit Efficiency ≈ 80%
Low Line Voltage = -10%, Transistor Conduction ≈ 45%

Flyback Limitations

The flyback circuit can be dispensed with immediately. The transistor and transformer utilization is very poor. The required magnetic design would result in a ridiculously large and expensive power transformer. Flybacks are seldom practical above 200W.

Forward Converter Limitations

Forward converters have been described in the literature that operate at a kilowatt. However, transformer utilization is poor because only one-half of the B-H loop is used to deliver power. Accordingly, the transformer is twice the size of a push-pull design. Core reset must be provided via another winding that delivers the reset current to the DC input supply via a diode, but these elements can also add losses.

Although only one power switch is required, it must have high blocking capability (850V ratings are commonly used). The high voltage impressed on the switch reduces its reliability, as numerous studies indicate and field history confirms. Furthermore, in order to have reasonably good switching speeds and current gain, transistors with V_{CE} ratings of 400 to 450V must be used. These devices must be heavily snubbed so that collector current is fairly low when the voltage rises above the V_{CEO} (or $V_{CEX(SUS)}$) rating. The snubber is also another source of power losses and adds to the parts count.

A two-transistor forward converter is sometimes used. The second transistor contributes nothing to converter operation, except that it allows the voltage to be clamped to the input rail. This reduces the voltage stress by a factor of two or more. However, on-state power loss is doubled. In addition, a transformer coupled drive circuit to the second (upper) transistor, (or preferably both transistors) is required. A more cost effective design results by using the same two transistors in a push-pull arrangement.

Push-Pull Designs

Push-pull circuits need a transformer only half the size of the forward converter because the entire B-H loop is utilized. In addition, the output ripple frequency is doubled which permits reducing the size of the filter elements. The push-pull drive circuits are more complex than those used in single ended designs, but do not significantly affect reliability or consume much space.

Three push-pull configurations are in common use. From Table 1, the basic center-tap push-pull circuit looks attractive. It requires only two transistors and operates at the lowest current level possible for a given power output. However, it has two severe disadvantages which, in practice, have resulted in a poor field reliability history in off-line applications. For this reason, it is rarely used today in the United States.

The first disadvantage is that the circuit places a voltage stress on the power switch, which is worse than the single transistor forward converter. This stress occurs because the transformer requirements are such that leakage inductance is fairly high which enhances voltage transients. Accordingly, snubbing must be used. A spike clipper circuit may also be necessary to limit voltage peaks, but the clipper circuit consumes power.

The second disadvantage is core flux unbalance. The ferrites commonly used for core material are very easily saturated by the small amount of DC core flux resulting from the unbalance of the volt-second product of each half-cycle of AC induction. Since the saturation and switching characteristics of the power transistors cannot be identical, the core flux will "walk" to one of the saturated regions of the B-H curve. As a result of the diminished primary inductance on one half-cycle only, one transistor develops a large collector current spike. The extra dissipation in this transistor results in a serious loss of efficiency. In addition, the process is regenerative so that a thermal runaway situation is likely.

Two solutions are possible; one is to gap the transformer core so that some DC core flux does not cause saturation, and the other is to use current mode control. Unfortunately, a gapped core increases the leakage inductance which aggravates the spiking problem; a spike clipper becomes more of a necessity and it will dissipate power, further lowering efficiency. Current mode control may add additional complexity and cost, but does guarantee balanced switch currents.

The half-bridge configuration overcomes the two serious problems of the basic center-tap push-pull circuit. The circuit impresses no more than line voltage on the switches. Spikes are easily clamped to the rails via diodes. Core flux unbalance is eliminated because the transformer is capacitor coupled. Because the primary is utilized 100%, the transformer is smaller than the basic center-tap design and leakage inductance and interwinding capacitance are lower.

The price paid is: The coupling capacitor must be a non-polarized, low ESR, low loss design. The collector current is double that of the basic circuit. At power levels above 600W, the transistor choice narrows. In addition, each transistor should have its own transformer coupled driver circuit. None of these disadvantages is serious, however, and they are well worth the cost for the performance advantages.

The full-bridge deserves mention. It has the advantages of the half-bridge circuit and does not require a coupling capacitor if current mode control is used. It does require

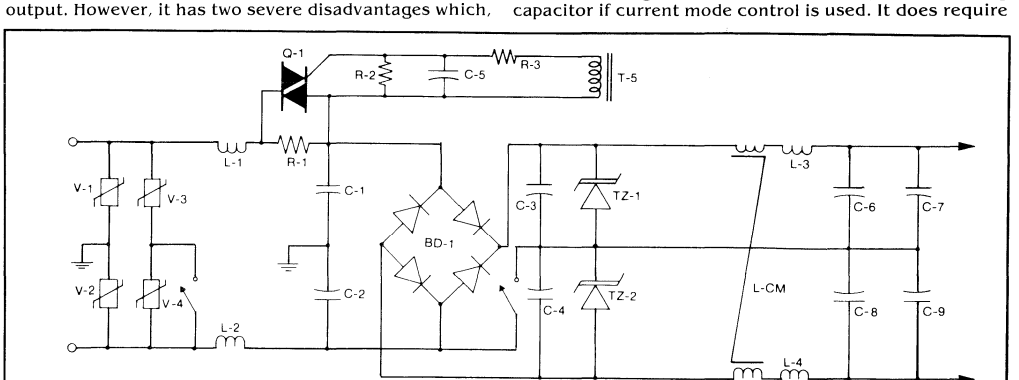

Figure 1. Input network includes transient suppression, EMI filter, rectifier, and ripple filter.

four transistors and associated drive circuits, however, so it is only used when the required power rating of the converter exceeds the capability of the half-bridge.

Circuit Description

The power supply is a single output, 1000W, off-line switcher providing 5V at 200A maximum. The converter topology is a conventional half-bridge utilizing only two bipolar switching elements. The switching transistors are driven by regenerative or proportional drivers with anti-saturation Baker clamps for fast switching. Output regulation and "hiccup" mode current limiting is achieved using the conventional, widely used SG-3524 PWM control IC.

Input Rectifier / Filter System

The input network is shown in *Figure 1*. The input transient suppressor and EMI filter are integrated into the rectifier and ripple filter system as described in an earlier paper (2). The EMI filter, composed of C-1 through C-4, L-CM and L-1 through L-4, attenuates common mode and differential mode conducted noise to levels below that specified by FCC level A. Transient suppression is provided by the varistors V-1 through V-4 and the TransZorb® suppressor strings TZ-1 and TZ-2. The chokes, L-1 through L-4, assist in diverting most of the transient energy on the AC line through the varistors and TransZorb diodes. Bridge rectifier BD-1, capacitors C-6 through C-9, triac Q-1 and resistor R-1 comprise the input rectifier / filter and inrush limiter section. The combination of the bridge rectifier and the filter capacitors are utilized in a conventional manner either as a voltage doubler or as a full-bridge rectifier, depending on whether the AC is strapped for 115 or 208 / 220 respectively. The nominal DC voltage developed for the inverter varies from approximately 290 to 335V, depending upon the AC line voltage applied.

Inrush limiting is achieved by allowing the input capacitors to be charged through R-1. After the inverter turn-on delay, shunt triac Q-1 is fired by the auxiliary gate winding on the converter power transformer T-5. When Q-1 is on, the input current is fed primarily through Q-1. R-2 and C-5 prevent noise tripping of Q-1.

Inverter Section

The inverter (*Figure 2*) is a half-bridge topology composed of switching transistors Q-2 and Q-3, commutating diodes D-4 and D-8, and power transformer T-5. The primary of T-5 is AC coupled via C-12 to prevent volt-second imbalances. A snubber network R-8 and C-13 is used. T-2 and T-3 are the drive transformers and T-4 is a current sensing transformer; their functions are described later.

Use of the 2N6925 transistor makes it easy to obtain a 1KW output at 40kHz with only two power switches. The key characteristics of this device are shown in Table 2 as presented on the manufacturer's data sheet (3). (Note that the 2N6924 transistor, which shares the data sheet, has the same specifications except for voltage ratings.) In addition to having low saturation voltage and fast switching, the switching safe area (RBSOA) is extremely

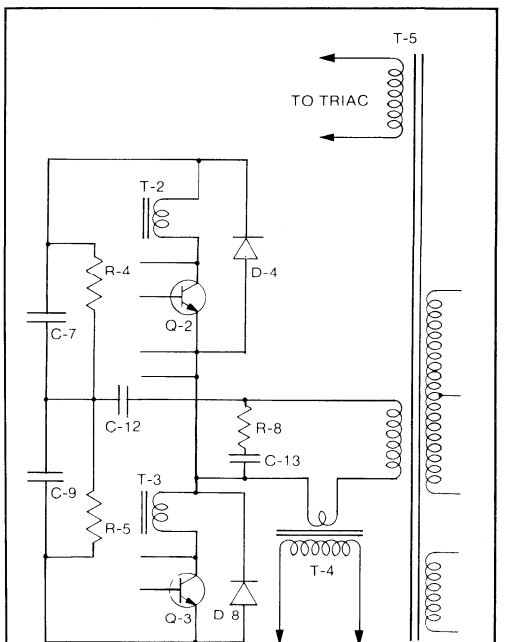

Figure 2. Half-Bridge Inverter Section

Table 2. Specifications of major interest for the 2N6924/25 transistor family.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)							
SYMBOL	**DESCRIPTION**		**2N6924**		**2N6925**		**UNIT**
V_{CEV}	Collector-Emitter Voltage, Blocking		550		550		Volts
$V_{CEX(sus)}$	Collector-Emitter Voltage, Inductive Switching		450		500		Volts
$V_{CEO(sus)}$	Collector-Emitter Voltage, Sustaining		400		450		Volts
ELECTRICAL CHARACTERISTICS (Applies to all types unless otherwise noted.)							
			T_C = 25°C		T_C = 100°C		
SYMBOL	**CONDITIONS**	**PART NO/NOTES**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**
h_{FE}	I_C = 25A, V_{CE} = 2.0V	Pulsed: Notes 1 & 2	8.0				
$V_{CE(sat)}$	I_C = 25A, I_B = 5.0A			1.0		1.5	Volts
$V_{CE(sat)}$	I_C = 35A, I_B = 9.0A			2.0			Volts
t_d	I_C = 25A, I_{B1} = 5.0A; **Resistive Load**, V_{CC} = $V_{CEX(sus)}$			20			ns
t_r				50			ns
t_{sd} (t_f) *	**Current Source Load**	Measured to 10V		1.0		3.0	µs
t_{sv}	**Inductive Load**			1.3		1.6	µs
t_{rv}	I_C = 25A, I_{B1} = 5.0A, I_{B2} = 10A; t_p = 30µs, L = 100µH, V_{CLAMP} = $V_{CEX(sus)}$			30		60	ns
t_{fi}				30		40	ns
t_c				50		90	ns

*Dynamic Saturation Time

Notes: 1) Measured using Kelvin connections.
2) Pulse measurement conditions: Length = 300µs. Duty cycle < 2%.

good. As *Figure 3* shows, these transistors will switch peak rated current to a voltage 50V above the specified V_{CEO} rating. Snubbing is therefore not necessary to insure transistor survival; however, some snubbing is used in the converter to reduce transistor dissipation and transient voltage ringing. Such practice is widespread in the industry because field experience has proven that snubbers improve reliability.

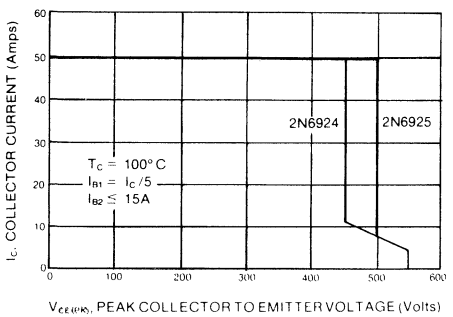

Figure 3. Reverse Bias Safe Operating Area.

Base Drivers

The power switches (Q-2 and Q-3) are driven by regenerative drive circuits that maintain a constant drive ratio (collector to transformer secondary drive current) over the entire inverter load range. A ratio of 6:1 was chosen for the drive transformer, which assures a low saturation voltage for the transistor at the peak collector current of 18A. Two identical circuits are used, one driving each power switch. Baker clamp diodes are also employed. The Baker clamp adjusts base drive in relation to the transistor's current gain, which enhances turn-off switching speeds and further helps to keep storage time regulated with variations in load current.

One of the base drive circuits is shown in *Figure 4*. It works as follows: When drive transistor Q-5 is turned on, the primary winding of drive transformer T-3 is clamped (shorted) and power switch Q-3 is turned off at this time. At the same time current through reset resistor R-29 causes flux to build up in the core of the driver transformer. In order to turn on switch Q-3, driver Q-5 is turned off. The flyback energy in the core of T-3 now appears as an on-drive voltage across the base drive winding of Q-3. Collector current flow in the feedback winding on T-3 keeps base current flowing into the switch by the ratio of the turns of these two windings. Hence, the base drive current is always a fixed proportion of the collector current. Base current flow through D-6 and D-7 develops a voltage across C-14. To turn Q-3 back off, Q-5 must be turned on again. This stops the regenerative action of T-3 and provides a low impedance path for the charge on C-14 to reverse bias the base-emitter of the power switch that turns it off. Primary current flow in T3 is composed of the reflected currents in the secondary windings; it flows through Q-5, D-25 and D-27. The primary is effectively shorted, which makes the secondary windings appear as very low impedances. Therefore, a fairly high IB2 is achieved without using complex circuitry.

Diode D-5 keeps the power switch more in quasi-saturation than hard saturation when in the on-state, thus aiding in fast turn-off. Base snubber C-15 and R-10 prevent ringing in the drive circuit.

The effectiveness of the base drive circuit is illustrated by the waveforms of *Figures 5* and *6*. The drive waveform is close to the ideal (4) for fast switching of bipolar transistors. The peak amplitude of IB2 is not exceptionally high — approximately 1.5A for 10A of IC — because spectacularly fast switching is not necessary in this application to achieve low power loss. The transistor turn-off waveforms show that the load line appears essentially resistive. Rise and fall times are approximately 100ns. Power loss during turn-off at full power output is an insignificant 3.6W per transistor.

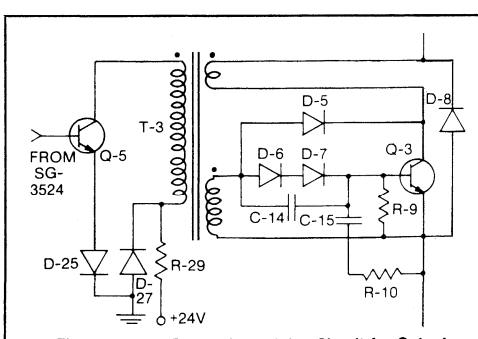

Figure 4. Base Proportional Drive Circuit for Output Power Switches.

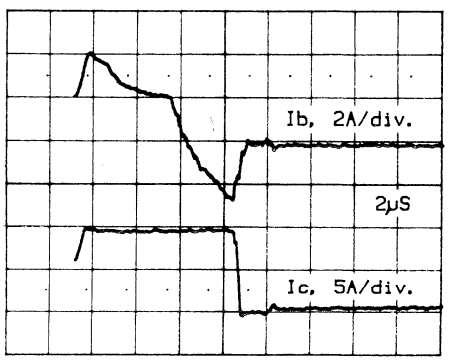

Figure 5. Base Drive waveform during a full converter cycle.

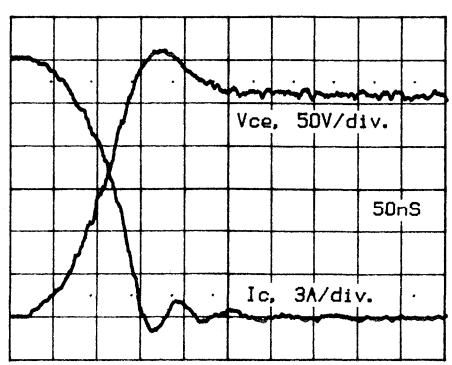

Figure 6. Transistor Turn-Off Waveforms.

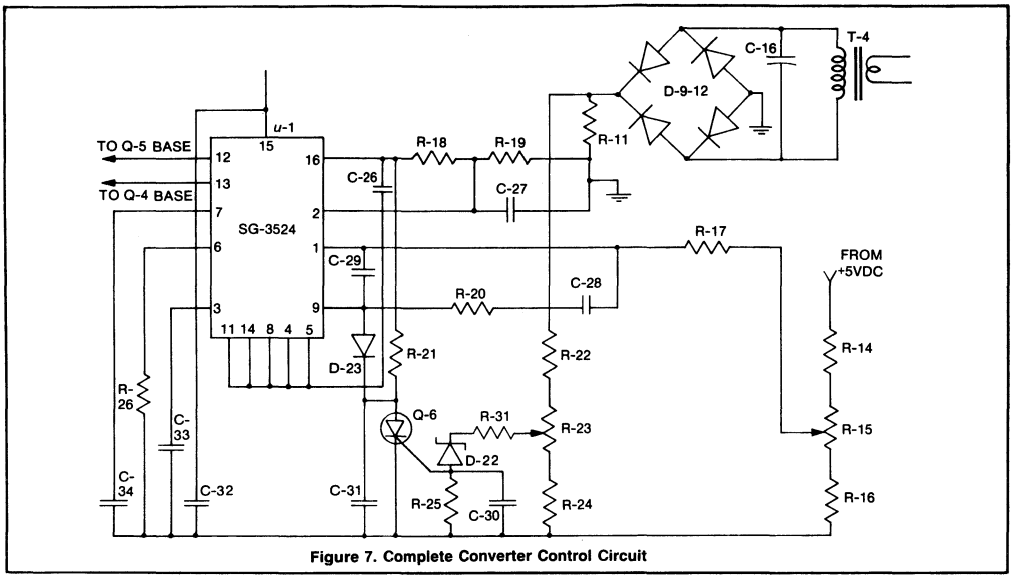

Figure 7. Complete Converter Control Circuit

Control Circuit

The power supply control circuit is designed around the SG-3524 pulse width modulator IC. The chip contains all the necessary functions for controlling a fixed frequency pulse width modulated switching power supply. The complete control circuit is shown in *Figure* 7.

The supply output voltage is sensed and divided down to 2.5V by R-14, -15, and -16. R-15 provides voltage adjustment which feeds into the control chip's error amplifier at pin 1. Closed loop phase compensation is provided by R-20, C-28 and C-29. The switching frequency is nominally 40kHz and is set by R-26 and C-34. Inverter dead time is set by C-33.

Current limiting is provided by sensing the peak primary inverter current with T-4 and rectifying the signal in D-9 through 12. If the peak current (due to an overload) creates sufficient voltage on the wiper of R-23 to exceed the zener threshold of D-22, SCR Q-6 will fire and dump soft-start capacitor C-31. This action will reduce the inverter pulse width to zero. In a short time, the current through Q-6 will drop below the holding level of the SCR. Recharging of C-31 through R-21 begins allowing the inverter pulse width to "soft-start." If the overload condition persists, this cycle will repeat and the inverter will alternately shut-off and then soft-start in a "hiccup" mode until the overload is removed. Capacitor C-30 prevents internal switching noise from inadvertently firing Q-6.

Other Circuits

The nominal control circuit operating voltage is approximately 24V. The control logic is initially powered on by a simple power supply composed of a line frequency transformer, a bridge rectifier and filter. Once the inverter has started, the logic power is obtained from a bootstrap winding on the inverter transformer. Since the line frequency transformer operates for a very short time, its VA rating and size may be quite small.

Secondary rectification of the main output is done by Schottky diodes in a full wave center tap arrangement. A secondary snubber network is required to attenuate voltage spikes on the diodes. The filter is choke fed.

Converter Performance

The converter's performance is satisfactory for most computer applications. Input dropout AC voltage measured 80V when strapped for a 120V input. Output ripple under full steady state load measured 20mV. The variation in DC output from full load 90V AC input to no load 135V AC input is only 27 millivolts. With a 50A load step applied at a slew rate of $1A/\mu s$, overshoot and undershoot measured 85mV. Efficiency is greater than 70% from half to full load current. Most of the loss is in the output Schottky rectifiers, a typical situation in high power 5V supplies.

Conclusion

Satisfactory commercial performance at 1KW can be achieved using just two transistors in half-bridge topology with an economical control chip. A simple proportional drive circuit easily provides low-loss switching when high speed third generation power switches are used.

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1) W.R. Skanadore, "Toward an Understanding and Optimal Utilization of Third Generation Bipolar Switching Transistors," Proceedings of INTELEC, 1982, pp 196-203, IEEE, 445 Hoes Lane, Piscataway, NJ 08854. IEEE Catalogue No. 82CH1818-4.

2) Bill Roehr, "An Effective Transient and Noise Barrier for Switching Power Supplies," Official Proceedings of the Eleventh International PCI Conference, 1986, pp 189-194, Intertec Communications, Inc. 2472 Eastman Ave., Bldg. 34, Ventura, CA 93003.

3) 2N6924 / 5 Data Sheet, General Semiconductor Industries, 2001 West 10th Place, Tempe, AZ 85281.

4) David B. Bell, "Designing Optimal Base Drive for High Voltage Switching Transistors," Proceedings of Powercon 7, Pages F1-1 to F1-12, Power Concepts, Inc., P.O. Box 5226, Ventura, CA 93003.

5) SG-3524 Data Sheet, Silicon General Semiconductor, 11651G Monarch St., Garden Grove, CA 92641.

RELATIONSHIP OF SWITCHING SPEEDS AND RBSOA TO BASE CIRCUIT DRIVE CONDITIONS*

by

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*Originally presented at SATECH '87 Conference.Proceedings Available from Intertec Communications, Inc., 2472 Eastman Ave. Bldg. 34, Ventura, CA 19003.

ABSTRACT

Results of testing high voltage transistors designed for off-line switching power supplies are discussed. The effects of using a base drive inductor on crossover times and reverse bias safe operating area are described. Tests are run to confirm that the amplitude of reverse base current is a major determinant of switching performance.

INTRODUCTION

The turn-off switching speeds and the Reverse Bias Safe Operating Area (RBSOA) are of primary importance in power switching applications, but are among the most elusive characteristics of all for a bipolar power transistor. The measured characteristics are explainable in a general fashion, but they are certainly not always predictable.

Some years ago, Pshaenich[1] performed a fairly extensive empirical study of several factors which affect switching and RBSOA. The test vehicle was the 2N6545/7 series of power switching transistors, which was the first generation of high-speed, rugged power transistors designed for off-line switching service. Today third generation[2] transistors provide considerable improvements in both switching speed and ruggedness. Consequently, the original investigation will be expanded to include these third generation parts.

An important variable not previously examined in detail is the effect of the base drive waveform on the performance of the first generation switch. Pshaenich used two reverse drive schemes: "constant current" and "constant voltage." The reported switching times were not greatly different provided the magnitude of the reverse drive current (I_{B2}) was the same for both drive schemes. Consequently, it seems likely that dynamic base impedance during turn-off may have been highly influencial in determining the reverse current during turn-off. In addition inductance in the base drive circuit has been reported by Hettersheid[3] to exert a favorable influence on turn-off performance. A base coil is widely used in European designs; additionally, some inductance is always present in any converter base drive circuitry, and is quite significant in those using a transformer coupled drive circuit. The issue of base drive inductance was not addressed in the earlier work, although some must have been present and must have influenced the "constant voltage" measurements to some degree.

The present investigation focuses on the effects of the base drive waveform on switching speeds and RBSOA. Data is taken using constant current drive as well as voltage drive with various values of inductance between the voltage source and the base. A comparison of first and third generation devices is shown.

THE BASE CURRENT WAVEFORM

The reverse base current during the turn-off crossover interval is the primary circuit-controlled factor in determining the switching speed. Variations in the transistor base-emitter impedance can make it difficult to maintain adequate reverse base current until turn-off is complete. Figures 1 and 2 show how the base voltage varies during turn-off. Figure 1 applies to a 2N6547 and Figure 2 applies to a 2N6923, a third generation part. Note that the older part shows a more pronounced increase in effective base impedance as the turn-off phase nears completion. This increasing impedance manifests itself as a negative-going base-emitter voltage, whereas in the third generation device, it remains positive through almost the entire turn-off event, going negative only after the collector current falls during turn-off.

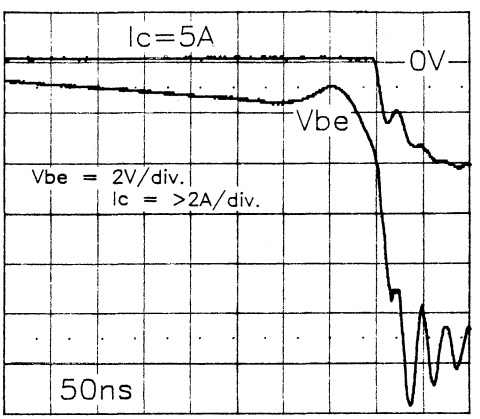

FIGURE 1—Base-Emitter Voltage and Collector Current at Turn-Off for a 2N6547

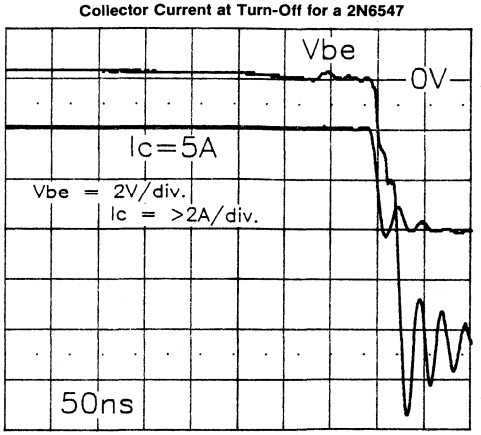

FIGURE 2—Base-Emitter Voltage and Collector Current at Turn-Off for a 2N6923

The older part would obviously benefit from being driven with a turn-off source which has a high compliance voltage or which uses some means to keep the current constant, such as a base coil. In the test circuit used, the off-bias voltage was adjusted to account for the base impedance so that I_{B2} was at a prescribed value during turn-off crossover time.

The circuit used is shown in Figure 3. Either R_{B2} or L_B is set to zero, depending on whether voltage/inductive drive or constant current drive is desired. Base current waveforms for drive schemes using constant current and a base inductor are shown in Figure 4. Note that the coil maintains a relatively constant di/dt, which can be controlled by the off-bias level, V_{BB2}. As the transistor switches off, the coil keeps the base current flowing continuously until collector current decays to zero. Then the forward biased base impedance becomes high and coil current flows into the emitter-base junction in the avalanche mode, as previously described by Hetterscheid.

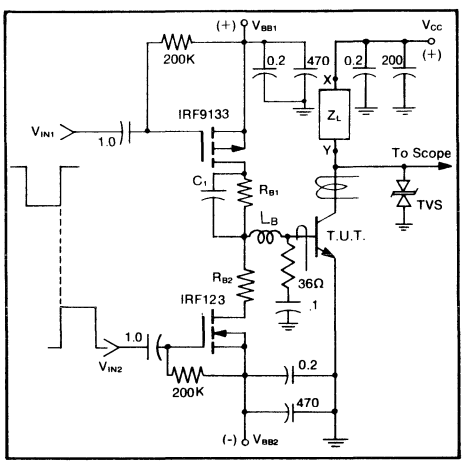

FIGURE 3—Switching/RBSOA Test Circuit

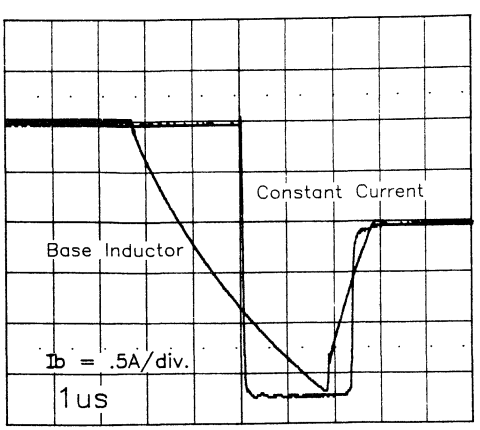

FIGURE 4—Base Current Waveforms When Using Constant Current or Base Inductor Drive

SWITCHING TEST RESULTS

Results of a set of switching tests are shown in Figures 5 and 6. Note that the crossover time improves as the base coil inductance is increased and that the optimum base current, regardless of the coil value, is around 1.7A. Collector current is 5A for these tests, three times the optimum I_{B2} value.

The price paid for improved crossover time is an increase in storage time as Figure 6 shows. During storage time, excess charge must be removed from the transistor. When it is removed slowly, charges deep in the collector have time to exit or recombine. Then, as the voltage rise time begins, there is little excess charge located remotely within the device to complicate turn-off; current fall time may approach its theoretical value which is determined primarily by the transistor's transition frequency, f_T.[4]

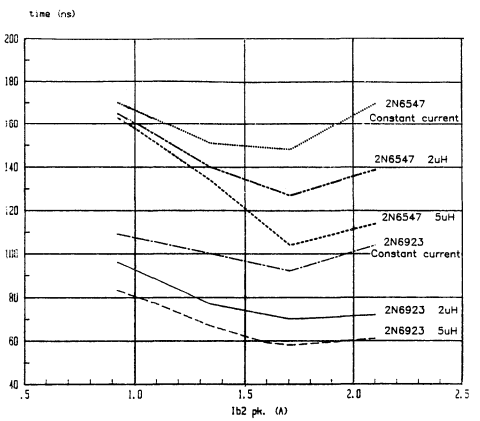

FIGURE 5—Crossover Time vs Peak Reverse Base Current For Various Off-Drive Conditions

$I_C = 5A$, $I_{B1} = 1A$

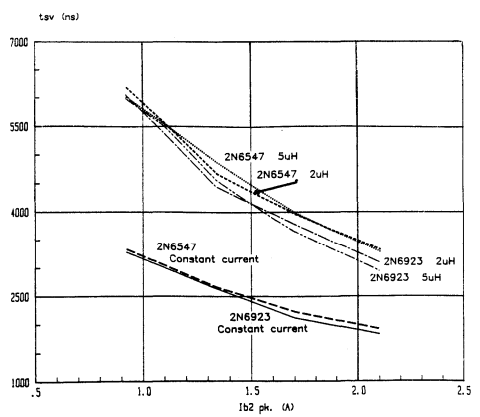

FIGURE 6—Storage Time vs Peak Reverse Base Current During Crossover Interval for Various Off-Drive Conditions

$I_C = 5A$, $I_{B1} = 1A$

Tests were also run at a collector current of 15A. This value is the design center current for the 2N6923 but the maximum rated current for the 2N6547, so the parts cannot be compared as equivalents. At this current level, it is difficult to achieve high I_{B2} with large inductors because the V_{BB2} voltage required exceeds the base-emitter junction breakdown voltage. However, a suitable combination was used and the resulting data is shown in Table 1. Note that the coil is very effective for the older part, causing about a 2:1 reduction in crossover time. The third generation part, however, shows only a slight improvement when a coil is used, because the newer part employs a structure which better controls the placement of stored charge, thereby facilitating the charge removal process.

The crossover waveforms associated with these tests are shown in Figures 7, 8, and 9. Comparing Figures 7 and 8, it is seen that the base coil has markedly improved current fall time. Not only does the coil reduce stored charge prior to current fall, but it maintains a more constant reverse current drive despite the rising base impedance as the transistor turns-off. Both effects reduce current "tailing." Figure 9 shows the waveforms for a 2N6923 under corresponding drive conditions.

TABLE 1
CROSSOVER TIME AT Ic = 15A
I_{B1} = 3A, V_{pk} = 450V, L_C = 1270μH, pw = 30μs

A. Constant Current Off-Drive R_{B2} = 1Ω, V_{B2} = 8.7V, $I_{B2(pk)}$ = 4.5A				
Device	Unit	t_{fi} (ns)	t_{rv}	t_c
2N6923	3	24	50	68
	5	21	48	64
	7	21	55	69
2N6547	10	103	146	256
	13	97	121	221
B. Inductive Off-Drive L_{B2} = 2μH, V_{B2} = 8.7V, $I_{B2(pk)}$ = 4.5A				
Device	Unit	t_{fi} (ns)	t_{rv}	t_c
2N6923	3	18	45	57
	5	16	43	53
	7	17	54	64
2N6547	10	58	108	169
	13	55	69	125

RESULTS OF RBSOA TESTING

Previous literature[5, 6] has indicated that the Reverse Bias Safe Operating Area (RBSOA) is highly dependent upon the reverse base drive employed. Too little drive is often bad because excessive dissipation occurs during the slow turn-off time; too much drive is often bad because excessive current crowding occurs in the transistor emitter sites. With many types of transistors, the condition for best switching does not coincide with the condition for best RBSOA. The effect of the base coil is generally not described in data sheets so tests were run in the circuit of Figure 3 to determine its effect.

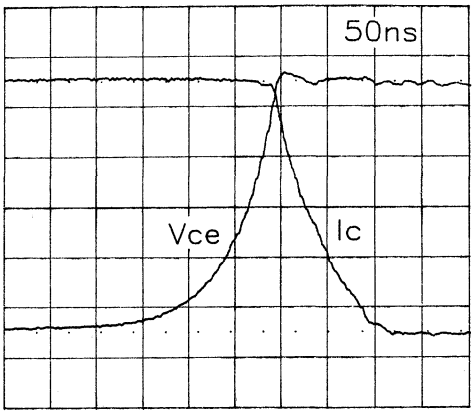

FIGURE 7—Crossover Waveform for 2N6547 Using Constant Current Drive
$I_{C(pk)}$ = 15A, V_{CE} = 450V, $I_{B2(pk)}$ = 4.5A

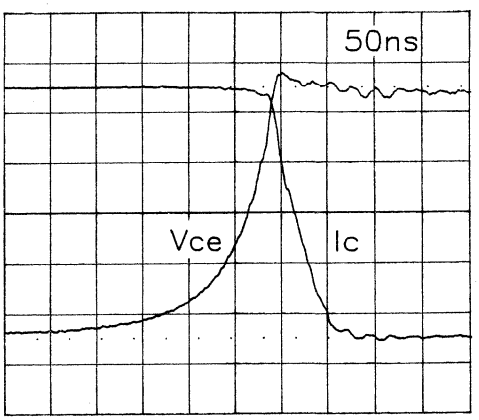

FIGURE 8—Crossover Waveform for a 2N6547 Using a Base Inductor
$I_{C(pk)}$ = 15A, V_{CE} = 450V, $I_{B2(pk)}$ = 4.5A

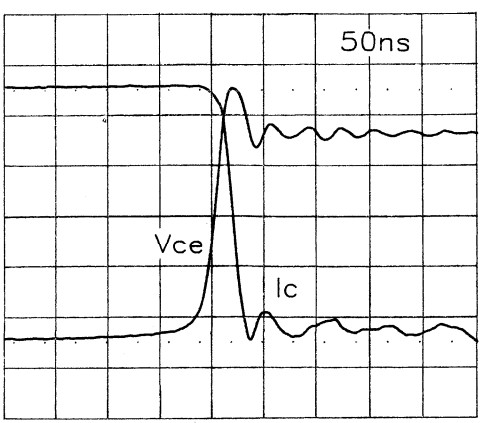

FIGURE 9—Crossover Waveform for a 2N6923 Using a Base Inductor
$I_{C(pk)}$ = 15A, V_{CE} = 450V, $I_{B2(pk)}$ = 4.5A

With drive conditions the same as those used for the data of Figures 4 and 5, resulting typical data is shown in Figure 10 for 2N6923 transistors. The curve is the same shape as that observed for crossover time, indicating that the off-drive current for fastest switching yields the lowest RBSOA at the collector clamp voltage of approximately 625 volts.

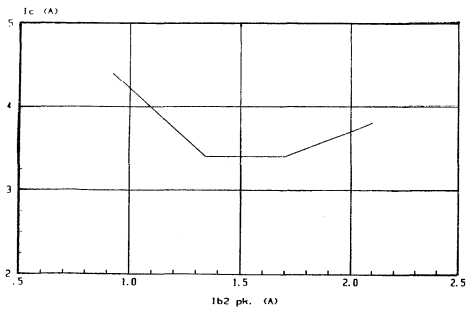

FIGURE 10—Typical Failure Current

2N6923, $V_{CE} = 625V$

This is characteristic of bipolar switching transistors of all types to varying degrees, and is most easily explained in terms of the I_{B2}/I_C ratio. For very low ratios, emitter current crowding is minimal, implying a somewhat higher current capability for a given clamp voltage. As this ratio is increased, emitter crowding becomes more important, serving to lower the current (or voltage) at which second breakdown occurs. As the ratio is further increased, the recovery current of the collector-base diode becomes comparable to and exceeds emitter current, so that despite the fact that emitter crowding is continuing, the actual emitter current is significantly lower, causing the *measured* collector current second breakdown limit to rise. Taking the ratio to the extreme and eliminating emitter current altogether ($I_{B2}/I_C = 1$) would therefore suggest that *all* of the measured collector current was actually collector-base diode recovery current, and that without emitter current crowding there would be a substantial improvement in RBSOA capability. This can be demonstrated for many bipolar transistors—usually, however, at only a fraction of rated $I_{C(max)}$[7].

Tests were run using a base coil or a resistance drive from 8 volts which approximates a constant current. Results depended only on the value of I_{B2} during crossover, not on its waveshape. Apparently, the charge history does not affect RBSOA. Other tests were run using different combinations of V_{BB2} and R_{B2} to achieve the given values of I_{B2}. The results were the same regardless of the V_{BB2}/R_{B2} combination.

CONCLUSION

The primary variable in determining crossover time is the magnitude of reverse base current (I_{B2}) applied to the transistor during the crossover interval. The source voltage level of the off-drive does not affect results when the value of I_{B2} is the same for various voltage levels. Depending on the way a transistor handles the depletion of stored charge, a base coil may offer a worthwhile improvement in crossover time. The improvement when using third generation transistors is measurable but probably not worth accepting the large increase in storage time resulting from use of the base coil.

The primary variable in determining RBSOA is also the magnitude of I_{B2} during the crossover interval. No significant improvement was discernable by using a base coil with third generation parts.

ACKNOWLEDGEMENTS

Thanks are due to William Skanadore, for his critical review of the text and many helpful suggestions, and to Pat Sarraillon for her transcription.

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Life Tests and Power-Age Capabilities

General Semiconductor Industries, Inc. has complete facilities to provide life tests and power-age on all devices they manufacture.

- High temperature storage life testing up to 200°C
- Voltage temperature stress tests at both ambient and elevated conditions.
- Free air operating life. Test capability in excess of 5000 positions for power transistors, and 15,000 positions for transient suppressors.

Environmental Test Capabilities

TEST	CAPABILITY
Acceleration, Sustained (Centrifuge)	0-20,000g (Standard)
Altitude (Barometric Prsssure, Reduced)	450,000ft. Simulated Altitude with TA = 25°C Capability
Dew Point	-65°C to 150°C
Moisture Resistance	-10°C to +85°C, 40% to 100% RH
Radiographic Inspection (X-Ray)	Resolution to 0.001 inch, 150kV—5mA
Salt Atmosphere/Spray	25°C to 35°C, up to 20% Salt Solution by Weight
Seal — Gross Leak	1 x 10^{-5} atm cc/sec, Fluorocarbons,
— Fine Leak	
—Fine Leak (Helium)	1 x 10^{-9} atm cc/sec
Symbolization (Resistance to Solvents)	
Shock (Mechanical)	Pulse Shape—Approximate Half-sine 500-1500g @ 0.5 msec
Steam Aged Solderability	
Temperature Cycling	-65°C to +200°C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Stud Torque, Terminal Torque
Thermal Shock	-65°C to +150°C
Vibration, Fatigue	60 Hz, 5-20g
Vibration, Variable Frequency	100-2000 Hz as Limited by 1 inch DA and 60 inches/second Velocity; 0-20g (Standard)

Military Test Standard Capabilities

TEST CATEGORY	MIL-STD-202	MIL-STD-750
Altitude	All Conditions	All Conditions
Dew Point		All Conditions
Moisture Resistance	All Conditions	All Conditions
Resistance to Solvents (Symbolization)	All Conditions	
Salt Atmosphere	All Conditions	All Conditions
Seal, Gross Leak	Method 112B Conditions A, B, & D	Method 1071 Conditions C, D, E, & K
Seal, Fine Leak	Only Method 112B Condition C, Pro. IIIA	Method 1071 Condition H
Solderability	All Conditions	All Conditions
Soldering Heat	All Conditions	All Conditions
Temperature Cycling	All Conditions, Except Method 107 Conditions D & E	
Terminal Strenght (Lead Integrity)	All Conditions	All Conditions
Thermal Shock, (Glass Strain)	All Conditions	All Conditions
Acceleration, Sustained (Centrifuge)	All Conditions, to 30kg	All Conditions, to 30kg
Shock (Mechanical)	Method 213B, Conditions D, E, & F	All Conditions
Vibration, Fatigue	All Conditions	All Conditions
Vibration, Variable Frequency	All Conditions	All Conditions
X-Ray	All Conditions	All Conditions

JAN/JANTX(V) AVAILABILITY

TransZorb Suppressors
MIL-S-19500

/434	/500		/507	
1N5555	1N5907	1N5647A	1N6036A	1N6055A
1N5556	1N5629A	1N5648A	1N6037A	1N6056A
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	1N5632A	1N5651A	1N6040A	1N6059A
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	1N5645A	1N5664A	1N6053A	1N6072A
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TRANSISTORS
MIL-S-19500

/349	/393	/394	/509	/514
2N3506	2N3418	2N4150	2N6338	2N6274
2N3507	2N3419		2N6341	2N6277
	2N3420			
	2N3421			

NOTE: Selected non-QPL products are available with processing to equivalent JTX levels per MIL-S-19500. For information, contact your local General Semiconductor Industries sales representative.

APPENDIX A

Module Military Processing

Processing Level	Testing Provided
H1	Sub-module screening
H2	Sub-module and module screening
H3	Sub-module and module screening and Group B and C Lot Testing

These screening levels can be ordered on GSI standard devices intended for military applications by adding the processing level code as a suffix to the standard part number.

Submodule Screening Test Plan

100% Testing	MIL-STD-750 Method
Storage, TA=175°C for 24 hours	1032
Temperature Cycle, 20 Cycles, TA= -65/+175°C, 15 min each extreme	1051C
Acceleration, 10kg, Y1 axis	2006
Fine Leak, $5x10^{-8}$ Atm cc/sec	1071G
Gross Leak, FC-43 @ 125° C for 1 min	1071D
Electrical #1, Read and Record	4022, 4016
Surge Pulse, 20 Pulses each device 10 us x 1000 us Pulse Wave form at Ipp	---
Electrical #2, IR (go no go)	4016
H.T.R.B., TA - 125°C @ VR for 96 hours	1038
Electrical #3, Read & Record BV 2% and IR 50% of Initial Value or 1 µA, whichever is greater	4022
Group A Electrical BV, Ir, VC (go no go)	4022, 4016

Module Screening Test Plan

100% TESTING	MIL-STD-750 Method
Storage, TA = +150°C for 24 hours	1032
Temperature Cycle, -65°/+150°C, 10 cycles 30 min. each extreme	1051F
Electrical #1 Read & Record BV & IR *	4022, 4016
Surge Pulse, 20 Pulses each device, 10 us x 1000 us Pulse Wave Form at Ipp	----
Electrical #2 IR (go no go) *	4016
H.T.R.B., TA = +125°C @ VR for 96 hours *	1038
Electrical #3, Read & Record BV ± 2% and IR 50% of Initial Value or 1 μA, whichever is greater*	4016
Marking	----
Group A Electrical, BV, IR, Vc (go no go) *	4022, 4016

Module Assembly Group B Testing

Inspections	Conditions	MIL-STD-750 Method	Small Lot Sample Plan
Sub Group 1			4/0
Solderability	----------	2026	
Resist. to Solvents	----------	1022	
Sub Group 2			6/0
Temperature Cycles	10 Cycles 30 minutes each extreme	1051F	
End Points*	-65° to 150°C BV, IR	4022, 4016	
Sub Group 3			12/0
Electrical *	BV, Ir	4022, 4016	
Operating Life *	@VR + 125°C 340 hours	1026	
End points *	BV = 5% IR = 50% of initial value or 20% IR (max) whichever is greater	4022, 4016	

Module Assembly Group C Testing

Inspections	Conditions	MIL-STD-750 Method	Small Lot Sample Plan
Sub Group 1			6/0
Physical Dimensions	------	2066	
Sub Group 2			6/0 Destructive Test
Terminal Strength	A, 10 lbs., 10 sec	2036	
Moisture Resistance	Omit Initial Conditioning	1021	
End Points *	BV, IR*	4022, 4016	
Sub Group 3			6/0
Shock	1500G, 0.5 ms, X1, Y1, Z1	2016	
Vibration		2056	
End Points *	BV, IR*		
Sub Group 4			6/0 Destructive Test
Salt Atmosphere		1041	
Sub Group 5			12/0
Steady State * Op. Life	@VR, + 125°C, 1000 hours *	1026	
End Points *	BV = 5% IR = 50% of initial value or 20% IR (max) whichever is greater		

* NOTE: For bidirectional devices test both polarities - Split hours on operating life test and surge pulses to 50% each polarity.

APPENDIX B

MIL Processing Test Plan for DLZ Series - H1 Versions (Unidirectional)

100% Screening/Group A, per MIL-S-19500	**MIL-STD-750 Method**
Internal visual	2072
Storage, TA = +150°C for 24 hours	1032
Temperature cycling, 10 cycles, 15 min. ea. ext.	1051F
Constant acceleration Y1 axis, 20kg	2006
Fine leak, 1 x 10^{-8} atmcc/sec	1071G
Gross leak	1071D
Elect 2, IR (go / no go)	
H.T.R.B., TA = +125°C for 160 hours VR = (rated)	1038
Elect 3, ΔIR = 100% or 20% of Group A limit, whichever is greater	
ΔBV = $\pm$ 2% from initial reading	
Marking	
Final Elect (all Group A parameters - go / no go)	

ATTRIBUTES DATA SUPPLIED

MIL Processing Test Plan for DLZ Series - H1 Versions (Bidirectional)

100% Screening/Group A, per MIL-S-19500	MIL-STD-750 Method
Internal visual	2072
Storage, TA = +150°C for 24 hours	1032
Temperature cycling, 10 cycles, 15 min. ea. ext.	1051F
Constant acceleration Y1 axis, 20kg	2006
Fine leak, 1 x 10^{-8} atmcc/sec	1071G
Gross leak	1071D
Elect 1, Read & record BV, IR	
Pulse stress, 10 pulses ea. dir. Ip = 10A tp = 8 x 20 µsec	
Elect 2, IR go / no go (both dir.)	
H.T.R.B., TA = + 125°C for 80 hours, VR = (rated) (pol. A)	1038
Elect 3, ΔIR = 100% or 20% of Group A limit, whichever is greater (pol. A)	
H.T.R.B., TA = + 125°C for 80 hours, VR = (rated) (pol. B)	1038
Elect 4, ΔIR = 100% or 20% of Group A limit, whichever is greater (pol. B)	
ΔBV = ± 2% from initial reading (pol. A & B)	
Marking	
Final Elect (all Group A parameters - go / no go)	

ATTRIBUTES DATA SUPPLIED

MIL Processing Group B Test Plan for DLZ Series - H2 Versions (Unidirectional)

LTPD	Subgroup	Test	MIL-STD-750 Method
15	1	Solderability	2026
		Resistance to solvents	1022
10	2	Elect. BV, IR (limits)	4016, 4022
		Temperature cycling, 10 cycles, 15 min.	1051F
		Fine leak, 1 x 10^{-8} atmcc/sec Gross leak - no bubbles	1071G 1071D
		Elect. BV, IR (limits)	4016, 4022
5	3	Elect. BV, IR (limits)	4016, 4022
		Pulse, Ip = 10A, tp = 8 x 20μsec, 20 pulses	
		Elect. IR (limit)	4016
		Steady-state operation life, TA = + 125°C, VR = (rated), for 340 hours	1027
		Elect. ΔIR = 100% or 20% of Group A limit, whichever is greater	4016
		ΔBV = ± 5% from initial reading	4022
20	4	Decap, Bond strength	2037
	5	N/A	
7	6	Elect. BV, IR (limits)	4016, 4022
		High-temperature life (non-operating) TA = + 150°C for 340 hours	1032
		Elect. ΔIR = 100% or 20% of Group A limit whichever is greater	4016
		ΔBV = ± 5% from initial reading	4022

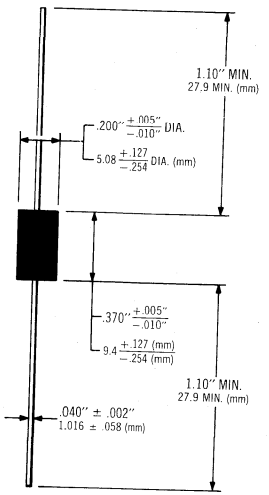
NOTE: Use small lot sampling plan for lot sizes < 500 pcs.

MIL Processing Group B Test Plan for DLZ Series - H2 Versions (Bidirectional)

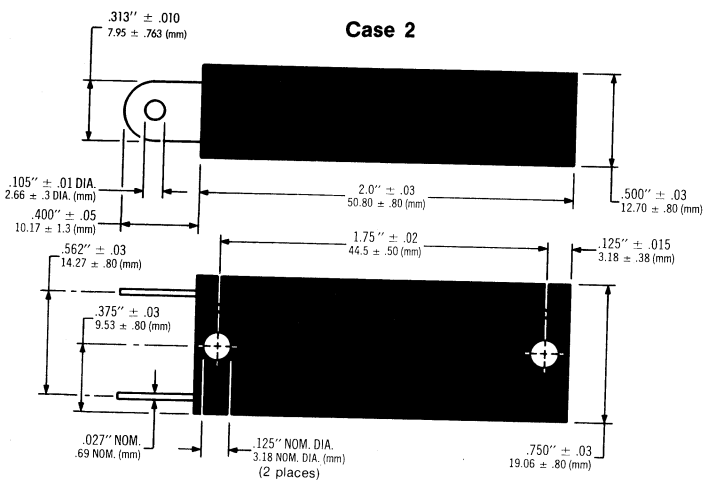
LTPD	Subgroup	Test	MIL-STD-750 Method
15	1	Solderability	2026
		Resistance to solvents	1022
10	2	Elect. BV, IR (limits) (both pol.)	4016, 4022
		Temperature cycling, 10 cycles, 15 min.	1051F
		Fine leak, 1 x 10^{-8} atmcc/sec Gross leak - no bubbles	1071G 1071D
		Elect. BV, IR (limits) (both pol.)	4016, 4022
5	3	Elect. BV, IR (limits) (both pol.)	4016, 4022
		Pulse, Ip = 10A, tp = 8 x 20μsec, 10 pulses ea. dir.	
		Elect. IR (limit) (both pol.)	4016
		Steady-state operation life, TA = + 125°C, VR = (rated), for 170 hours (pol. A)	1027
		Elect. ΔIR = 100% or 20% of Group A limit, whichever is greater (pol. A)	4016
		Steady-state operation life, TA = + 125°C, VR = (rated), for 170 hours (pol. B)	1027
		Elect. ΔIR = 100% or 20% of Group A limit, whichever is greater (pol. B)	4016
		ΔBV = ± 5% from initial reading (pol. A&B)	4022
20	4	Decap, Bond strength	2037
	5	N/A	
7	6	Elect. BV, IR (limits) (both pol.)	4016, 4022
		High-temperature life (non-operating) TA = + 150°C for 340 hours	1032
		Elect. ΔIR = 100% or 20% of Group A limit whichever is greater (pol. A&B)	4016
		ΔBV = ± 5% from initial reading (pol. A&B)	4022

NOTE: Use small lot sampling plan for lot sizes < 500 pcs.

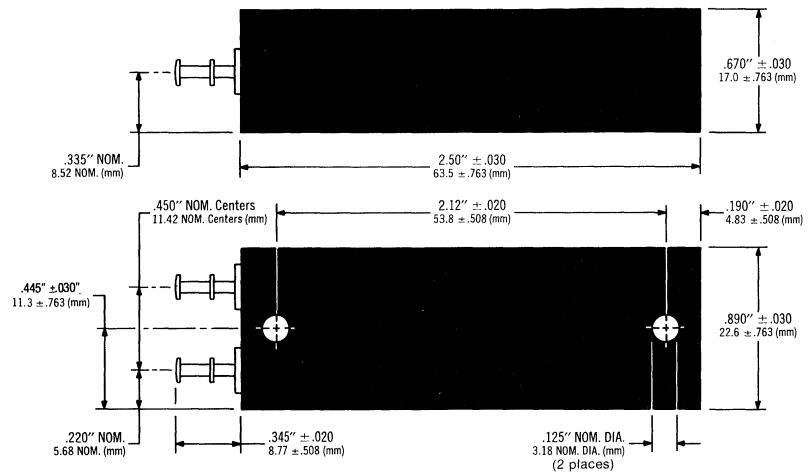
Case 1


1.10" MIN.
27.9 MIN. (mm)
.200" +.005" −.010" DIA.
5.08 +.127 −.254 DIA. (mm)
.370" +.005" −.010"
9.4 +.127 (mm) −.254 (mm)
1.10" MIN.
27.9 MIN. (mm)
.040" ± .002"
1.016 ± .058 (mm)

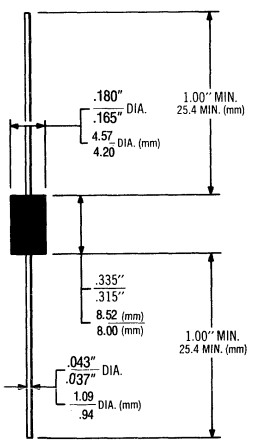
Case 2


.313" ± .010
7.95 ± .763 (mm)
.105" ± .01 DIA.
2.66 ± .3 DIA. (mm)
.400" ± .05
10.17 ± 1.3 (mm)
2.0" ± .03
50.80 ± .80 (mm)
.500" ± .03
12.70 ± .80 (mm)
.562" ± .03
14.27 ± .80 (mm)
1.75" ± .02
44.5 ± .50 (mm)
.125" ± .015
3.18 ± .38 (mm)
.375" ± .03
9.53 ± .80 (mm)
.027" NOM.
.69 NOM. (mm)
.125" NOM. DIA.
3.18 NOM. DIA. (mm)
(2 places)
.750" ± .03
19.06 ± .80 (mm)

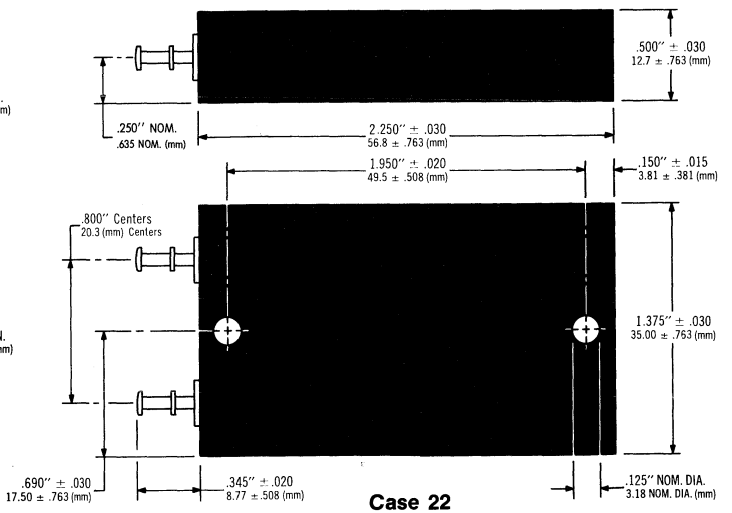
CASE OUTLINES—DIODES



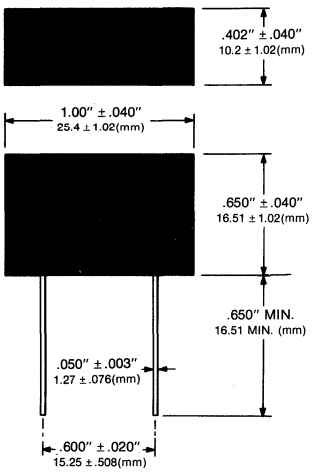
Case 3



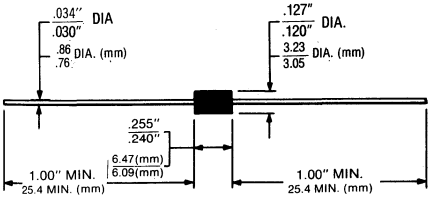
Case 7



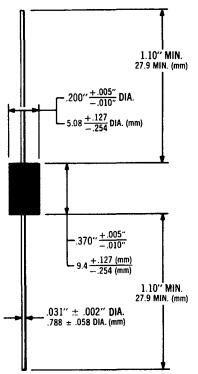
Case 22



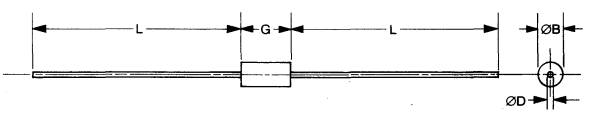
Case 24



Case 25



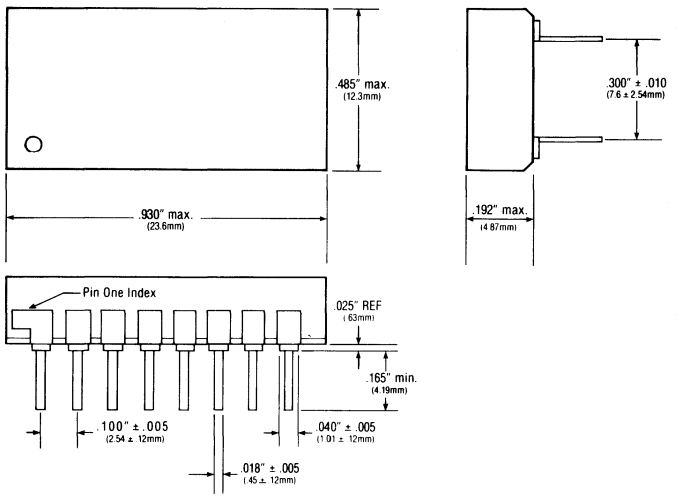
Case 26



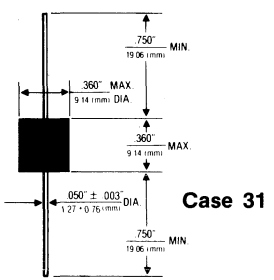
LETTER	DIMENTIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
ØB	.115	.140	2.92	3.56	3
ØD	.037	.042	.94	1.07	4
G	.150	.300	3.81	7.62	4
L	.900	1.300	22.86	33.02	

Case 27

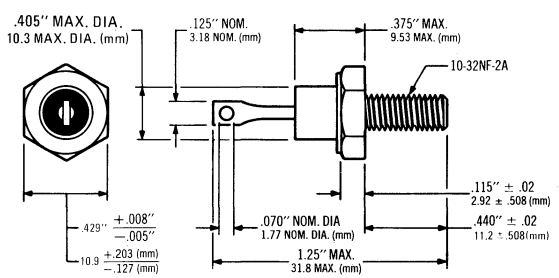
CASE OUTLINES—DIODES



Case 29

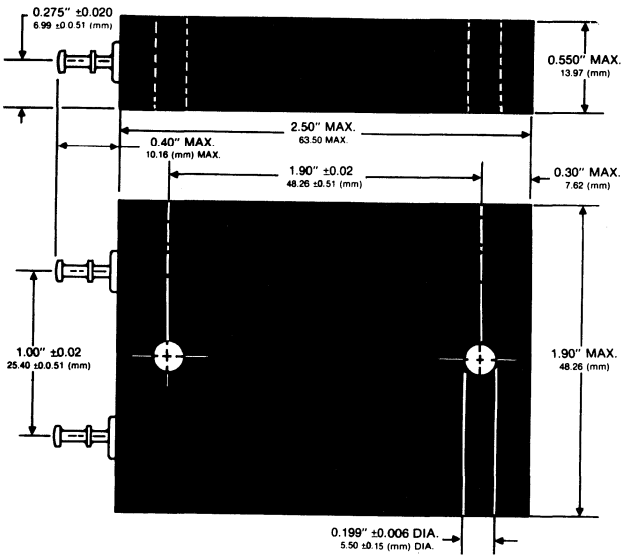


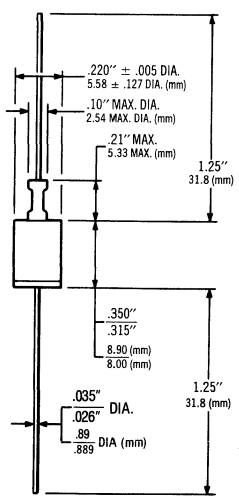
Case 31



DO-203AA
(DO-4)

Case 32

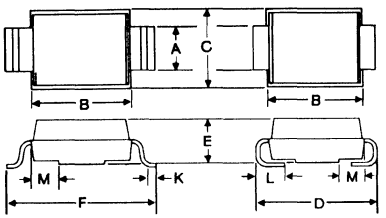




DO-202AA
(DO-13)

DO-215AA
"Gull Wing"

DO-214AA
"C Bend"
(Modified J-Bend)

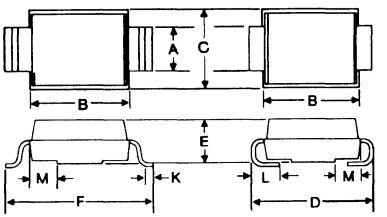


DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.077	.160	.130	.205	.075	.235	.015	.030	.038
MAX	.083	.180	.155	.220	.095	.255	.030	.060	.058
DIMENSIONS IN MILLIMETERS									
MIN	1.96	4.06	3.30	5.21	1.91	5.97	0.38	0.76	0.97
MAX	2.10	4.57	3.81	5.59	2.41	6.48	0.76	1.52	1.47

Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

DO-215AB
"Gull Wing"

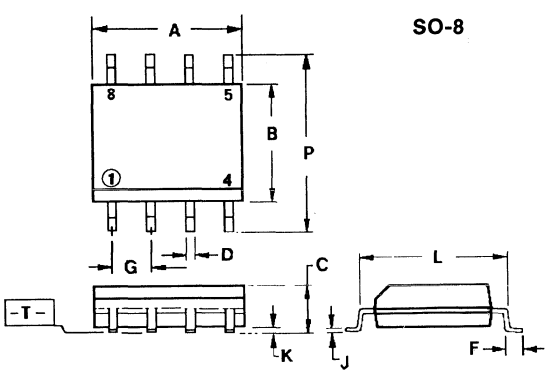
DO-214AB
"C Bend"
(Modified J-Bend)



DIMENSIONS IN INCHES									
	A	B	C	D	E	F	K	L	M
MIN	.115	.260	.225	.305	.075	.380	.025	.030	.038
MAX	.121	.280	.245	.320	.095	.255	.400	.060	.053
DIMENSIONS IN MILLIMETERS									
MIN	2.92	6.60	5.72	7.75	1.91	9.65	0.64	0.76	0.97
MAX	3.07	7.11	6.22	8.13	2.41	10.16	1.02	1.52	1.35

Typical Standoff Height: 0.004" - 0.008" (0.1mm - 0.2mm)

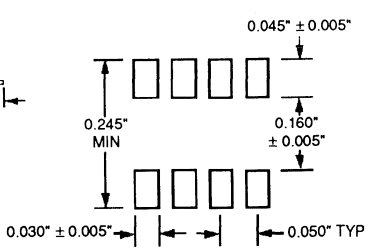
SO-8



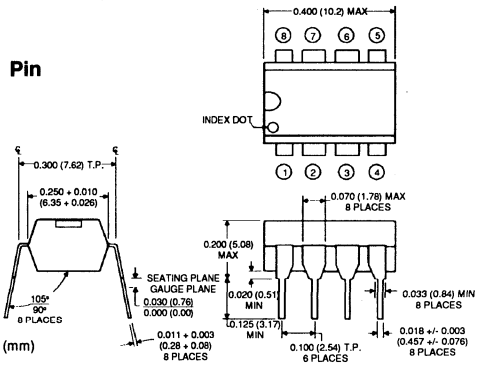
NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION "A" IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖	0.25 (0.010) Ⓜ	A ②

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.206
P	5.79	6.20	0.228	0.244

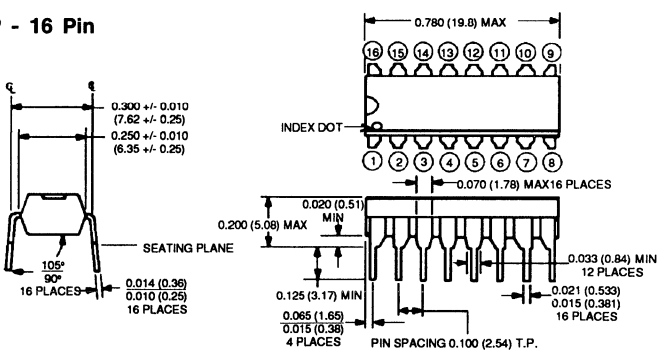


Plastic DIP - 8 Pin



Measurements in inches (mm)

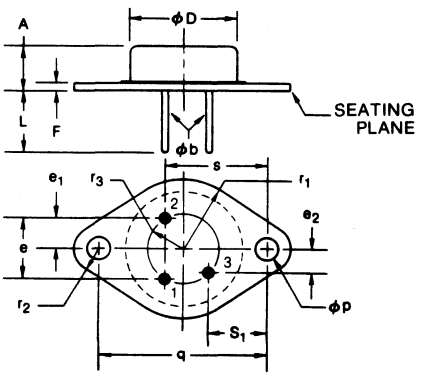
Plastic DIP - 16 Pin



Measurements in inches

CASE OUTLINES—TRANSISTORS

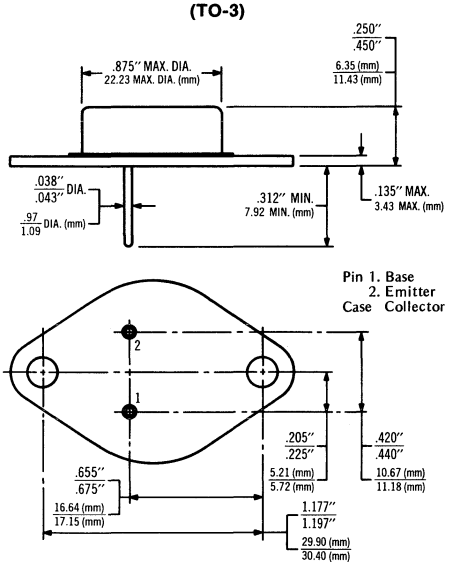
F-30
(3 Terminal TO-3)
Isolated Collector



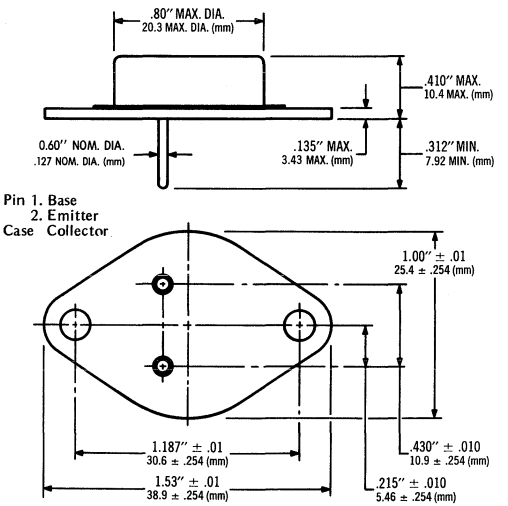
SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	6.35	11.43	0.250	0.450	
ϕb	0.97	1.09	0.038	0.043	3 leads
ϕD		22.23		0.875	
e	10.67	11.18	0.420	0.440	
e_1	5.21	5.72	0.205	0.225	
F		3.43		0.135	
L	7.92		0.312		3 leads
ϕp	3.84	4.09	0.151	0.161	
q	29.90	30.40	1.177	1.197	
r_1		13.34		0.525	
r_2		4.78		0.188	
s	16.64	17.15	0.700	0.730	
S_1	10.03	10.29	0.395	0.405	
e_2	3.68	4.19	0.145	0.165	
r_3	6.30	6.40	0.248	0.252	

PIN DESCRIPTION:
1. BASE
2. EMITTER
3. COLLECTOR

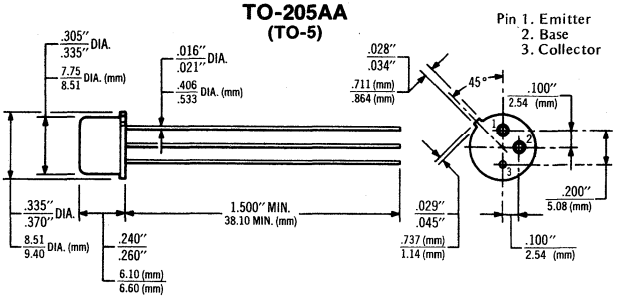
TO-204AA
(TO-3)



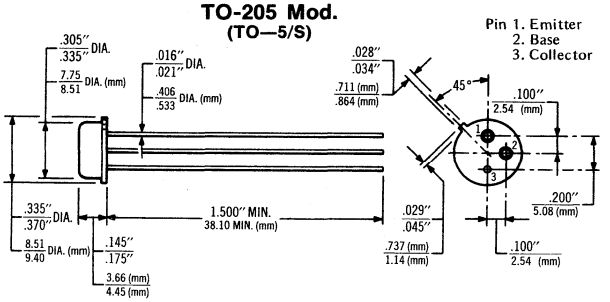
TO-204AE
(TO-3 Mod.)



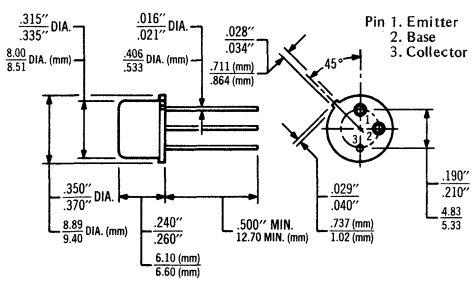
TO-205AA
(TO-5)



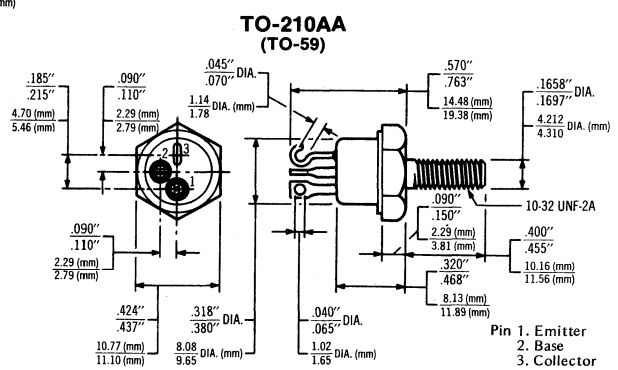
TO-205 Mod.
(TO—5/S)

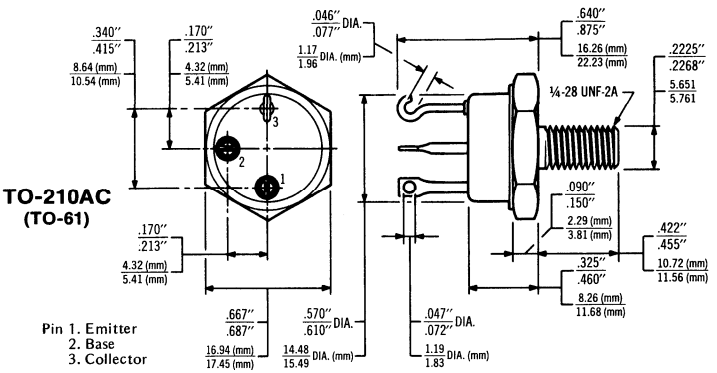


TO-205AD
(TO-39)



TO-210AA
(TO-59)

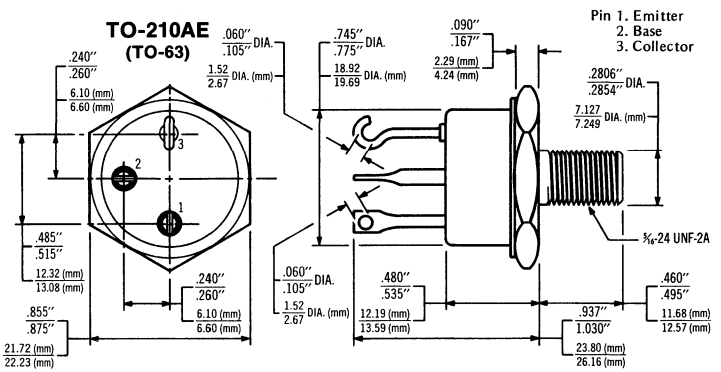


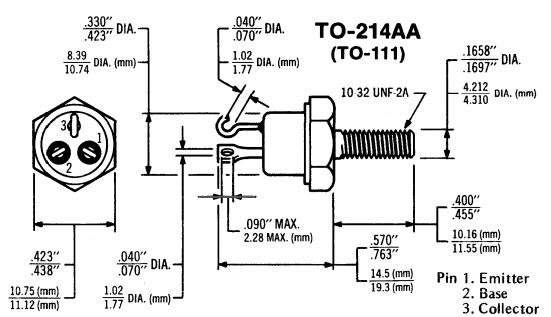


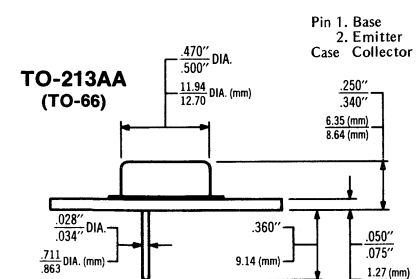
CROSS REFERENCE

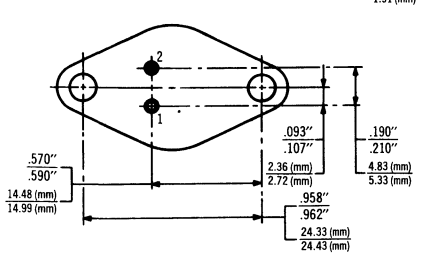
Former JEDEC outlines to current 200 series outlines

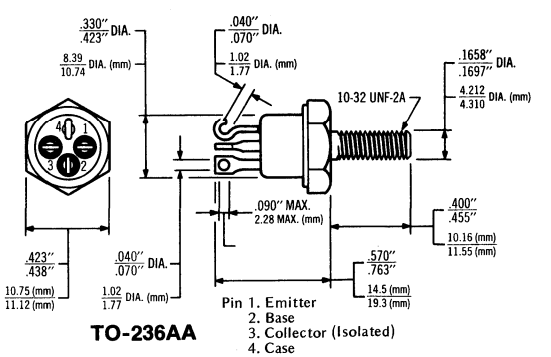
Outline Family	Reference To DO-200 Series
DO-4	DO-203AA, MA
DO-5	DO-203AB, MB
DO-6	
DO-7	DO-204AA, MA
DO-8	DO-205AA, MA
DO-9	DO-205AB, MB
DO-10	
DO-11	
DO-12	DO-202MA, 210AC
DO-13	DO-202AA
TO-3	TO-204AA, MA
TO-5	TO-205AA
TO-39	TO-205AD
TO-59	TO-210AA
TO-61	TO-210AC
TO-63	TO-210AE
TO-66	TO-213AA
TO-111	TO-214AA











LEAD TAPE PACKAGING STANDARD

I. AXIAL LEADED COMPONENTS

1. This Section covers packaging requirements for the following GeneralSemiconductor Industries' axial-leaded components used in automatic testing and insertion equipment. General Semiconductor Industries' cases covered by this Section are Case 1, Case 7, Case 25, and DO-13.

2. This Section establishes GSI standard practices for lead-tape packing of axial-leaded components. Packaging shall consist of axial leaded components mounted by the leads on pressure-sensitive tape, wound onto a reel. This packaging practice meets the requirements of EIA standard RS-296D: Lead Taping of Components in Axial Lead Configuration for Automatic Insertion" Level 1.

3. Component leads must meet the following standards:
   i) Leads shall not be bent beyond .047 " (1.2mm) from their nominal position.
   ii) The "C" dimensions shall be governed by the overall of the packaged component. The distance between the flanges shall be .059" (1.5mm) to .315" (8mm) greater than the overall components.
   iii) Leads shall not extend beyond the tape more than .063" (1.6mm) and shall be contained between the tapes at a minimum of .126" (3.2 mm).
   iv) Cumulative dimension "A" tolerance shall not exceed .059" over five consecutive components.

4. Orientation of all polarized components must be oriented in one direction. The cathode lead tape shall be colored, and the anode lead tape shall be white.

5. Reeling must meet the followling standards:
   i) Components on a reel shall not be representative of more than four date codes.
   ii) A minimum of 1 foot leader tape shall be provided before the first component on the reel and at the end of each reel.
   iii) Kraft paper is wound between the layers of taped components for their protection.
   iv) Components shall be positioned perpendicularly between pairs of .197" (5mm) to .250" (6.35mm).
   v) Centering of components between the tape shall be such that the difference between D1 and D2 does not exceed .055".
   vi) Quantity per reel is indicated in Table 1. Orders for tape and reeled product will be shipped only in full reel increments.
   vii) A maximum of 25% of the components per reel quantity may be missing without consecutive missing components.
   viii) Each reel is adequately protected in an appropriate container.

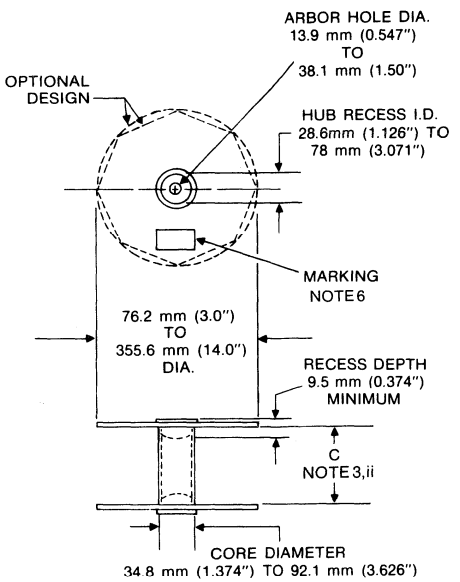
I. AXIAL LEADED COMPONENTS (continued)

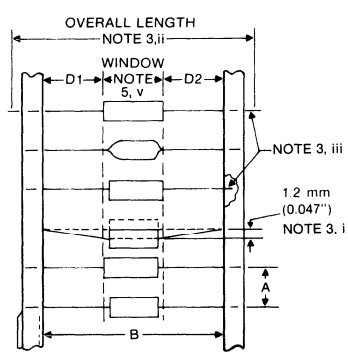
6. Marking of reel shall consist of part numbers, purchase order number, quanitity, date of reeling, manufacturer's name and /or trademark.

TABLE I - PACKAGING DETAILS AXIAL LEADED COMPONENTS

GSI CASE TYPE	QUANTITY PER REEL	COMPONENT SPACING "A"		TAPE SPACING "B"		MAX. OFF ALIGNMENT		[1] REEL DIMENSION	
		in.	mm	in.	mm	in.	mm	"C"	"D" MAX
Case 1	1,000	.395	10.0	2.06	53	.047	1.2	3.0	14.0
Case 7	2,000	.200	5.0	2.06	53	.047	1.2	3.0	14.0
Case 25	3,000	.200	5.0	2.06	53	.047	1.2	3.0	14.0
DO-13	1,000	.395	10.0	2.06	53	.047	1.2	3.0	14.0

[1] Reel dimensions are in inches.





II. SURFACE MOUNT COMPONENTS

General Semiconductor Industries offers tape and reeling for DO-214 and DO-215 surface mount packages to meet the industry trend to utilize automatic placement equipment. GSI follows the requirements of EIA 481-1.

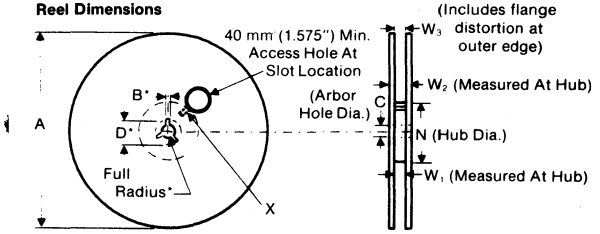
The material is a plastic carrier tape with embossed cavities in which the components are placed. A seeling tape is applied to the carrier tape to prevent the components from falling out. The sealing tape may not extend over the edge of the carrier tape nor extend over any part of the sprocket holes. GSI maintains sealing tape pull strength of 40 grams psi ± 30 grams.

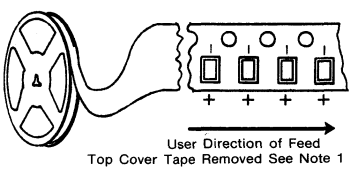
Two terminal polarity device will have cathode (positive polarity for TVS and zeners) adjacent to the sprocket holes. All units will be oriented in one direction.

Leader tape shall be 560 mm maximum with a minimum of 40 empty component carrier pockets covered with tape.

GSI CASE TYPE	TAPE SIZE	REEL SIZE	QTY / REEL	
			7"	13"
DO-214AA/215AA	12mm	7" & 13"	900	3,000
DO-214AB/215AB	16mm	13"	--	3,000

Reel Dimensions





*Drive spokes optional, if used asterisked dimensions apply.

Tape Size	A Max.	B* Min.	C	D* Min.	N	W_1	W_2 Max.	W_3	X
12mm	178 (7.00)	2 (.079)	13.0 ± 0.20 (.512 ± .008)	20.2 (.795)	60 ± 1.0 (2.36 ± .040)	$12.4^{+2.0}_{-0.0}$ ($.488^{+.078}_{-0.0}$)	18.4 max. (.724)	11.9 Min. (.469) 15.4 Max. (.607)	5 ± .50 (.197 ± .020)
12mm	330 (12.992)	2 (.079)	13.0 ± 0.20 (.512 ± .008)	20.2 (.795)	100 ± 1.0 (3.94 ± .040)	$12.4^{+2.0}_{-0.0}$ ($.488^{+.078}_{-0.0}$)	18.4 max. (.724)	11.9 Min. (.469) 15.4 Max. (.607)	5 ± .50 (.197 ± .020)
16mm						$16.4^{+2.0}_{-0.0}$ ($.645^{+.078}_{-0.0}$)	22.4 max. (.881)	15.9 Min. (.625) 19.4 Max. (.763)	7 ± .50 (.275 ± .020)

NOTES

REGIONAL SALES OFFICES

WESTERN REGIONAL OFFICE

GSI
P.O. Box 1870
Rocklin, CA 95677
TEL: 916-632-1404
FAX: 916-632-1470

EASTERN REGIONAL OFFICE

GSI
24 Lexington Street
Burlington, MA 01803
TEL: 617-229-1915
FAX: 617-229-2728

CENTRAL REGIONAL OFFICE

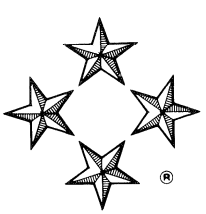
GSI
1900 East Golf Road #M100
Schaumburg, IL 60173-5011
TEL: 708-240-5657
FAX: 708-240-5620

NORTHERN EUROPE REGIONAL OFFICE

GSI N. Europe Operations
Silbury Business Center
356 Silbury Boulevard
Central Milton Keynes
MK9 2LR
UNITED KINGDOM
TEL: (44)(908) 60-48-48
FAX: (44)(908) 66-26-15

SOUTHERN EUROPE REGIONAL OFFICE

Square D/GSI France
50, Av du Vieux Chemin de St. Denis
92390 Villeneuve la Garenne
FRANCE
TEL: (33)(1) 40-85-14-16
FAX: (33)(1) 40-85-14-21



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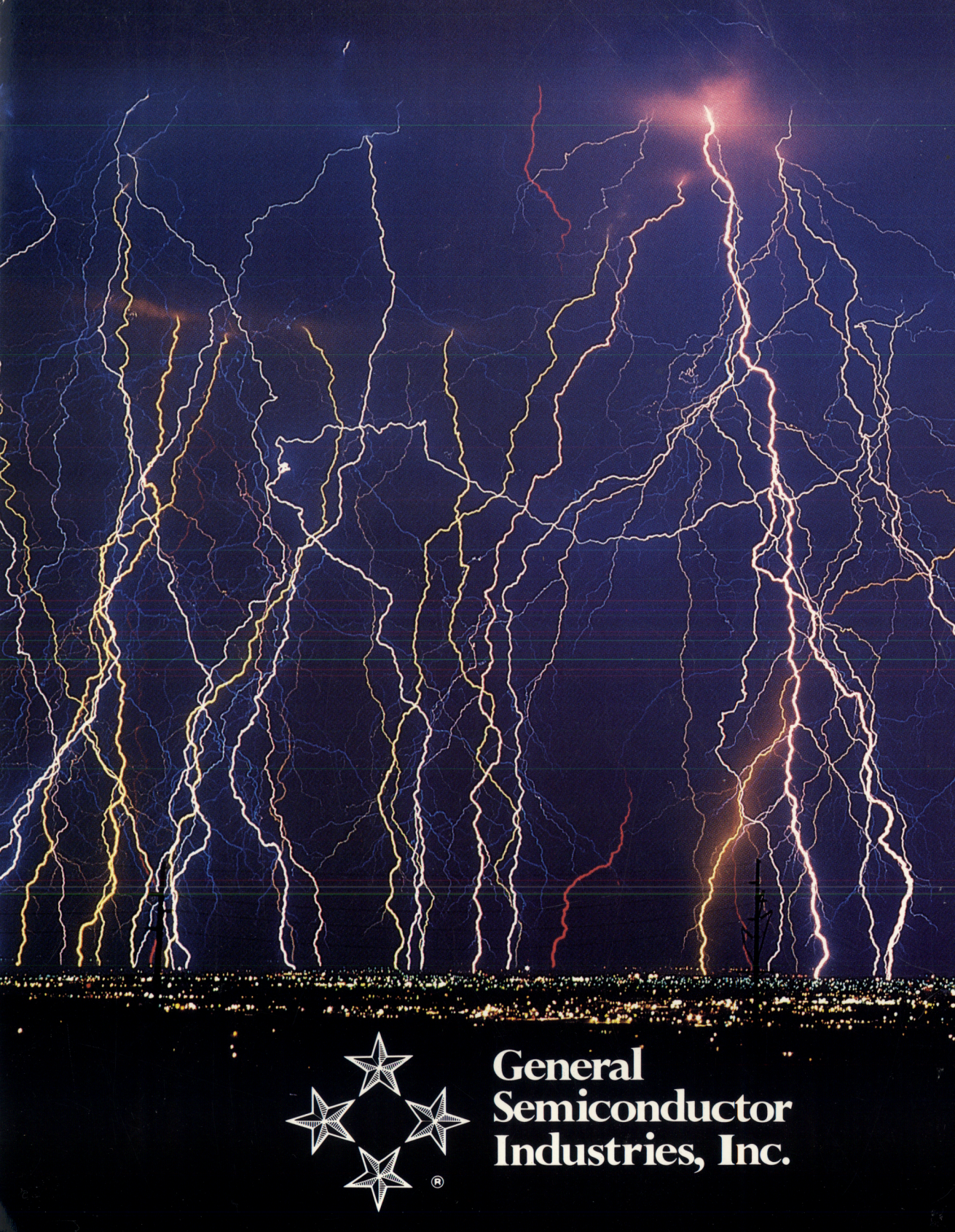

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